

Chapter 2

High-Resolution Wideband Continuous-Time $\Sigma \Delta$ Modulators

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2.1 Introduction

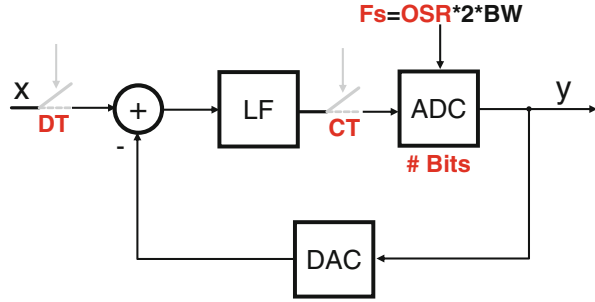
This paper is organized as follows. In Sect. 2.2 some key architectural choices and trade-offs are discussed when defining the optimal noise-transfer function (NTF) of a wideband and high-resolution delta-sigma modulator. Among the architectural choices are type and order of the loopfilter, ADC resolution, sampling frequency and number of stages. Important limiting factors related to the practical implementation of wideband delta-sigma converters are discussed in Sect. 2.2. Examples of such non-idealities are metastability, excess loop delay (ELD), non-linearity, and phase noise. These aspects can be taken into account on the architectural level to mitigate their impact. In Sect. 2.4 recent designs are presented that have pushed the envelope with respect to bandwidth and linearity. The conclusions are drawn in Sect. 2.5.

2.2 Architectural Choices

There are several important choices to be made when defining the architecture and the optimal noise transfer function of a delta-sigma modulator for given bandwidth and resolution specifications. Figure 2.1 shows the basic block diagram of a single-loop delta-sigma modulator that consists of a loopfilter, A/D converter (ADC) and feedback D/A converter (DAC). The main degrees of freedom are the position of the sampler, the loopfilter (LF) type, order and oversampling ratio (OSR) and the accuracy of the ADC and DAC.

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Fig. 2.1 Basic block diagram of a delta-sigma modulator



2.2.1 Sampler

The sampler is typically placed either at the input of the delta-sigma modulator or at the input of the ADC. The first configuration represents a discrete-time delta-sigma modulator which can be implemented with switched-capacitor circuits while the latter configuration is a continuous-time modulator with a continuous-time loopfilter implementation. Since a discrete-time modulator has the sampler directly at the input it suffers from aliasing of signals that may be present close to (multiples of) the sampling frequency. Therefore, an anti-alias filter is required in front of the delta-sigma modulator to adequately suppress aliased signals. In case of a continuous-time modulator, the loopfilter acts as an inherent anti-alias filter which relaxes or even eliminates the anti-alias filter in front of the modulator. In case of a switched-capacitor filter implementation, the filter coefficients are defined as capacitor ratios which are very accurate and do not require calibration. Also, the bandwidth of a discrete-time modulator can be easily scaled by changing the sampling frequency without the need for adapting the filter coefficients. This is different from a continuous-time filter implementation where filter coefficients are determined by e.g. RC time constants that are subject to significant spread ($\sim 40\%$) which also need to be tuned in case of sampling rate scaling. A drawback of switched-capacitor circuits is that the resolution depends on the settling accuracy of charge transfers which requires high-speed amplifiers, especially if the sampling frequency is high. Continuous-time filters do not have the settling requirement and usually require lower bandwidth amplifiers. Therefore, in the bandwidth range of several tens of MHz and above, many continuous-time modulators have been reported in literature [1–7].

2.2.2 Filter

The noise transfer function of the delta-sigma modulator is determined by the loopfilter order, filter type and the choice of filter coefficients. As an example, Fig. 2.2 shows the magnitude plots of two different NTF curves (both second-order).

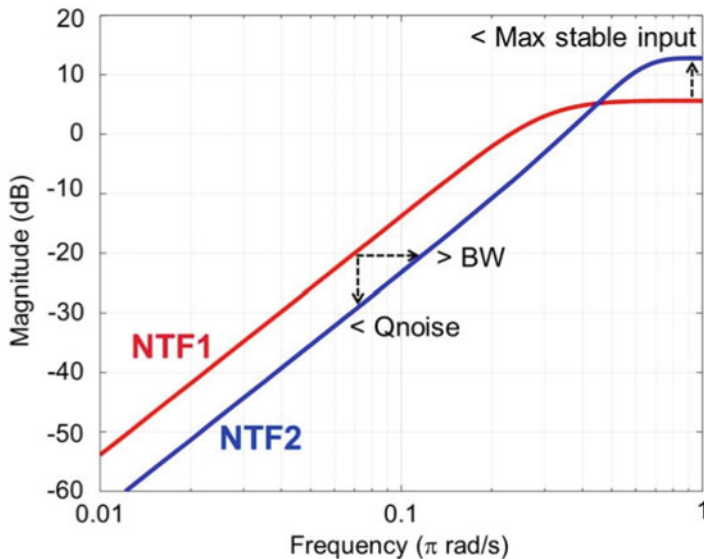


Fig. 2.2 Magnitude plot of second-order NTFs with different OOB gains

The blue transfer (NTF2) has lower low-frequency NTF gain compared to the red transfer (NTF1) but as a result it has higher OOB gain compared to NTF1. From Fig. 2.2 it becomes clear that a higher OOB gain leads to lower quantization noise (Qnoise) in a certain target (low-frequency) bandwidth or to an increased bandwidth (BW) for a certain target noise suppression. Besides the improved low-frequency quantization noise suppression and/or increased bandwidth, a negative implication of a higher OOB gain is that the maximum stable input level of the modulator is lower. The impact of a smaller maximum input signal level is that the modulator will become more sensitive to other noise sources like circuit noise. Further increasing the OOB NTF gain will ultimately lead to an inherently unstable modulator even without an input signal. Therefore, the design of the NTF will be a compromise between the maximum stable input level, bandwidth and quantization noise suppression.

Besides optimizing the NTF OOB gain as described above, the bandwidth and/or noise suppression can be improved by increasing the order of the loopfilter. This is shown in Fig. 2.3 where a third-order NTF is compared with a fifth-order NTF. At low frequencies the fifth-order NTF provides much better quantization noise suppression. Notice that at a certain frequency (F_x), the NTF curves cross and the fifth-order NTF becomes worse compared to the third-order NTF. As this crossing frequency will move to lower frequencies for higher-order filters it does not pay off to go to very high filter orders when the oversampling ratio is low (if $F_x < \text{bandwidth}$), which is usually the case for wideband delta-sigma modulators.

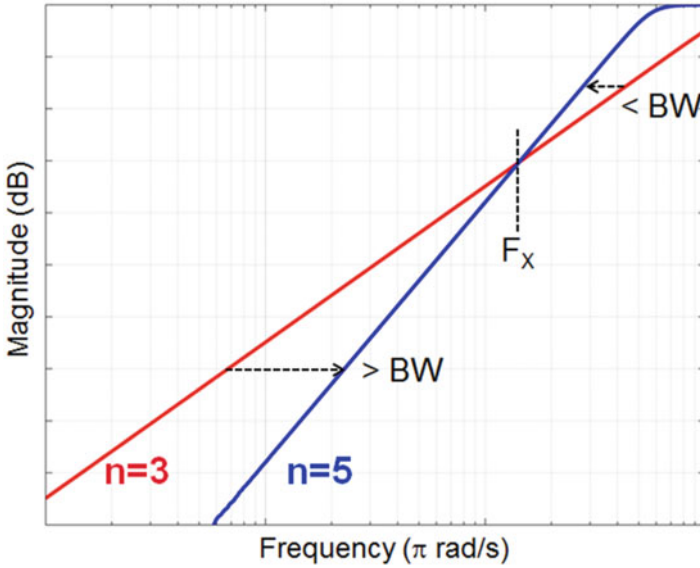


Fig. 2.3 Magnitude plot of third-order and fifth-order NTFs

Further optimization can be done by optimally distributing the NTF zeros in the signal band of interest as shown in Fig. 2.4. Spreading the NTF zeros in the signal band gives much better overall suppression of the quantization noise compared to the situation where all NTF zeros are at DC.

2.2.3 ADC

The quantization noise of the ADC is filtered by the NTF as was described in the previous section. Due to the noise-shaping and oversampling of the modulator, the intrinsic resolution of the ADC can be as low as 1-bit, while the accuracy in a specific bandwidth can still be very high. Moreover, employing a 1-bit ADC has the advantage that only a 1-bit DAC is required in the feedback path of the delta-sigma modulator, which is inherently linear. In wideband delta-sigma modulators, usually a 1-bit ADC is not enough to achieve the bandwidth and resolution requirements. Typically a 4-bit ADC is utilized [3–6] which seems to be a good compromise between ADC complexity, speed and performance. Increasing the number of bits in the ADC can reduce the quantization noise and increase the bandwidth in two ways. Firstly, the quantization noise itself will be smaller as a result of more bits in the ADC. Secondly, as the quantization noise in the delta-sigma loop becomes smaller, the maximum OOB gain of the NTF can be increased while still having a sufficiently large maximum stable input level. Increasing the OOB gain helps to further reduce

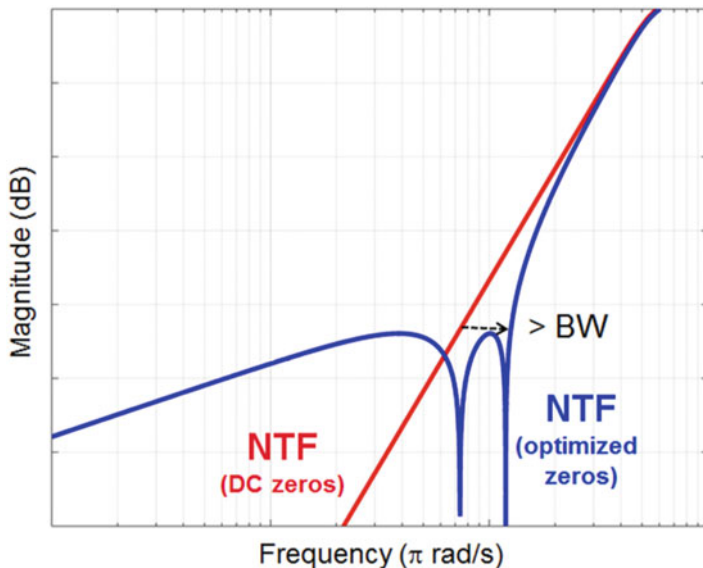


Fig. 2.4 Magnitude plot of fifth-order NTFs with DC zeros and optimized zeros

the in-band quantization noise as was shown in Fig. 2.2. As a result of the NTF optimization, the quantization noise floor in the signal band can be improved more than the improvement in intrinsic ADC resolution when increasing the number of bits.

2.2.4 Multi-Stage Noise-Shaping (MASH)

In the previous sections an overview of the main optimization opportunities of a delta-sigma modulator was given. The key parameters are the filter order, number of ADC bits and oversampling ratio. The degrees of freedom in this design space are more than adequate to design a high-resolution delta-sigma ADC with low to medium bandwidth. Recently published delta-sigma designs however demonstrate a trend towards much higher bandwidths, far exceeding 100 MHz which is being pushed by new wireless standards. On the architectural level the design parameters of the delta-sigma modulator are constrained to practical limitations [3]. As a delta-sigma modulator is a feedback system, the loop stability requirements put constraints on the maximum number of ADC bits, the maximum sampling frequency and hence the oversampling ratio and the maximum loopfilter order. This is explained in more detail in Sects. 2.3 and 2.4.

An architectural solution to break the bandwidth barrier and enable wider bandwidths at low oversampling ratios within the constraint of the maximum

sampling frequency is the cascaded or multi-stage noise-shaping (MASH) delta-sigma modulator. The MASH delta-sigma modulator originated as a solution to implement a stable higher-order modulator with multiple low-order stages [8]. The concept of a (2-1-1) MASH modulator is shown in Fig. 2.5. For simplicity, the DACs are not shown in Fig. 2.5. It consists of N (3 in this example) cascaded delta-sigma modulators where each consecutive stage digitizes the quantization error of the previous stage. This way redundancy is created in the system of the quantization errors of the first $N-1$ stages. With this redundancy, the quantization errors of the first $N-1$ stages can ideally be cancelled in the digital domain and what remains is the quantization error of the N^{th} stage which is shaped by the NTFs of all stages combined. As an example, consider the output of the first (2nd-order) delta-sigma modulator stage of Fig. 2.5. The output y_1 contains the input signal x with two delays and the quantization noise q_1 shaped by a second-order NTF. The quantization error q_1 is extracted from the first stage by subtracting the ADC1 input and ADC1 output (DAC omitted) and fed through interstage gain g_1 to the input of the second (first-order) delta-sigma stage. The output bitstream y_2 of the second stage contains the amplified quantization noise $g_1 \cdot q_1$ with one delay and the quantization error q_2 of ADC2 shaped with a first-order NTF. Both outputs y_1 and y_2 contain q_1 , but with different transfer functions. The transfers of q_1 can be equalized by delaying y_1 with one clock period while filtering y_2 with the NTF of stage 1 and dividing by interstage gain g_1 . After subtraction, the combined output y_{12} does not contain quantization error q_1 . A similar analysis can be done for q_2 and the third stage of the MASH modulator. The overall output y does not contain q_1 and q_2 while the quantization error q_3 of ADC3 is filtered with a 4th-order NTF and suppressed by interstage gains g_1 and g_2 combined. As the overall 4th-order NTF is a combination of low-order (1st and 2nd) NTFs, it provides better quantization noise suppression compared to the NTF of a single-stage 4th-order delta-sigma modulator. In addition to that, the application of interstage gains (g_i) between the stages can further suppress the quantization error. Figure 2.6 compares the NTF of a 2nd order delta-sigma modulator with a 2-1 and 2-1-1 MASH.

The effectiveness of the digital noise cancellation is limited by the matching inaccuracy between the analog and digital filters. In practice the analog loop filters will suffer from mismatch. Therefore, the quantization noise contributions of the individual stages will not be perfectly cancelled which puts a limit on the maximum noise suppression that can be achieved. Traditionally, MASH delta-sigma modulators have been solely implemented with switched-capacitor (SC) circuits due to the fact that the coefficients of SC filters are set by capacitor ratios which have very high accuracy and match very well with the coefficients of the digital noise-cancellation filters. In [9] the feasibility of a continuous-time implementation of a MASH delta-sigma modulator has been demonstrated. Recently, the application of continuous-time MASH delta-sigma modulators has pushed the bandwidth from tens of MHz to far beyond 100 MHz [6].

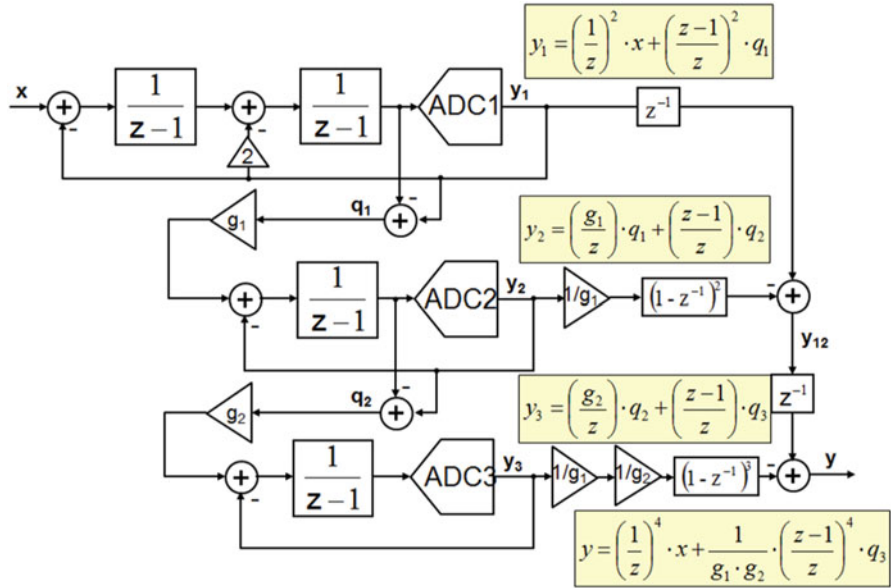


Fig. 2.5 Example of a 2-1-1 MASH delta-sigma modulator

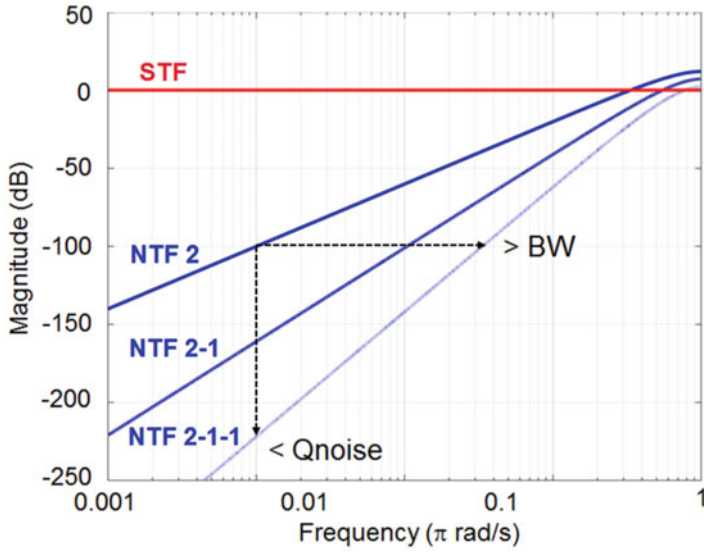


Fig. 2.6 NTFs of 2nd-order, 2-1 MASH and 2-1-1 MASH

2.3 Non-Idealities

Previously it was mentioned that the design space of a high-speed wideband delta-sigma modulator is constrained due to loop stability requirements which is related to the speed and accuracy limitations of the used technology. As an example, the ADC in the delta-sigma loop of Fig. 2.1 requires a certain amount of time to convert the analog input signal into a digital representation. This latency of the ADC is inside the feedback loop and directly impacts the stability. In particular if the ADC is clocked at a very high (GHz) frequency, the loop becomes very sensitive to latency. Another aspect of loop stability is for example related to the parasitic loading of the loopfilter output with the ADC input capacitance. In high-speed wideband delta-sigma modulators, typically low-latency multi-bit flash ADCs are employed, which introduce a significant load capacitance for the loopfilter [3]. This results in an additional parasitic pole in the system that hampers stability. These and other non-idealities related to high-speed delta-sigma modulators will be discussed in the following sections.

2.3.1 Metastability

A metastability error occurs if the ADC does not have enough time to generate a fully settled digital output for a certain input signal. Usually the digital decision is made by means of a regenerative latch with a positive feedback loop. Due to the exponential behavior of the latch, the delay of the latch becomes large for example in case of a very small latch input signal or an input signal with certain dynamics [10]. In case of insufficient gain, the metastable output state of the ADC will propagate through the feedback loop to the DAC and will result in an incomplete DAC feedback charge. The impact of metastability can be easily verified when modelling the ADC in the delta-sigma loop (Fig. 2.1) with finite quantizer gain, while the metastable output y of the delta-sigma modulator is converted into an ideal digital signal by an ideal digitizer with infinitely large gain. Figure 2.7 shows two simulated output spectra in case of infinite quantizer gain (blue) and a finite quantizer gain of 80 dB. The red spectrum shows a flat highly elevated noise floor in the low-frequency band that degrades the maximum resolution that can be achieved.

There are two approaches to reduce the probability of metastable errors. Either the amount of gain within the ADC time budget must be increased by e.g. decreasing the time constant of the regenerative latch, or the time budget for the ADC should be increased. Improving the time constant is a delicate task and can be realized by e.g. increasing the bias current or reducing the capacitive load of the latch. Increasing the time budget leads to larger latency that impacts the stability of the loop. A dedicated excess loop delay compensation loop can allow for more delay while maintaining stable operation of the modulator loop which is described next.

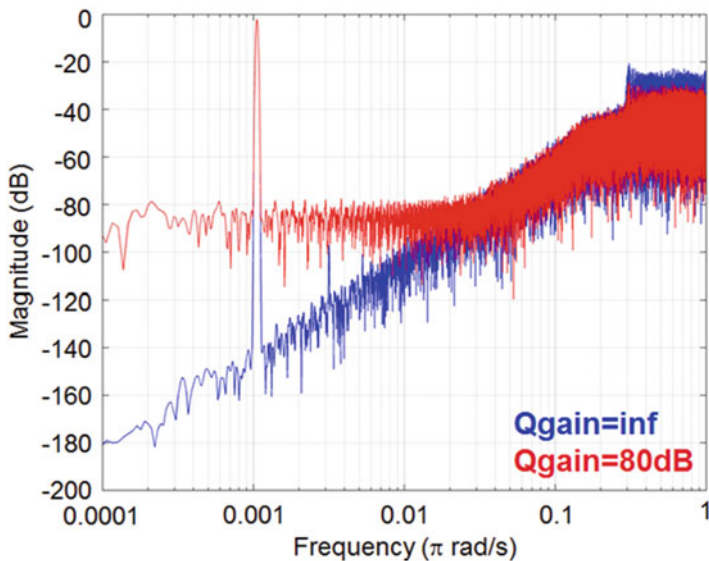


Fig. 2.7 Simulated output spectra of a 1-bit delta-sigma modulator with infinite quantizer gain (blue) and with finite quantizer gain of 80 dB (red)

2.3.2 Excess Loop Delay (ELD)

Metastability and excess loop delay are tightly coupled as the metastability probability requirement dictates the ADC time budget for a given latch time constant. Other delay contributions origin from e.g. propagation delays of digital circuitry and DACs inside the delta-sigma feedback loop. An ELD compensation loop [11] can allow for a clock period delay without compromising stability or the shape of the NTF. The concept of the ELD loop is shown in Fig. 2.8. In this example the quantizer latency is modelled as a clock period delay. An additional feedback path d around the quantizer delay stabilizes the loop in the presence of the extra delay and the NTF can be mapped to the ideal second-order NTF (in the example of Fig. 2.8 the NTF mapping is achieved for coefficients $a_1 = 1$, $a_2 = 3$ and $d = 2$). ELD compensation is widely used in high-speed wideband delta-sigma modulators. Excess phase, e.g. due to a parasitic pole at the output of the loopfilter as a result of the ADC input capacitance, can be compensated in a similar way.

2.3.3 Non-Linearity

The focus has been so far on the (quantization) noise aspects of the delta-sigma modulator. Besides noise, distortion is another critical performance parameter of

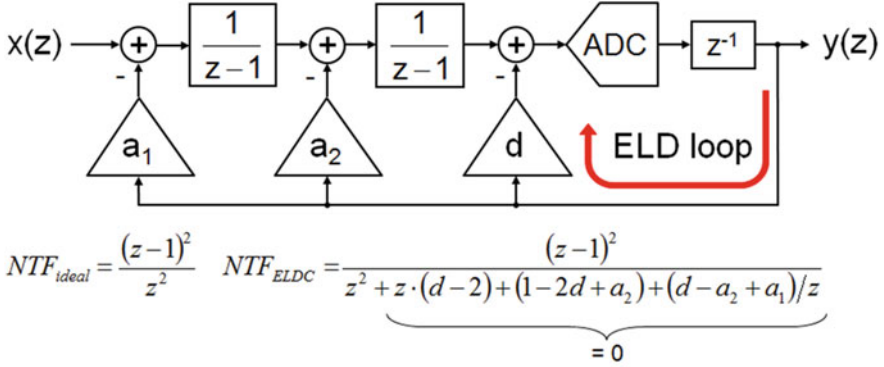


Fig. 2.8 Second-order delta-sigma modulator with one period ELD compensation

the ADC. Due to non-linearity, distortion components at harmonic frequencies can occur as well as an increased noise level in case of large input signals. A dominant contributor to distortion is typically the feedback DAC. As mentioned before, many wideband delta-sigma modulators incorporate multi-bit ADCs and multi-bit feedback DACs. Due to the low number of bits, the DACs are usually implemented as a thermometer DAC with e.g. unit current sources. Due to mismatch between the unit current sources, distortion components at even and odd harmonic frequencies will occur and high frequency quantization noise will leak in the low-frequency signal band via intermodulation distortion (Fig. 2.9). It is not uncommon that the peak signal-to-noise-and-distortion ratio (SNDR) of a wideband multi-bit delta-sigma modulators drops 5–10 dB relative to the dynamic range (DR) due to non-linearity effects. For some applications this may be ok but for e.g. multi-channel receivers (a typical application for high-resolution wideband ADCs) such a loss is unacceptable, as the presence of a strong in-band blocker signal leads to desensitization of the receiver for weak wanted signals. Besides static mismatch errors, also dynamic errors like intersymbol interference (ISI) will degrade the performance of the delta-sigma modulator. In literature, many techniques have been reported to improve the static errors of a multi-bit DAC via analog calibration [12], digital post correction [13–15], dynamic element matching algorithms such as data weighted averaging (DWA) [16–21] as well as static errors like ISI [22] via return-to-zero (RTZ) coding, ISI shaping [23], etc.

2.3.4 Phase Noise

For continuous-time delta-sigma modulators the purity of the sampling clock is very important. This is due to the fact that the amount of feedback current from the DAC during a clock period is directly depending on the clock timing. Noise on

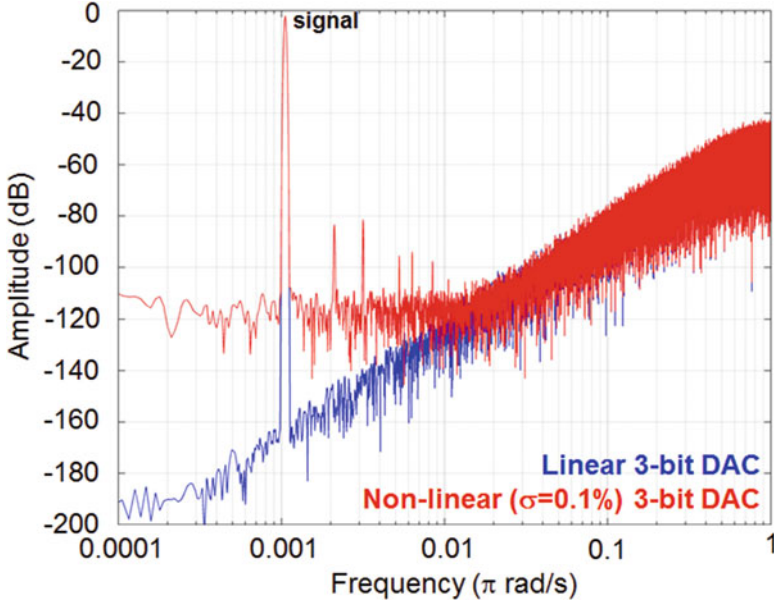


Fig. 2.9 Simulated output spectra of a 3-bit delta-sigma modulator with a linear DAC (*blue*) and 0.1 % mismatch DAC (*red*)

the clock edges directly reflects into noise injection at the input of the modulator. The wideband phase noise of the clock leaks into the signal band via reciprocal mixing with the OOB quantization noise. This is in particular a limitation in 1-bit delta-sigma modulators that have high OOB quantization noise. For multi-bit DACs the OOB noise is lower which relaxes the far-off phase noise requirements. An effective solution to mitigate the effect of reciprocal mixing is to filter the DAC signal with a finite impulse response (FIR) filter [24] to reduce the OOB quantization noise. Mismatch between the FIRDAC coefficients results in a slightly altered filter transfer but does not introduce non-linearity. However, a FIRDAC can introduce significant delay in the feedback path which needs to be compensated to maintain loop stability [1].

2.4 High-Resolution Wideband Delta-Sigma Modulator Designs

In this paragraph some implementation examples are described that have pushed the envelope for wideband delta-sigma modulators with respect to architecture, bandwidth and linearity. The first section presents an implementation of a

continuous-time MASH delta-sigma modulator. The second example is a GHz rate modulator with >100 MHz bandwidth. The last design demonstrates a high-resolution wideband delta-sigma modulator that realizes <-100 dB in 25 MHz bandwidth.

2.4.1 A Continuous-Time MASH Delta-Sigma ADC

In [9] a first implementation of a continuous-time 2-2 MASH delta-sigma modulator has demonstrated 67 dB DR in 10 MHz at an oversampling ratio of only $8\times$. A quadrature configuration of the 2-2 MASH was presented in [25]. The design of the quadrature 2-2 MASH is shown in Fig. 2.10. The ADC consists of two different channels to handle complex in-phase (I) and quadrature phase (Q) signals. The loopfilter of each delta-sigma stage consists of two RC integrator stages (e.g. R1C1, R2C2 in the top left corner) with a feedforward capacitor (e.g. Cff1) for loop stabilization. The 2nd-order loopfilters of the quadrature sigma-delta stages have complex cross-coupling resistors (e.g. Rfb1, Rfb2). Depending on the sign of the cross-coupling connections the NTF zeros can be freely distributed either in the positive or negative frequency band. All resistors in the loopfilters can be calibrated with 1 % accuracy to match the analog loopfilter to the digital noise cancellation filters (not shown). The delta-sigma modulators incorporate 4-bit flash quantizers with offset calibration and 4-bit SC feedback DACs. The quantization errors of the first quadrature sigma-delta stages are duplicated by means of resistors R3 and DAC2 that are connected to the input virtual ground nodes of the second quadrature stages. The topology of the second quadrature stages is identical to the first. Figure 2.11 shows the measured complex quantization noise spectrum of the quadrature 2-2 MASH. All NTF zeros are positioned in the positive frequency band from 0.5 to 20.5 MHz. In this measurement, a -1 MHz image tone has been applied to the input. The image leakage appears at +1 MHz and is 58 dB down. The quantization noise at the edge of the image band at -20 MHz is about 40 dB higher than the in-band noise between 0.5 and 20.5 MHz. The quadrature 2-2 MASH realized 77 dB DR and 69 dB peak SNDR in 20 MHz zero-IF (0.5–20.5 MHz) bandwidth at a sampling frequency of 340 MHz and 56 mW power consumption from a 1.2 V supply (90 nm CMOS). Recent publications of wideband continuous-time MASH delta-sigma architectures have demonstrated 85 dB DR/74.6 dB SNDR in 50 MHz (3-1 MASH) [5], 90 dB DR/72.6 dB SNDR in 53 MHz (0-3 MASH) [2] and 67 dB DR/64.7 dB SNDR in 465 MHz (1-2 MASH) [6].

2.4.2 A 4 GHz CT Delta-Sigma ADC with 125 MHz Bandwidth

In this section, a 4 GHz rate continuous-time delta sigma ($CT\Sigma\Delta$) ADC is presented [3]. The ADC achieves 70 dB dynamic range and -74 dBFS total harmonic

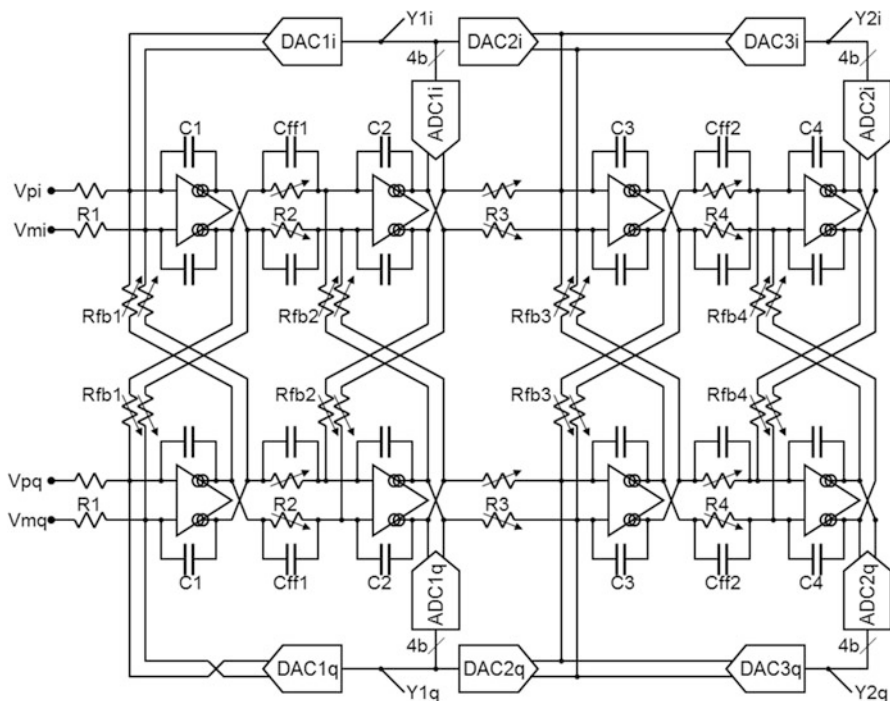


Fig. 2.10 Continuous-time quadrature 2-2 MASH

distortion (THD) in 125 MHz. Such large bandwidth and high linearity is achieved by employing a high-speed loop filter topology, in combination with a low latency 4-bit Quantizer and DAC architecture.

Figure 2.12 shows the block level diagram of the high-speed CT $\Sigma\Delta$ modulator, which uses a capacitive feedforward loopfilter architecture. A feedforward loopfilter architecture requires a summation node for its feedforward coefficients. The summation node should not introduce additional ELD. A summation node can be implemented by using an active summing amplifier. When the modulator is clocked at GHz sampling rates, the limited gain-bandwidth product of the summing amplifier limits the SQNR performance of the modulator. The limited gain of the summing amplifier acts as a fixed attenuation in the delta-sigma loop and reduces the effective gain of the loop filter. Moreover, the limited BW of the summing amplifier acts as an additional pole in the loop and degrades the phase margin of the loop filter. For a design targeting 4 GHz sampling rate, an active feedforward summation node requires an amplifier with a gain-bandwidth product in excess of 20 GHz [26]. In addition to its limited GBW, the summation amplifier needs to drive a multi-bit quantizer, which further increases the GBW requirement of the amplifier. Therefore, the summing amplifier is one of the major bottlenecks that limits the maximum sampling speed of the modulator.

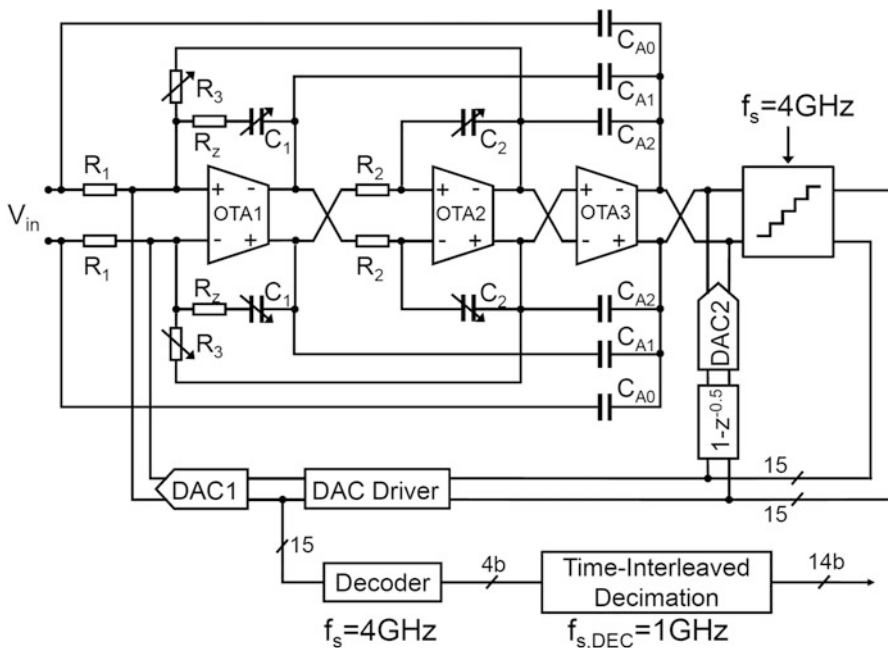


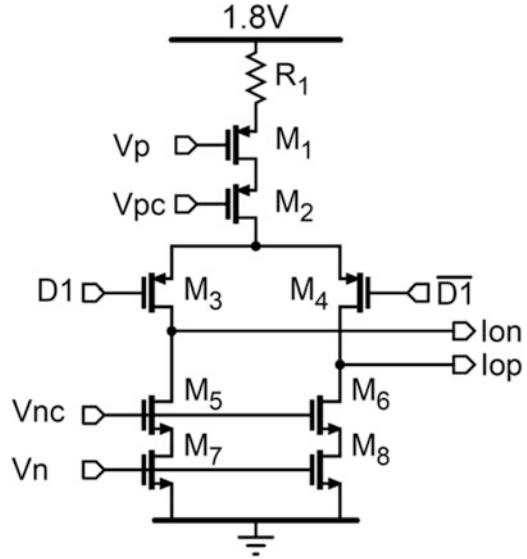
Fig. 2.13 Measured spectra with a 0.85 V@2.5 MHz and 0.85 V@7.67 MHz signal

integrates a digital differentiator [27]. Furthermore, an overall feed-forward path is implemented by CA0 to relax the requirements on the loop filter's linearity [28] and to reduce the peaking in the signal transfer function of the modulator at the cost of lower anti-alias filtering.

In Fig. 2.13 shows the top level architecture of the 3rd order CTΣΔ modulator. The first two integrators are implemented as RC integrators since they can meet the linearity requirement of -70 dBFS THD. Moreover, the zero introduced due to the limited transconductance (g_m) of the first integrator, a resistor ($R_z = 1/g_m$) in series with the integration capacitor (C_1) is employed. The first two operational-transconductance-amplifiers (OTAs) are implemented as two-stage amplifiers with feedforward frequency compensation [29]. The last integrator is a $g_m C$ integrator since it has relaxed linearity requirements. It is implemented as a resistively degenerated folded-cascode amplifier. Since, the modulator uses a capacitive feedforward architecture, the last OTA is not in the speed critical path thus relaxing its gain-bandwidth requirements. The power dissipation of the last integrator is negligible compared to first two integrators.

To compensate RC spread, the capacitors C1&C2, and resistor R3 can be separately adjusted via five-bit networks. The tuning range covers 0.5-2 \times of the nominal RC time constant. In order to reduce calibration overhead, the nominal bias current of the gmC integrator can also be varied 0.5-2 \times to calibrate the pole frequency of the third integrator of the loopfilter ($\omega_3 \propto \text{gm}$). The feedforward

Fig. 2.14 Schematic of a unit element of 4-bit DAC1



coefficients of the loopfilter are fixed by the ratios of the capacitors (CA1 and CA2). The quantizer is implemented as a 4-bit flash ADC. To meet the stability requirement of the modulator, the quantizer should generate a valid signal in less than one clock period. In this design, we have allocated half a sampling-clock period (125 ps) to meet the stability requirements. The remaining half of the sampling period is reserved for propagation of signals and re-clocking of DAC input signals.

DAC1 is a 4-bit current-steering DAC designed for 11-bit intrinsic matching. Achieving this with MOS current sources consumes too much area and results in poor high-frequency linearity. Figure 2.14 shows one-unit element of DAC1. Therefore, DAC1 uses resistively degenerated PMOS current sources. By using a higher supply voltage for DAC1 (1.8 V), R_1 can be made larger, effectively reducing the noise contribution of DAC1 and reducing the ADC's overall power consumption. Since the voltage drop on R_1 is about 0.7 V, M1–8 can still be implemented using thin-oxide transistors. At high sampling rates, the unequal rise and fall time of the output of DAC1 can cause inter-symbol interference (ISI) [22, 30]. To minimize this, DAC1 employs a fully differential architecture and DAC1 driver's D-FF and switch drivers are dimensioned to achieve a signal-to-noise ratio (SQNR) of better than 80 dB.

The ADC has been fabricated in 45 nm baseline LP-CMOS and has an active area of 0.9 mm². The ADC including the decimation filter dissipates 256 mW from a 1.1 V supply and 3.2 mW from a 1.8 V supply, which is the supply voltage of the DAC1 as described before. Figure 2.15 shows an FFT of the measured-decimated output of the $\Sigma\Delta$ ADC with no input signal. The ADC's noise floor¹ is flat in the

¹The noise floor is the average of four measurements.

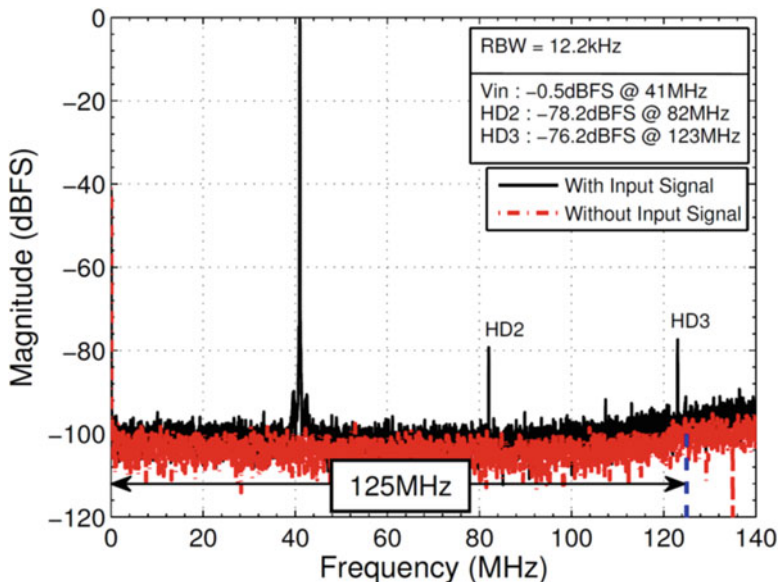


Fig. 2.15 FFT of measured output for an input signal of -0.5 dBFS at 41 MHz

signal BW of 125 MHz and rises slightly at higher frequencies due to the presence of out-of-band quantization noise. To measure the ADC's distortion, sinusoidal input signals with a maximum input voltage of $2.0\text{V}_p - p$ differential were supplied to the ADC. The decimated output for a 41 MHz input signal at -0.5 dBFS has been captured in real-time; its FFT is shown in Fig. 2.15. The THD is -74 dBFS.

2.4.3 A 25 MHz BW CT Delta-Sigma ADC with <-100 dB THD

In [7] a continuous-time delta-sigma ADC is presented that achieves <-100 dB THD and 77 dB SNDR in 25 MHz bandwidth. The modulator comprises of a 1-bit feedback DAC, which is highly insensitive to process spread and mismatch, and a wideband high precision voltage regulator to mitigate dynamic errors of the 1-bit DAC.

Figure 2.16 shows the model block diagram of the delta-sigma ADC. It has a 4th-order loopfilter with two resonance filters ($\omega_1/s - \omega_2/s - d_1$ and $\omega_3/s - \omega_4/s - d_2$), two internal feedforward paths (c_2 and c_3), a signal feedforward path (c_1) and three 1-bit feedback DACs. The main feedback DAC (DAC1) and the reference circuit are critical for the linearity of the ADC. Although theoretically a 1-bit DAC is inherently linear, any signal- or data-dependent residue on the DAC reference voltage will lead to distortion, spurious tones and increased in-band noise. To achieve the noise and

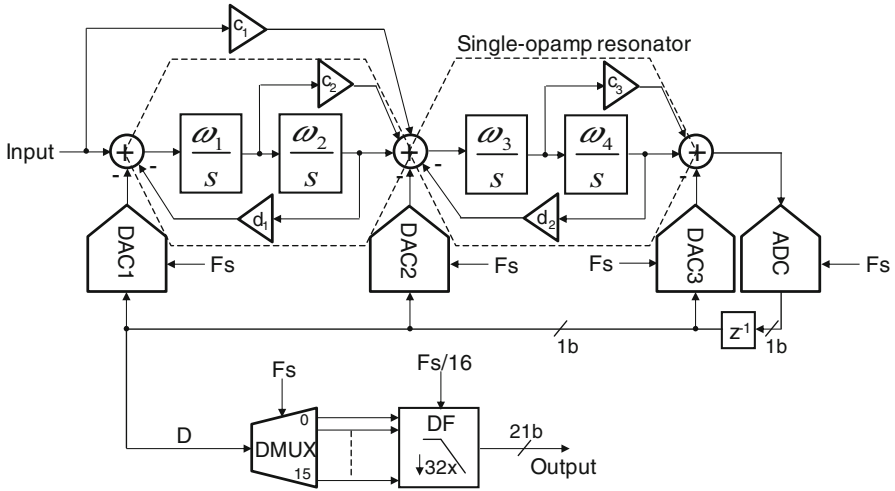


Fig. 2.16 Block diagram of the 4th-order delta-sigma ADC

distortion performance a resistive return-to-open DAC is used. During open state the data dependent charge in the parasitic capacitance at the switch side of the DAC resistor must be sufficiently discharged via the DAC resistor to the loopfilter virtual ground nodes to avoid distortion due to memory effects. The loopfilter model is mapped to a cascaded implementation of two single-opamp resonators [28, 31]. The resonator filter implementation has an inherent zero. Therefore, no additional summing amplifiers are needed which saves power as only two amplifiers are used to implement the complete 4th-order loopfilter. The pseudo differential amplifier consists of three inverter stages with Miller compensation. The common-mode of the amplifier input nodes is controlled via resistors by an inverter-based common-mode amplifier sensing the output common-mode. The bias current of the first resonator filter is dictated by linearity requirements and the current of the second filter by speed requirements.

The choice for a partial feedforward and feedback topology of the loopfilter is a trade-off between power, noise and minimal out-of-band (OOB) peaking of the signal transfer function (STF). STF peaking is highly undesired as it results in loss of dynamic range for OOB interferers. Signal feedforward path c_1 has been added to reduce STF peaking close to the signal band to ~ 4 dB. Because of the continuous-time loopfilter, no extra anti-alias filter is required. The 1-bit quantizer is dithered and has a local excess loop delay (ELD) compensation DAC (DAC3) to allow for one clock period delay in the feedback loops. The quantizer and DACs are clocked at 2.2 GHz and the time budget for the quantizer latch is maximized to half a clock cycle to minimize meta-stability related errors. The remaining time budget accounts for latency of buffer and retiming circuits. The 2.2 GHz 1-bit output data is de-multiplexed and fed to a decimation filter (DF) that decimates by $32\times$ and outputs 21-bit data at 68.75 MS/s.

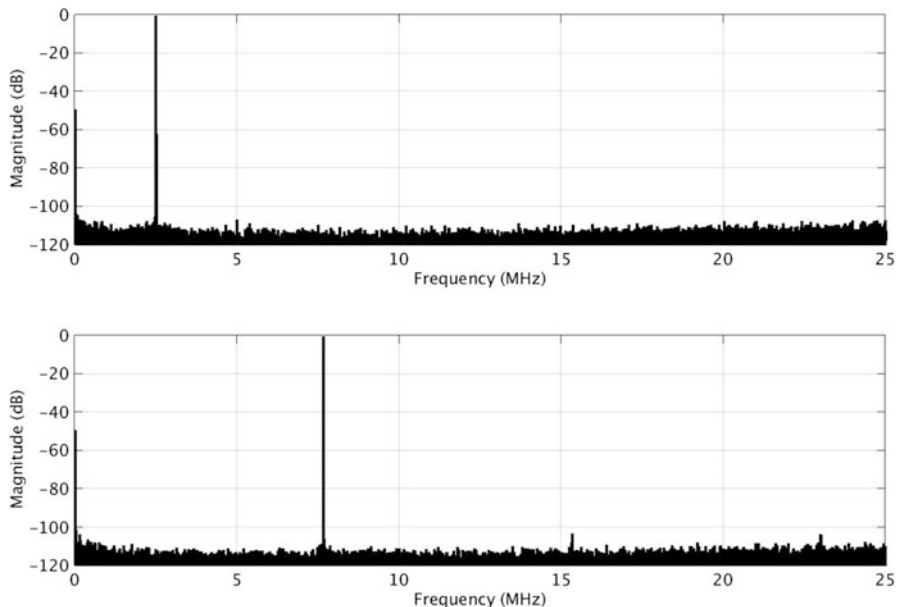


Fig. 2.17 Measured spectra with a 0.85 V@2.5 MHz and 0.85 V@7.67 MHz signal

The ADC has been fabricated in a TSMC 65 nm CMOS process. The modulator and the 1.2 V supply regulators measure 0.25 mm² and 0.35 mm² respectively. Figure 2.17 shows the output spectra (RBW 880 Hz) with 0.85 V peak differential input signals at 2.5 MHz and 7.667 MHz respectively. In both measurements HD2 and HD3 are below -100 dBc. The dynamic range and peak SNDR are 77 dB in 25 MHz bandwidth. The modulator power consumption including clock distribution is 41.4 mW.

2.5 Conclusions

This paper describes design aspects of high resolution and wideband continuous-time $\Sigma\Delta$ modulators for wireless applications. The optimal noise transfer function and the choice of architecture are the two most important design steps required to achieve the resolution in a given bandwidth. First of all, in a single loop delta-sigma modulator, the main design parameters are the loopfilter order, oversampling ratio and the accuracy of the ADC and DAC. Since a delta-sigma modulator is a feedback system, the loop stability requirements limit the maximum sampling rate in practical implementations, thus the bandwidth of the modulator. In that case, multi-stage noise-shaping (MASH) delta-sigma modulator architecture enables wider bandwidth by eliminating the maximum sampling rate limitation.

The design space of single-loop and MASH delta-sigma modulator architectures is limited by speed and accuracy limitations of the available process technologies. Recently published delta-sigma modulators are clocked at GHz sampling rates, the non-idealities associated with the internal ADC and DAC of the modulator limit their performance. Metastability and ELD limit the maximum sampling rate, whereas the non-linearity and phase noise of the sampling clock limit the achievable dynamic range.

Three implementations of CT delta-sigma modulators are presented which advanced the state-of-the-art envelope in terms of architecture, bandwidth and linearity. The first implementation introduced a continuous-time 2-2 MASH delta-sigma modulator architecture which achieves 77 dB DR in 20 MHz and 56 mW power consumption. The second implementation pushed the sampling speed of single loop delta-sigma modulators to 4 GHz by employing a high-speed capacitive feedforward loop filter architecture and achieved the 70 dB DR in 125 MHz. The third implementation achieves <-100 dB THD and 77 dB SNDR in 25 MHz bandwidth. Such high linearity is enabled using a 1-bit feedback DAC and integrated high precision voltage regulator.

References

1. P. Shettigar, S. Pavan, A 15mW 3.6GS/s CT- $\Sigma\Delta$ ADC with 36MHz bandwidth and 83dB DR in 90nm CMOS. *ISSCC Digest of Technical Papers*, pp. 156–157, Feb 2012
2. Y. Dong, R. Schreier, W. Yang, S. Korrapati, A. Sheikholeslami, A 235mW CT 0-3 MASH ADC achieving -167dBFS/Hz NSD with 53MHz BW. *ISSCC Digest of Technical Papers*, pp. 480–481, Feb 2014
3. M. Bolatkale, L.J. Breems, R. Rutten, K. Makinwa, A 4GHz CT $\Sigma\Delta$ ADC with 70dB DR and -74dBFS THD in 125MHz BW. *ISSCC Digest of Technical Papers*, pp. 470–471, Feb 2011
4. H. Shibata, R. Schreier, W. Yang, A. Shaikh, D. Paterson, T. Caldwell, D. Alldred, P.W. Lai, A DC-to-1GHz tunable RF $\Sigma\Delta$ ADC achieving DR=74dB and BW=150MHz at $f_0=450$ MHz using 550mW. *ISSCC Digest of Technical Papers*, pp. 150–151, Feb 2012
5. D. Yoon, S. Ho, H. Lee, An 85dB-DR 74.6dB-SNDR 50MHz-BW CT MASH $\Sigma\Delta$ Modulator in 28nm CMOS. *ISSCC Digest of Technical Papers*, pp. 272–273, Feb. 2015
6. Y. Dong, J. Zhao, W. Yang, T. Caldwell, H. Shibata, R. Schreier, Q. Meng, J. Silva, D. Paterson, J. Gealow, A 930mW 69dB-DR 465MHz-BW CT 1-2 MASH ADC in 28nm CMOS. *ISSCC Digest of Technical Papers*, pp. 278–279, Feb 2016
7. L. Breems, M. Bolatkale, H. Brekelmans, S. Bajoria, J. Niehof, R. Rutten, B. Oude-Essink, F. Fritschij, J. Singh, G. Lassche, A 2.2GHz continuous-time $\Sigma\Delta$ ADC with -102dBc THD and 25MHz BW. *ISSCC Digest of Technical Papers*, pp. 272–273, Feb 2016
8. Y. Matsuya, K. Uchimura, A. Iwata, T. Kobayashi, M. Ishikawa, T. Yoshitome, A 16-bit oversampling A-to-D conversion technology using triple-integration noise-shaping. *IEEE J. Solid-State Circuits*, **22**(6), 921–929 (1987)
9. L. Breems, A cascaded continuous-time $\Sigma\Delta$ modulator with 67dB dynamic range in 10MHz bandwidth. *ISSCC Digest of Technical Papers*, pp. 72–73, Feb 2005
10. J. Cherry, W. Snelgrove, Clock jitter and quantizer metastability in continuous-time delta-sigma modulators. *IEEE Trans. Circuits Syst. II* **46**, 661–676 (1999)
11. P. Benabes, M. Keramat, R. Kielbasa, A methodology for designing continuous-time sigma-delta modulators, in *Proceedings of European Design and Test Conference, ED TC'97*, pp. 46–50, Mar 1997

12. P. Witte, J. Kauffman, J. Becker, Y. Manoli, M. Ortmanns, A 72 dB-DR CT $\Sigma\Delta$ modulator using digitally estimated auxiliary DAC linearization achieving 88 fJ/conv in a 25 MHz BW. *ISSCC Digest of Technical Papers*, 2012, pp. 154–156, 2012
13. J. Kauffman, P. Witte, J. Becker, M. Ortmanns, An 8.5 mW continuous-time $\Sigma\Delta$ modulator with 25 MHz bandwidth using digital background DAC linearization to achieve 63.5 dB SNDR and 81 dB SFDR. *IEEE J. Solid State Circuits* **46**(12), 2869–2881 (2011)
14. Y.-S. Shu, J.-Y. Tsai, P. Chen, T.-Y. Lo, P.-C. Chiu, A28 fJ/convstep CT delta sigma modulator with 78 dB DR and 18 MHz BW in 28 nm CMOS using a highly digital multibit quantizer. *ISSCC Digest of Technical Papers*, pp. 268–269, 2013
15. T. Cataltepe et al., Digitally corrected multi-bit $\Sigma\Delta$ data converters. *ISCAS*, pp. 647–650, May 1989
16. M.J. Story, Digital to analogue converter adapted to select input sources based on a preselected algorithm once per cycle of a sampling signal. U.S. Patent 5 138 317, 11 Aug 1992
17. B.H. Leung, S. Suturja, Multi-bit sigma-delta A/D converter incorporating a novel class of dynamic element matching techniques. *IEEE Trans. Circuits Syst. II* **39**, 35–51 (1992)
18. R. Schreier, B. Zhang, Noise-shaped multi-bit D/A converter employing unit elements. *Electron. Lett.* **31**(20), 1712–1713 (1995)
19. R.T. Baird, T. Fiez, Linearity enhancement of multi-bit $\Sigma\Delta$ A/D and D/A converters using data weighted averaging. *IEEE Trans. Circuits Syst. II* **42**, 753–762 (1995)
20. T. Kwan, R. Adams, R. Libert, A stereo multi-bit $\Sigma\Delta$ D/A with asynchronous master-clock interface. *ISSCC Digest of Technical Papers*, vol. 39, Feb 1996, pp. 226–227
21. I. Galton, Spectral shaping of circuit errors in digital-to-analog converters. *IEEE Trans. Circuits Syst. II* **44**(10), 808–817 (1997)
22. R.W. Adams, Design and implementation of an audio 18-bit analog-to-digital converter using oversampling techniques. *J. Audio Eng. Soc.* **34**(3), 153–166 (1986)
23. L. Risbo, R. Hezar, B. Kelleci, H. Kiper, M. Fares, A 108 dB DR, 120 dB THD and 0.5 Vrms output audio DAC with intersymbol interference shaping algorithm in 45 nm. *ISSCC Digest of Technical Papers*, pp. 484–485, 2011
24. B. Putter, $\Sigma\Delta$ ADC with finite impulse response feedback DAC. *ISSCC Digest of Technical Papers*, pp. 76–77, Feb 2004
25. L. Breems, R. Rutten, R.H.M. van Veldhoven, G. van der Weide, A 56mW continuous-time quadrature cascaded $\Sigma\Delta$ modulator with 77dB DR in a near zero-IF 20MHz band. *IEEE J. Solid-State Circuits*, pp. 2696–2705, Dec 2012
26. M. Bolatkale, L. Breems, K. Makinwa, *High Speed and Wide Bandwidth Delta-Sigma ADCs* (Springer, Dordrecht, 2014)
27. G. Mitteregger et al., A 20-mW 640-MHz CMOS continuous-time ADC With 20 MHz signal bandwidth, 80-dB dynamic range and 12-bit ENOB. *IEEE J. Solid State Circuits* **41**(12), 2641–2649 (2006)
28. H. Chae, J. Jeong, G. Manganaro, M. Flynn, A 12mW low-power continuous-time bandpass $\Sigma\Delta$ modulator with 58dB SNDR and 24MHz bandwidth at 200MHz IF. *ISSCC Digest of Technical Papers*, pp. 148–149, 2012
29. J. Silva, U. Moon, J. Steensgaard, G. Temes, Wideband low distortion delta-sigma ADC topology. *Electron. Lett.* **37**(12), 737–738 (2001)
30. E. van der Zwan, E. Dijkmans, A 0.2-mW CMOS $\Sigma\Delta$ modulator for speech coding with 80 dB dynamic range. *IEEE J. Solid State Circuits* **31**(12), 1873–1880 (1996)
31. S. Zeller et al., A 9th-order continuous time $\Sigma\Delta$ -ADC with X-coupled differential single-opamp resonators *MWSCAS*, pp. 1–4, Aug 2011

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