

Preface

Over the past few decades, very large scale integration technologies have been widely improved, allowing the proliferation of consumer electronics and enabling the steady growth of the integrated circuit (IC) market to an estimated value of over \$350 billion in 2016. The steady increase in performance of ICs in the recent past has been mostly supported by an exponential growth in the density of transistors while inversely reducing the transistors' cost, as described by Moore's law. Even though it is still valid today, its end, as such an exponential law "can't continue forever" was already preconized by Moore itself, and is pushing for new technological advancements outside complementary metal-oxide-semiconductor (CMOS) IC design. In the meanwhile, telecommunications, medical, and multimedia applications extensively use of electronic devices where blocks of analog and mixed-signal (AMS), digital processors and memory blocks are integrated together. While AMS components in these system-on-a-chip (SoC) designs usually occupy approximately 20 % of the die area, the design effort and respective design costs are considerably higher in comparison to their digital counterpart. In this context, the lack of mature automation tools for analog design has its share of blame in this SoC design paradigm.

Generally the complexity in the design of analog circuits is not due to the number of devices, but from their sensitivity to noise and the countless interactions between them, e.g., parasitic disturbances, crosstalk, substrate noise, thermal noise, etc. Plus, for smaller technology nodes with the increasing complexity of design rules and physical effects, the impact of these interactions is even greater. Despite the algorithms and techniques introduced in the last 25 years, analog IC design automation tools still strive to keep up with the new challenges created by technological evolution. Therefore, designers' exploration of the solution space keeps on being mostly manual, and their knowledge and experience crucial in making effective decisions at all stages of the analog design flow, creating additional risks and elongating the time needed to complete the design. On the other hand, in the digital IC design realm several mature electronic design automation (EDA) tools and design methodologies are available, pushing the design productivity forward.

Currently most of the low-level phases of the process are automated that help the designers keeping up with the new capabilities offered by the technology and making design reuse the commonplace. Since this difference in the level of automation becomes critical when digital and analog circuits are integrated together, the rising of efficient and state-of-the-art tools to boost analog designers' productivity is an intensive research topic in both academia and industry.

The work presented in this book belongs to the scientific area of electronic design automation and addresses automatic sizing of analog ICs. The developed multi-objective design methodology for automatic analog IC sizing was implemented in the tool AIDA-C. In AIDA-C, the usage of state-of-the-art multi-objective multi-constraint optimization engines enables the exploration of circuit design trade-offs. Process variation effects on circuit's performance are accounted with user-defined worst-case corners, and circuit's performance evaluation is done with industrial circuit simulators, e.g., Mentor Graphics' ELDO[®], Synopsys' HSPICE[®], or Cadence's Spectre[®], ensuring that the developed automatic circuit sizing is compliant with the accuracy requirements of analog designers. In addition, layout effects are included in the sizing-flow to decrease the number of independent sizing and layout iterations required to obtain a post-layout correct design. To further enhance AIDA-C, a model for first-order interactions between design variables and circuit performance, the Gradient Model, derived using machine learning techniques, is used to guide and accelerate the optimization process. The proposed approach was validated with both classical and new analog circuit structures for a several design processes, i.e., 130-nanometer, 180-nanometer, and 350-nanometer design kits, showing its validity and generality.

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This book is organized in eight chapters.

Chapter 1 presents a brief introduction to analog IC design automation, with special emphasis to automatic circuit sizing and optimization taking into account layout effects and random variations. The motivation to address automatic analog IC design is given, then, a well-accepted design flow for analog ICs that is the starting point for the methodology proposed in this book is described.

Chapter 2 presents a study of the available tools for analog design automation, overviewing state-of-the-art sizing optimization, robust design and layout-driven approaches. Valuable information can be gathered from them, such as algorithms and evaluation methods.

Chapter 3 introduces the developed automatic flow for analog IC design and particularly the general description of the developed methodology providing more detail about the inputs and interfaces of AIDA-C.

Chapter 4 describes the multi-objective optimization techniques used in AIDA-C, addressing the non-dominated sorting genetic algorithm II (NSGA-II), multi-objective simulated annealing (MOSA) and multi-objective particle swarm optimization (MOPSO) algorithms. The enhancements made by using machine learning techniques, i.e., the Gradient model, are also explored.

Chapter 5 studies the results obtained with the proposed IC sizing approach with different parameters for the optimization kernel, the impact of considering nominal or worst-case conditions in the evaluation of the circuits, and also, the advantages of enhancing the optimization kernels with the gradient model. Also, two amplifiers and an oscillator are used to compare the performance of the three optimization kernels (NSGA-II, MOSA MOPSO).

Chapter 6 presents two new methodologies to include layout effects in the sizing optimization loop: the floorplan-aware approach, which is a method to include layout's geometric properties in the optimization with negligible impact in the performance; and the layout-aware approach that accounts for the parasitic effects.

Chapter 7 presents the results obtained with the proposed analog layout-aware sizing approach, by considering the circuit's floorplan and layout induced parasitics. The efficiency of the methodology is proved in the successful design and area improvement of four design cases: a single-stage folded cascode amplifier with bias, a single-stage amplifier with gain enhancement using voltage combiners, a two-stage Miller amplifier, and a two-stage folded cascode amplifier, for a 130-nanometer design process.

In Chap. 8, the closing remarks and future directions for the continuous development of AIDA-C are outlined.

Lisbon, Portugal

Nuno Lourenço
Ricardo Martins
Nuno Horta

Automatic Analog IC Sizing and Optimization

Constrained with PVT Corners and Layout Effects

Lourenço, N.; VAT PT502854200, I. de T.; Gomes Horta,
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