Preface

The strong interaction between *Electronic Design Automation* (EDA) tools and *Complementary Metal-Oxide Semiconductor* (CMOS) technology contributed substantially to the advancement of modern digital electronics. The continuous downscaling of CMOS *Field Effect Transistor* (FET) dimensions enabled the semiconductor industry to fabricate digital systems with higher circuit density at reduced costs. To keep pace with technology, EDA tools are challenged to handle both digital designs with growing functionality and device models of increasing complexity. Nevertheless, while the downscaling of CMOS technology requires more complex physical design models, the logic abstraction of a transistor as a switch has not changed even with the introduction of 3D FinFET technology. As a consequence, modern EDA tools are fine-tuned for CMOS technology and the underlying design methodologies are based on CMOS logic primitives, i.e., negative unate logic functions. While it is clear that CMOS logic primitives will be the ultimate building blocks for digital systems in the next 10 years, no evidence is provided that CMOS logic primitives are also the optimal basis for EDA software. In EDA, the efficiency of methods and tools is measured by different metrics such as (i) the result quality, for example the performance of an automatically synthesized digital circuit, (ii) the runtime, and (iii) the memory footprint on the host computer. With the aim to optimize these metrics, the accordance to a specific logic model is no longer important. Indeed, the key to the success of an EDA technique is the expressive power of the logic primitives' handling and solving the problem, which determines the capability to reach better metrics.

In this book, we investigate new logic primitives for electronic design automation tools.

We improve the efficiency of logic representation, manipulation, and optimization tasks by taking advantage of majority and biconditional logic primitives. We develop synthesis tools exploiting the majority and biconditional logic expressiveness. Our tools show strong results as compared to state-of-the-art academic and commercial synthesis tools. Indeed, we produce the best (public) results for many circuits in combinational benchmark suites. On top of the enhanced

synthesis power, our methods are also the natural and native logic abstraction for circuit design in emerging nanotechnologies, where majority and biconditional logic are the primitive gates for physical implementation.

We accelerate formal methods by (i) studying core properties of logic circuits and (ii) developing new frameworks for logic reasoning engines. Thanks to the majority logic representation theory, we prove nontrivial dualities for the property checking problem of logic circuits. Our findings enable sensible speedups in solving circuit satisfiability. With the aim of exploiting further the expressive power of majority logic, we develop an alternative Boolean satisfiability framework based on majority functions. We prove that the general problem is still intractable, but we show practical restrictions that instead can be solved efficiently. Finally, we focus on the important field of reversible logic where we propose a new approach to solve the equivalence checking problem. We define a new type of reversible miter over which the equivalence test is performed. Also, we represent the core checking problem in terms of biconditional logic. This enables a much more compact formulation of the problem as compared to the state of the art. Indeed, it translates into more than one order of magnitude speedup for the equivalence checking task, as compared to the state-of-the-art solution.

We argue that new approaches to solve core EDA problems are necessary, as we have reached a point in technology where keeping pace with design goals is tougher than ever.

Santa Clara, USA Luca Gaetano Amaru

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Amaru, L.G.

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