

Nanopackaging of Si(100)H Wafer for Atomic-Scale Investigations

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Abstract Ultra-high vacuum (UHV) investigations have demonstrated a successful development of atomic nanostructures. The scanning tunneling microscope (STM) provides surface study at the atomic scale. However, the surface preparation is a crucial experimental step and requires a complex protocol conducted in situ in a UHV chamber. Surface contamination, atomic roughness, and defect density must be controlled in order to ensure the reliability of advanced UHV experiments. Consequently, a packaging for nanoscale devices has been developed in a micro-electronic clean room environment enabling the particle density and contaminant concentration control. This nanopackaging solution is proposed in order to obtain a Si(001)-(2×1):H reconstructed surface. This surface is protected by a temporary silicon cap. The nanopackaging process consists in a direct bonding of two passivated silicon surfaces and is followed by a wafer dicing step into 1-cm² dies. Samples can be stored, shipped, and in situ opened without any additional treatment. A specific procedure has been developed in order to open the nanopackaged samples in a UHV debonder, mounted in the load-lock chamber of a

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low-temperature STM system (LT-STM). Statistical large scan LT-UHV-SEM images and LT-UHV-STM images have been obtained enabling the surface study at the atomic resolution.

1 Introduction

Nowadays, science cannot progress without collaboration between different partners. The particular skill provided by each research laborator or industrial member of a consortium is the key success criteria for a collaborative project. One of the limits for these collaborations is the possibility to exchange samples without degradation due to transportation. Typically, surface contamination can happen during the surface shipment between different laboratories. Indeed, impurities can be trapped by the sample due to the atmospheric air exchange such as hydrocarbons or particles with the sample surface. Consequently, a protection of a functionalized surface or an object on a surface must be carried out in order to conserve its integrity. The packaging for nanoscale device, named “nanopackaging” [1] aims at encapsulating organic or inorganic material at the nanoscale in an appropriate environment and connecting these objects. The nanopackaging field is particularly relevant for atomic-scale devices fabrication and surface atomic wires studies which the specifications concerning the surface properties must deal with the lowest roughness and smallest defect density as possible. These surface structure studies are mostly conducted using the scanning tunneling microscopy (STM) used also, for example, to measure the electronic conductance of a single molecule [2, 3] or to study the surface conductance of atomic-scale systems [4]. However, a well-atomically ordered surface, passivated with light atoms like hydrogen having a low defect density and large terraces, is now requested.

Consequently, the nanopackaging solution has been proposed and one solution is based on a silicon chip sliced from a 200-mm silicon wafer coming from the development nanotechnology clean room [5, 6]. These developments aim at both protecting and connecting an object at the nanoscale (nano-object), an intramolecular circuit, or an atomic-scale circuit.

The process must change the silicon surface in order to obtain a reconstructed Si(001)-(2×1):H surface. For this purpose, two steps need to be achieved: first, the surface large terrace preparation performed in a clean room, and second the surface modification conducted in a dedicated environment permitting the reduction of defect particles and volatiles contaminants.

The surface preparation aims at the hydrogen saturation of the silicon surface followed by a thermal treatment in order to rebuild the silicon surface [7]. Then, the nanopackaging process is performed by a direct wafer bonding of two passivated silicon surfaces [8], permitting a hermetic seal, and consequently, a surface preservation against the atmosphere. Finally, the surface-to-the-nano-object connection has been ensured by a backside connection from the nanoscale device to the macroscale characterizing tool.

STM studies are generally performed in laboratories. In this way, a 200-mm wafer dicing step has been included enabling to obtain 1-cm^2 dies. The protected surface is a determining parameter for STM applications because the temporary cap allows keeping a stable Si(001):H surface. These samples can be stored during few months out of the clean room and be opened only when the manipulation is planned. No contamination is normally coming into play during the transportation between the clean room and the laboratories. That is why, these samples are especially used for collaborative project where an exchange between different laboratories takes place. The Si(001)-(2 \times 1):H surface is particularly appreciated for ultra-high vacuum (UHV) applications because of the well-ordered SiH atoms enabling the surface atomic wire construction using the STM atom-by-atom manipulation mode [9].

These samples are debonded in a UHV opening holder, specially designed and mounted in a load-lock chamber attached to a cryogenic low-temperature STM system (LT-STM). A crucial factor in the debonding procedure is the way of mounting the sample on the holder. Therefore, a method has been developed and a reproducible opening protocol has been established. Indeed, the samples are transferred immediately after the debonding process to the LT-STM sample stage, where they are cooled down to 4 K. The reconstructed Si(001)-(2 \times 1):H surface can be characterized, and LT-UHV-STM investigations are thus able to be conducted at the atomic scale. This chapter reports a detailed study at the atomic resolution of such surface thanks to statistical large scan obtained with the last generation of LT-UHV-STM equipment.

2 Nanopackaged Chip Fabrication

2.1 *Packaging Solution for Nanoscale Objects*

The packaging solution dedicated to protect and connect an object or a circuit at the nanoscale consists in a structure based on silicon microelectronics technologies. A platform has been developed on a silicon-on-insulator (SOI) substrate including a reconstructed Si(001):H(2 \times 1) surface, dedicated to fabricate an atomic-scale device [9, 10], as depicted in Fig. 1.

This well-ordered and hydrogenated silicon surface is particularly suitable for molecule grafting or surface nanoscale device fabrication. The nano-object is protected by a silicon temporary cap providing a hermetic encapsulation thanks to a direct bonding between two silicon wafers. This structure has been developed in 200 mm wafer diameter but atomic-scale investigations are mostly conducted in samples of a few centimeters; consequently, the bonded wafers have been diced in order to obtain $10 \times 10 \text{ mm}^2$ or $10 \times 12 \text{ mm}^2$ or $10 \times 14.2 \text{ mm}^2$ chips size as requested for the STM characterization. Previously, a bevel (cf. Sect. 2.2.2) has been etched at the edge of the silicon cap in order to facilitate the cap removal.

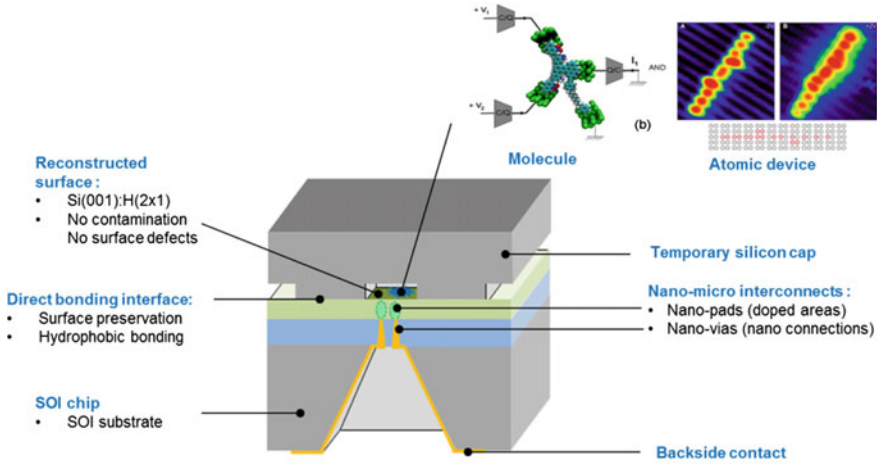


Fig. 1 The $1 \times 1 \text{ cm}^2$ chip allows to connecting a molecule or an atomic-scale device on the functionalized Si(001):H(2×1) surface. A silicon temporary cap containing a cavity provides the hermetic seal and ensures the nano-object protection. The connection from the object at the nanoscale is ensured by nano-microinterconnects toward the backside of the chip on which metal pads provide a connection to an electrical external source

As described in Fig. 1, thanks to this new kind of characterizing platform, the electrical properties of the nano-object can be studied, particularly because of the electrical connection with the backside of the chip. Indeed, the nano-object is located between the two implanted regions in the silicon layer and connected to nanovias through the box (silicon dioxide) layer of the silicon-on-insulator (SOI) substrate. The connection at the microscale is ensured by metal lines along a cavity achieved in the backside of the SOI substrate. The metal lines are extended until the backside of the chip on which metal pads are deposited providing the contact by submicronic probes for electrical studies of the nano-object.

However, this chapter is focused on the critical process module development consisting in the silicon surface improvement of the Si(001) surface damaged during the different steps of the process fabrication. A particular attention has been paid to the preparation and the packaging of this surface and especially concerning the roughness, the topology, or the particles density. These parameters must be controlled in order to preserve the surface at the atomic resolution required for a STM imaging.

2.2 Nanopackaged Chip Fabrication

The nanopackaging process is composed of elementary modules developed on a SOI substrate composed of a 400-nm-thick SiO_2 layer and 205-nm-thick

monocrystalline silicon layers. The silicon material properties have an important impact on the surface quality after surface reconstruction. In a perfectly cut wafer, an atomically flat surface will be obtained. At the opposite, wafer atomic terraces are formed when the flatness is not exactly along [110] and kinks can then be created. The misorientation angle which is less than few degrees from the (100) crystal plane is an important parameter for direct wafer bonding control [11], epitaxy models, and atomic-scale investigations. All the presented work here has been lead using a silicon (001) surface with a miscut angle ranging from 0.01° to 0.4° . Concerning the silicon doping, another important parameter not detailed more in here, the study has been conducted using P-type silicon with a resistivity of 8–10 $\Omega\cdot\text{cm}$.

The whole nanopackaging process flow can be divided in four mean technological modules as represented in Fig. 2:

Step 1–2: the first step consists in a chemical cleaning in order to remove particles and contaminants before the surface reconstruction treatment. This step is followed by surface reconstruction in a reduced pressure chemical vapor deposition reactor (RP-CVD) using hydrogen gas. It yields (2×1) reconstructed, H-terminated silicon (001) surfaces.

Steps 3–4: the protection of the last passivated reconstructed silicon surface is provided by hydrophobic direct bonding with a second reconstructed surface wafer with the same quality (temporary silicon cap). The bonded wafers are diced into 1-cm^2 samples in order to be loaded in a STM holder.

Steps 5–6: the surface of the samples is characterized and the nanopackaged chip is shipped to laboratories where the temporary cap is removed in a UHV chamber.

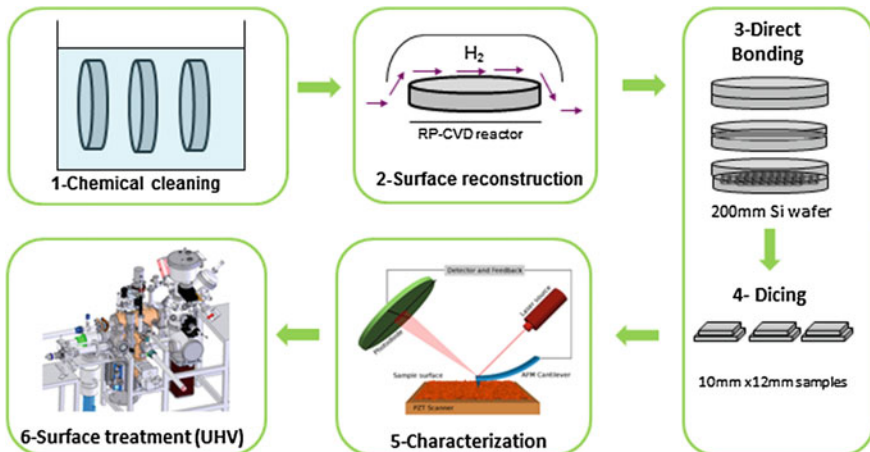


Fig. 2 Process flow description of nanopackaged SiH samples composed of a chemical cleaning, a surface reconstruction, a bonding of a silicon cap for surface preservation, and a dicing in 1-cm^2 pieces. The samples have been characterized before the shipment and a surface investigation in a UHV chamber can be started after the temporary cap removal

LT-UHV-STM investigations can thus be conducted at the atomic scale, especially in order to create a surface atomic wire.

When the electrical measurement on a nano-object is to be achieved, an optional step can be implemented consisting in its connection by the backside of a 200-mm substrate in which cavities have been etched. Two doped regions enabling the electrical continuity of the nano-object have been conducted in the SOI layer. These areas (nanopads) are connected with vias through the oxide layer of the SOI substrate at the nanoscale. These nanovias have been fabricated using a focused ion beam (FIB) which aims at etching the vias and filling using a tungsten plasma gun [12]. Finally, the interconnections between the nanovias and the backside metal pads at the submicronic scale have been obtained with tungsten lines deposited along the edge side of the cavity as illustrated at Fig. 3.

The interconnection development has been optimized with the fabrication of different matrices of 3×3 nanovias up to 7×7 nanovias with vias diameter of 100 nm, and a depth of 400 nm demonstrated that a high density of interconnections (4.106 vias/mm^2) has been successfully achieved [5]. Firstly, electrical measurements performed on a nanovias matrix have demonstrated that nanovias were clearly insulated from each other. Secondly, concerning the nano-object connection itself, it has been demonstrated that the distance between two implanted areas can be decreased down to 30 nm. This last distance is in the range accommodating the actual small extension of intramolecular circuit or of surface atomic-scale circuits [6]. The nano-object positioning between the doped areas is complex; consequently, in order to localize the implanted regions at the nanoscale, specific marks have been designed in the front side of the wafer.

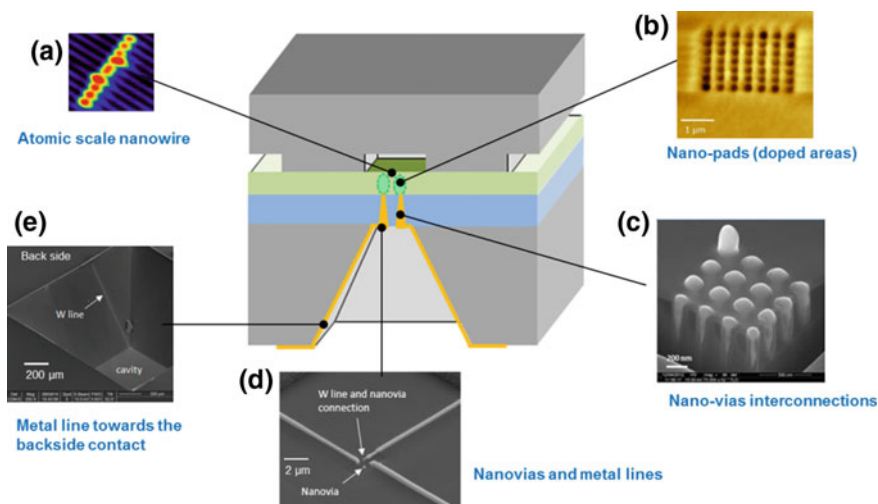


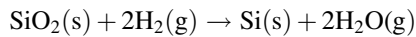
Fig. 3 Interconnections of an atomic-scale dangling bonds nanowire **a** composed of: **b** doped areas (nanopads) linked to **c** nanovias through a 400-nm-thick oxide layer, connected to **d** tungsten metal lines extended in the side of the cavities **e** toward the backside of the wafer

The backside interconnection step of this nanopackaging process is not always achieved, and in this case, only steps 1–4 will be achieved. For example, the presented STM analysis of the Si(001)-(2×1):H in this chapter does not need backside connections.

2.2.1 Reconstruction of the Silicon Surface

The first step of the process flow consists in Si(001)-(2×1):H front side surface preparation. Surface preparation is indeed of prime importance in order to obtain a Si(001) surface fit for hydrophobic bonding, atomic-scale engineering, or epitaxy. In the latter case, the goal is indeed to duplicate the atomic rows of the substrate into the layer. The presence on the surface of amorphous silicon oxide layers, polymers, or etching residues has then a crippling effect on the epitaxy quality. Depending on the nature of the substrate, two strategies may be used to obtain contamination-free Si surfaces fit for use.

The starting substrate may be bulk Si or a SOI substrate. It is then possible to carry out high-temperature bakes, during which dozens of liters of ultra-pure hydrogen, typically only a few parts per billion of impurities thanks to dedicated gas purifiers, are injected at reduced pressure into the epitaxy chamber in order to remove the 0.8–1-nm-thick layer of native or chemical SiO₂ which is initially present on the surface and smooth it. The simplified chemical reaction for the removal of the oxide layer is as follows:

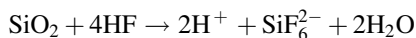


The need for high thermal budgets (typically higher than 1050 °C for 1 min, 1100 °C for 2 min as the CEA-LETI standard) prohibits the use of this surface preparation on patterned wafers (i.e., with active silicon zones surrounded by dielectrics) or ion implanted substrates. The active zones could facet due to strain generated by masking dielectrics, especially in a shallow trench isolation (or STI) configuration. An exo-diffusion of preimplanted atoms and a consequent autodoping of the epitaxial layer may also take place [13]. This type of bake is otherwise prohibited for thin Si films (e.g., less than 20 nm) on top of the buried oxides. If these criteria are not respected, moat recess and islanding of the films will take place [14, 15].

The surface preparation described above (where a native or chemical oxide present on the surface is removed by an in situ H₂ bake in suitable conditions) is thus far from being universal given the high thermal budgets needed. In order to minimize the latter, the following sequence is then typically used:

- (i) Native SiO₂ is removed by a “HF-last” wet cleaning [16]. During the next-to-last step of such a cleaning, the wafer is dipped in hydrofluoric acid diluted in deionized and deoxygenated water (dilution typically between 0.2

and 1%), in order to etch the SiO₂ layer. The dissolution reaction is as follows [17]:



The etching rate of thermal SiO₂, which is the most resistant of all, is around 1.2–1.4 nm.min^{−1} for 0.2% HF. During the last step, the wafer is rinsed in deionized and deoxygenated water to remove all the traces of HF. The wafer is then dried by for instance isopropyl alcohol vapors, before being loaded as quickly as possible in the load-lock chambers of the epitaxy tool, in an inert atmosphere (purified N₂ gas). After such a wet cleaning, approximately 85% of the Si dangling bonds are occupied by hydrogen atoms. The remaining 15% are mainly occupied by fluorine atoms as well as oxygen and carbon contaminants [18, 19].

- (ii) An H₂ in situ bake then takes place at temperature above 800 °C to remove all O, F, or C surface contaminants [16]. A (2 × 1) reconstructed surface perfectly passivated by hydrogen atoms is then obtained which is ideal for epitaxy, hydrophobic bonding or atomic-scale engineering.

A “HF-last” surface is only stable for a few dozens of minutes up to a couple of hours before the regrowth of a native oxide a few angstroms thick can be detected by spectroscopic ellipsometry. Minimizing the time between a “HF-last” wet cleaning and the loading of wafers inside chambers purged with high purity inert gases (such as N₂) is thus mandatory [20]. A perfectly hydrogen-passivated Si surface obtained by a high-temperature H₂ bake is by contrast stable for several days [21].

Concerning the reconstructed surface preparation, we have thus proceeded as follows: after a “HF-last” wet cleaning, we have proceeded with 20 Torr H₂ bakes in order to get rid of residual contaminants and formed (2 × 1)—reconstructed Si surfaces as atomically smooth as possible. Temperatures and durations varied depending on the nature of the substrate: 1100 °C and 2 min for bulk Si(001), to be compared with 950 °C and 2 to 7 min for SOI substrates (for the reasons mentioned above).

In the former case [e.g., on bulk Si(001)], we have deposited at 950 °C, 20 Torr a few tens of nm of Si on top of the annealed surfaces. We have used to that end the lowest SiH₂Cl₂ mass-flow deliverable in a 200-mm Applied Materials Epi Centura 5200 epitaxy tool. The goal was to remove the Si substrate’s starting surface (which might be damaged at the atomic scale), at high temperature and with a low growth rate (75 nm min^{−1} for F(SiH₂Cl₂)/F(H₂) = 0.00125, typically). We thus hoped to promote the surface mobility of Si adatoms and have some step flow growth. The “bulk” process ended up with a 5-min, H₂ bake at 950 °C, 20 Torr in order to obtain a stabilized (2 × 1)H—reconstructed Si surface as perfect at the atomic scale as possible.

An atomic force microscopy (AFM) study has been performed on Si(100):H surfaces after (i) a “HF-last” wet cleaning and (ii) a 1100 °C, 2-min hydrogen bake.

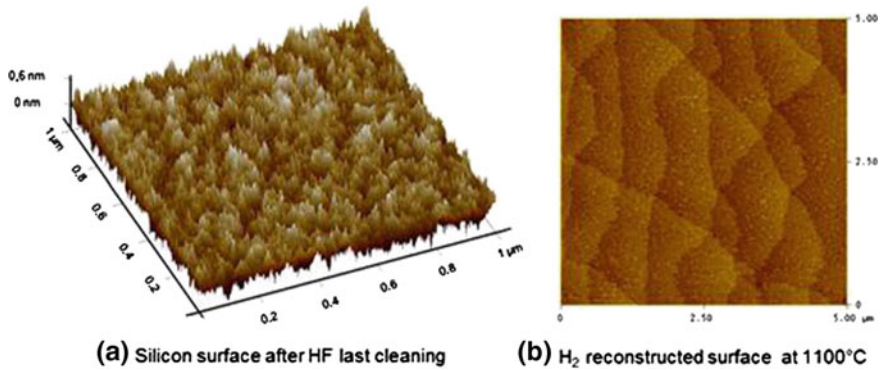


Fig. 4 AFM pictures of Si(001)H surfaces: **a** after a “HF-last” wet cleaning ($1 \times 1 \mu\text{m}^2$ scan size). **b** after a 1100°C , 2 min. H_2 bake (scan size: $5 \times 5 \mu\text{m}^2$); numerous wide terraces bordered by atomic step edges can be seen

This analysis has been made in the purpose of checking the freshly prepared surface. Images are provided in Fig. 3. The “HF-last” surface Z range (e.g., the height difference between the highest and the lowest point of the image) was 0.6 nm (scan $1 \times 1 \mu\text{m}^2$). No terrace was observed on that surface (Fig. 4a). Because of smoothing by the high-temperature H_2 bake, the Z range associated with the reconstructed surface is equal to 0.14 nm only, e.g., the height of a single atomic step. Large terraces are otherwise obvious in Fig. 4b. The terrace mean width is around 100 nm. The widest ones can reach 700 nm.

A well-ordered and smooth surface has thus been achieved; the next steps consist in a direct bonding and dicing steps in order to obtain the surface protection.

2.2.2 Bonding and Dicing

A direct bonding at room temperature has been applied in the clean room in order to reduce the contamination of the encapsulation. This step consists in putting into close contact a 200-mm silicon wafer which received the same reconstruction process described in the previous paragraph. The delay between reconstruction treatment and bonding must be the shortest possible in order to reduce the particles deposition. This time has been fixed at less than one hour for this study. The bonding energy keeping attached the two previous silicon wafers has been measured and compared with the energy of the non-reconstructed silicon wafers as reference. The bonding step has been optimized in order to obtain a low bonding energy providing an easy way to remove the silicon cap. However, at the opposite, a high bonding energy enabling a mechanic dicing without dies debonding is mandatory. A hydrophobic direct bonding step has been developed and the bonding energy has been measured to be between 110 and 140 mJ/m^2 while the reference bonding energy is around 20 mJ/m^2 at room temperature. Hence, the bonding

energy of reconstructed surfaces is more than five times higher than that of non-reconstructed surfaces. This result is consistent with the literature and verifies the fact that a strong dependence between bonding energy and surface roughness can be observed [22]. Besides, the bonding energy can be increased when a thermal treatment is applied, typically between 200 and 300 °C [8]. Such bonding energies have been demonstrated to be well suited for dicing step, i.e., without dies debonding.

Moreover, to make easier the chip's cap removal in a UHV-STM chamber, the nanopackaged chips include etched bevels aiming also at avoiding substrates wasting. Two bevels at the edge of each chip have been etched at the dimensions of 500 μm wide and 50 μm deep. In order to define the dies dimensions for the dicing step, 1.3-mm-wide and 50- μm -deep etched lines have been also added. The nanopackaged chip has been designed in order to receive an organic or inorganic object too; consequently, cavities have been etched in the silicon cap with different sizes ranging between 200 and 2000 μm . Figure 5 represents infrared images of the bonded wafer including a half part of the wafer containing the cavities while the right part does not have it. Figure 5a represents the X-axis etched lines providing the right dicing blade positioning and 1- cm^2 die can be observed in Fig. 5b. The cavities have been well observed in the center of each etched lines in both figures.

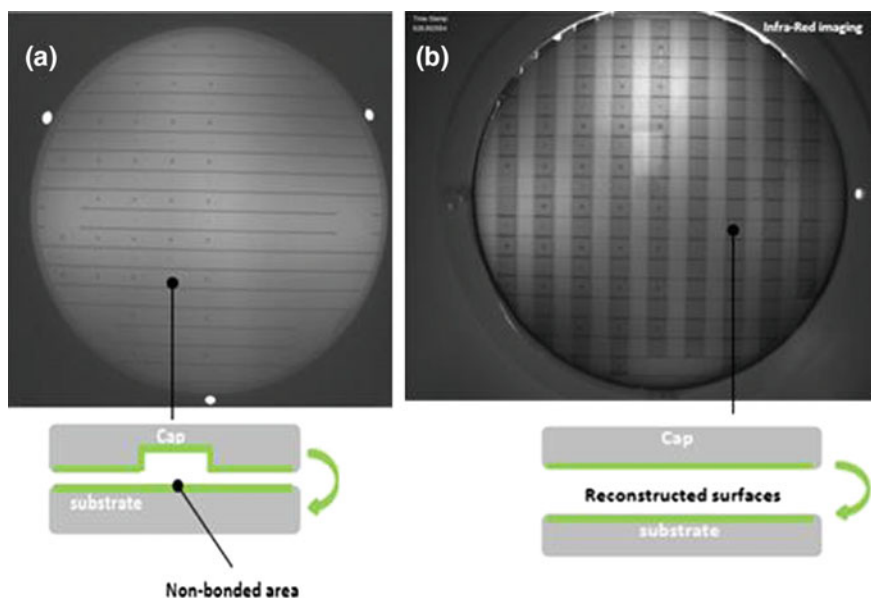


Fig. 5 Infrared images of a bonded SOI substrate with a silicon cap containing cavities in a half part of the 200-mm wafer. **a** X-axis guide etched lines for dicing step can be observed and **b** the 1- cm^2 chips after dicing step. The *left part* includes cavities in the center of the dies, the *right part* have been fabricated without cavities

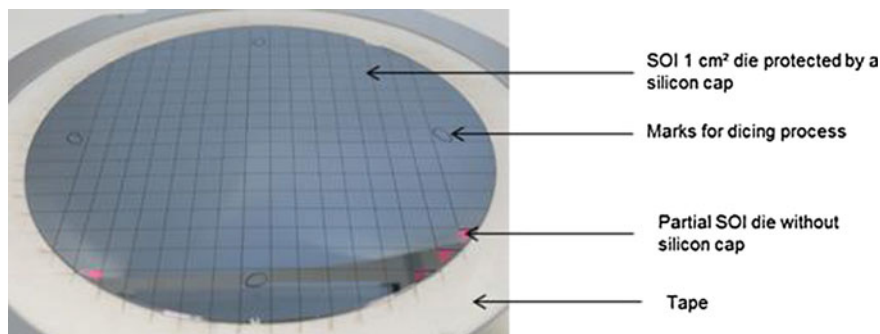


Fig. 6 Photograph of 200-mm SOI substrate bonded with a silicon cap. The wafer has been diced in $10 \times 10 \text{ mm}^2$ dies. Regarding the number of 1-cm^2 die with a temporary silicon cap, a yield superior at 95% has been obtained

Following the guide etched lines, the 200-mm bonded wafers have been diced using a Disco dicing tool. Two steps dicing processes have been used: a S5550 dicing blade ($150 \text{ }\mu\text{m}$ wide) has been used for a cut depth of $615 \text{ }\mu\text{m}$. The dicing blade has been stopped before the bonding interface. A second run has been performed with a S4060 blade ($110 \text{ }\mu\text{m}$ wide) through the bonding interface up to the tape on which has been put the bonded wafers. The saw rotation speed has been fixed at 30 K revolutions/min (rpm). After an optimization process, no dies breakdown has been occurred and only several incomplete dies at the edge of the wafers have been detached as depicted in Fig. 6. The process repeatability has been established superior at 95% of yield considering the entire 1-cm^2 dies. The alignment of the bonded wafers during this step has been ensured by dicing marks previously etched during the process flow.

As represented in Fig. 7, nanopackaged dies have been obtained composed of a silicon or SOI substrate with a Si(001):H(2×1) surface, protected by a silicon temporary cap. The bevels can be observed at the edge of the chip, facilitating the opening of the temporary cap thanks to a blade insertion. The hermeticity is ensured

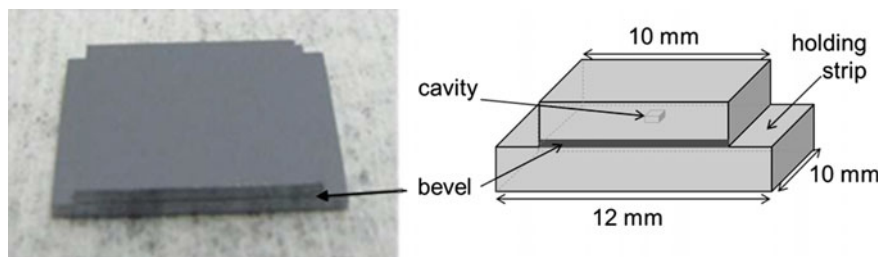
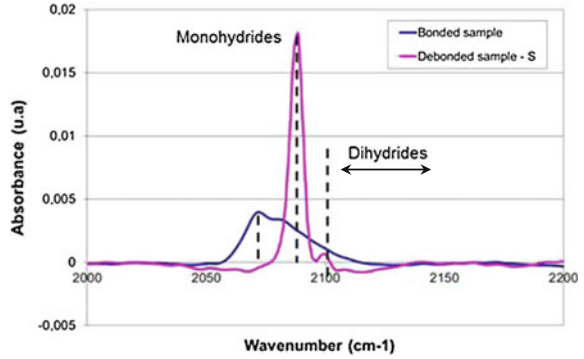


Fig. 7 Picture and scheme of a $12 \text{ mm} \times 10 \text{ mm}$ nanopackaged chip composed of a Si(001):H (2×1) surface protected by a silicon temporary cap and including bevels in order to facilitate the opening of the die

Fig. 8 Typical FTIR-MIR measurements of SiH peaks for “non-bonded” (2080 and 2095 cm^{-1}) and bonded (2065 and 2075 cm^{-1}) reconstructed surfaces



by the direct bonding of the cap and the surface is totally protected against the atmosphere contaminants. The sample can be stored during several months outside a clean room.

At the end of the process, a final control of the surface has been achieved on a die after silicon cap removal in order to verify the SiH surface saturation. A FTIR-MIR spectroscopy has been conducted in order to study the difference between a “bonded surface” and a free surface, i.e., none protected by a temporary cap. As depicted in Fig. 8, SiH peaks for “non-bonded” have been detected at 2080 and 2095 cm^{-1} and have been attributed to monohydrides [23, 24]. For bonded reconstructed surfaces, peaks (2065 and 2075 cm^{-1}) are shifted and are assumed to be due to monohydrides. Wave numbers of peaks attributable to dihydrides (2106 and 2116 cm^{-1}) are drawn for a better understanding.

FTIR-MIR spectrum shows significantly altered spectral shape: The peaks are shifted to lower frequency. This phenomenon has already been observed by Weldon et al. [25] for Si(111) reconstructed surface bonding. To explain this frequency shift, one should consider the modification of the monohydride environment due to the neighboring second wafer surface bonded.

To conclude this part, the 1- cm^2 chips have been successfully characterized and the results have demonstrated the presence of SiH saturation at the surface and large terraces after the reconstruction step achievement. These samples have thus been shipped to research laboratories in which atomic-scale surface studies have been performed using LT-UHV-STM systems.

3 The UHV Debonders

As presented in the previous paragraph, the Si(001):H(2 \times 1) surface is protected by a temporary cap. A hydrophobic bonding [8] has been conducted, and the dicing step has been successfully achieved without cap debonding. A crucial result for the nanopackaging concept consists in controlling the opening of the temporary cap in the UHV chamber in order to have access to the chip surface for atomic-scale

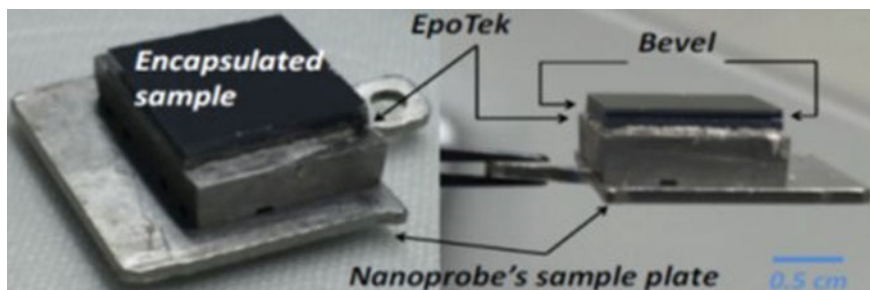


Fig. 9 A capped passivated silicon chip positioned on a Scienta Omicron sample plate using an EPO-TEK H21D glue. The blade of the UHV debonder will be introduced right inside one of the two bevels depending of the way the sample is pushed on the slider of the debonder

surface characterizations. The top-encapsulated passivated-silicon chips have to be opened under UHV conditions to avoid as much as possible any trace of contaminants before UHV-STM characterizations. As recalled in the above sections, Si(100)-H:(2×1) is a very reactive surface for the chemical contaminants in ambient conditions. Thus, we have chosen to minimize the number of native surface defects by opening the chip under UHV conditions. On a dice, the location of the bonding interface is indicated by a bevel (cf. Sect. 2.2.2) cut on the two opposite sides of the chip as illustrated in Fig. 9. To remove the cap, a robust cleaving blade is positioned flat as regards and toward the bevel. Then, the capped chip is pushed hard 500 μm deep inside the bevel between the cap and the sample. This toggles the cap out of the chip with a force applied corresponding to the force required at least to break the interfacial bonds between the two wafer-bonded substrates as detailed in the previous paragraph.

The selection of the glue to fix up robustly the backside of the silicon chip on a Scienta Omicron sample plate is an important step of the full process to be UHV and low-temperature compatible. Since in the following, the presented characterizations are performed on LT-UHV-STM systems, the selected glue has to stay conductive at 4 K, to be UHV compatible and hard enough to bear all the transferring steps through the successive chambers of our systems and first to resist the debonding step. Two kinds of glues have been tested: indium and a conductive epoxy polymer (EPO-TEK H21D). In our case, with our UHV “debonder” system EPO-TEK leads to the most reproducible results in term of stability. After preparing the EPO-TEK with a ratio 0.1/0.01 g and having left it at rest overnight, this preparation was applied as homogenous as possible on the sample transfer plate. Before gluing, the chip must be clean and non-oxidized at its backside to ensure a back ohmic contact with the metallic transfer plate. We have also taken care of the fact that the chip is perfectly free of any trace of constraints as cracks or pieces crumbling apart particularly at the edges of the dice. After positioning the chip on the glue at the surface of the transfer plate, the glue was polymerized by heating the sample up to 80 °C for 90 min in a standard laboratory oven. Finally, the encapsulated chip was inserted in the load-lock chamber of the LT-UHV-4 STM system

until the pressure in the system is stabilized down. This last phase may be critical in terms of applied mechanical constraints, as the temperature gradient is quite large [from the room temperature to the liquid helium or nitrogen temperature (4 and 77 K, respectively)]. During this step, it may happen that some samples simply break into the UHV analysis chamber of our nanoprobe.

The first generation of UHV debonders is presented in Fig. 10a. This mechanical tool is settled up in an UHV chamber of our UHV system at a base pressure of 3×10^{-11} mBar. It consists in a blade adjustable in height with a screw, in a metallic slider where the encapsulated chip is inserted until it gently touches the blade. To push the cap away, a wobble-stick was used to abruptly push again the sample plate toward the blade but without touching the chip. It generally results in a fast ejection of the cap away of the debonder, within some cases a collision happens between the end of the debonder and the chip itself since the alignment of the wobble-stick end with the sample stage cannot be perfect in this case.

After several trials, this technique was proved to be too brutal for the chip as for the wobble-stick itself. Furthermore and already noticed above in our UHV system configuration, it is almost impossible for the wobble-stick end to hit always the

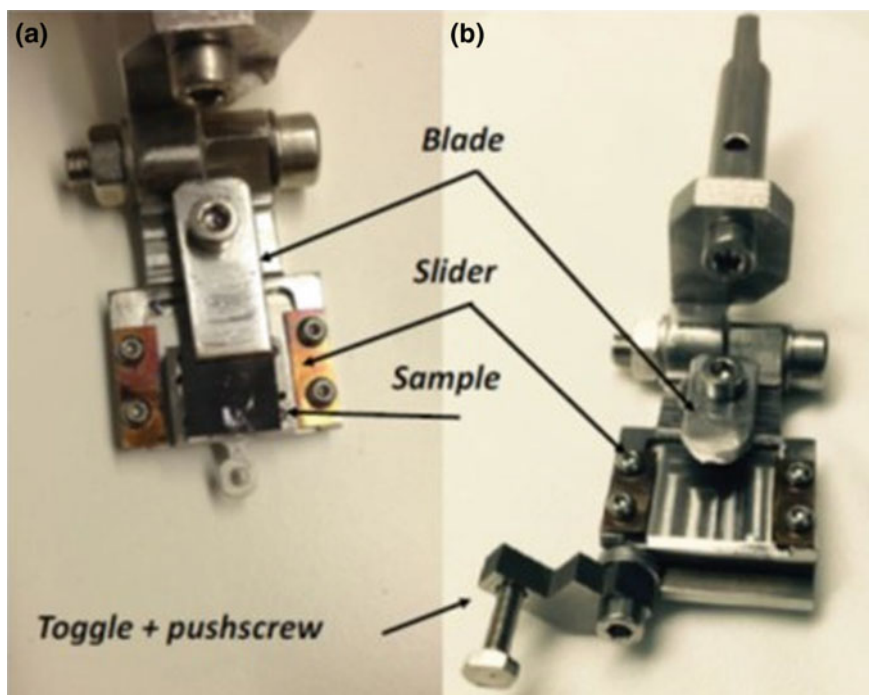


Fig. 10 The first (a) and second (b) generations of debonders. Different blade shapes have also been tried in order to minimize the constraints on the sample itself during the opening. The «push screw» on (b) is grabbed directly with the wobble-stick and rotated to push the sample toward the blade

same point on the trench of the sample plate when several trials are necessary to debond the cap. A second generation of UHV “debonding” was designed and fabricated as presented in Fig. 10b. A simple opening torque was added at the outer edge of the slider to hold the sample itself during the pushing toward the blade. This toggle owns an extra screw facing the sample which plays the role of a “push screw.” After this toggle is latched down on the debonder, this push screw is directly grabbed by the end of a rotating wobble-stick. Then, the push screw is rotated, pushing the sample toward the blade until the ejection of the cap occurs out of the sample. This is the debonding system used for the results presented hereafter in this chapter. However, the rotating wobble-stick was shown to be too weak for some samples. A new generation of debonder is under study with a fixed sample and a slow step-by-step approach of the cleaving blade toward the bevel. These further modifications were thought to keep minimizing the mechanical constraints applied on the nanopackaged chip.

4 UHV Surface Characterizations After the Opening

After its opening, the sample is transferred into the next UHV chamber where the LT-UHV-4 STM is seating without any further preparation. Then, a first approach of the tungsten tips is performed using an optical camera to locate them through the window on the surface sample as presented in Fig. 11.

This step permits to take a large-scale glance at the surface and to visualize macroscopic defects, if any. The macroscopic defects appearing on the surface in Fig. 11 may come from the cap removal. They may also have been trapped at the bevel space, coming from the slicing of the 200 mm wafer in chips.

Thanks to the on-top UHV scanning electron microscope (SEM) standing just above the four STM tips of the LT-UHV-4 STM head and also above the sample, a careful look on the sample surface cleanness was most of the time performed first at room temperature with a resolution better than the above Fig. 11 optical inspection. Figure 12 SEM image is giving a general picture of a sample edge after its opening in the UHV. Very few damages seem to have been created with our debonding technique.

For the low-temperature STM characterization, the debonded Si(100)H chip was slowly transferred on the LT-UHV 4 STM stage maintained at 4 K to avoid a too fast change in temperature of the sample starting from room temperature. Therefore, the sample was left for at least 15 min on the shielding door of the LT-UHV 4 STM inner cryostat before its direct insertion on the 4 K LT-UHV 4 STM head. Finally, we have statistically STM-scanned large-size areas by positioning the tips of our LT-UHV-4 STM system on the Si(100)H surface using the viewport optical camera as presented in Fig. 12.

A first set of STM images was obtained at liquid nitrogen temperature (77 K). As a first example, Fig. 11 is indicating where Fig. 13 STM image presented below was recorded. Each STM scanner of our LT-UHV 4 STM is able to scan over a

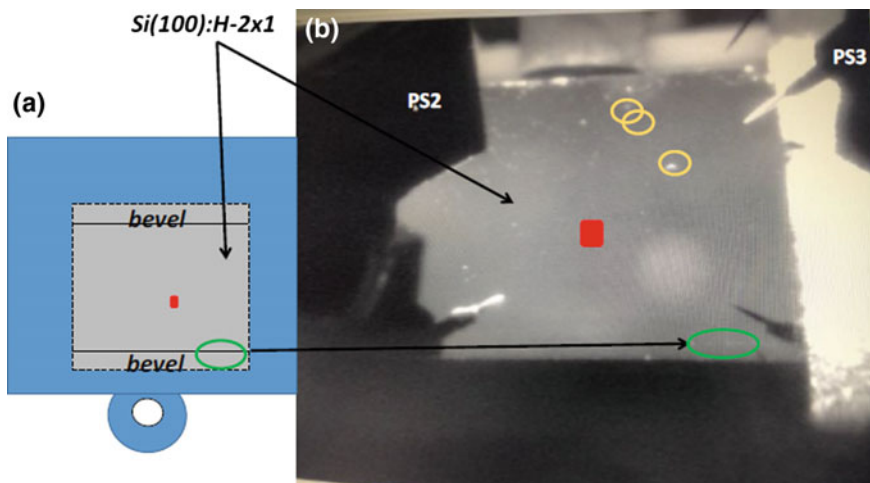


Fig. 11 **a** A schematic of a debonded sample (in gray) sitting on its sample plate (in blue). The red area is indicating where the tip loaded on the piezo scanner 3 (PS3-right side on **b**) is going to land on the surface. The location of the bevells where the blade was inserted to remove the sample cap is also indicated in A. The optical photograph **b** was recorded through a viewport of the LT-UHV-4 STM during the manual approach of the tips toward the surface of the chip. The 45° oriented tips loaded on PS3 and PS2 are reflecting on the Si(100)H surface. The area in red (**a**) was reported in (**b**) to persuade the reader that an STM tip apex can be very precisely located on the sample surface. The remaining trace of a bevel is indicated by the green circle on (**a**) and (**b**). The yellow circles are indicating the position of some macroscopic dusts on the surface

maximum window of about $2\ \mu\text{m} \times 2\ \mu\text{m}$. Notice that the complete chip surface is reachable by each scanner. But we have specifically imaged the Si(100)H surface area found under the tip apex of a given scanner. After a manual approach of the tip toward the surface, the Matrix software was left approaching gently and automatically a given tip by setting up the tunneling current intensity and the corresponding bias voltage like in a standard LT-UHV-STM. Here, we have used typically 2 V, 5 pA for the first approach in the tunneling regime. When the STM tip apex is stable enough, a large area can be scanned, typically in a scanning range between 50 and 500 nm (Fig. 13).

In average, we have found that the mono-atomic terraces are about 200–400 nm in lateral extension for the chips we have characterized and some mono-atomic stepped depletion areas are always observed distributed randomly all over a given terrace. Furthermore, the areas close to the edges of the Si(100)H chip are more defects covered than the central part of the chip as presented in Fig. 14.

Close to the edge of a given chip (red rectangle on the gray area Fig. 14b), it was possible to scan over some short mono-atomic terraces and their edges. Figure 14a empty-state STM image is characteristics of the relative disorder of this peculiar chip edge. Some SiH dimer rows can still be imaged running perpendicular from one terrace to another. Some dimers are decorated by some atomic-scale defects with defect density about 0.5 per nm^2 at the edge of this chip.

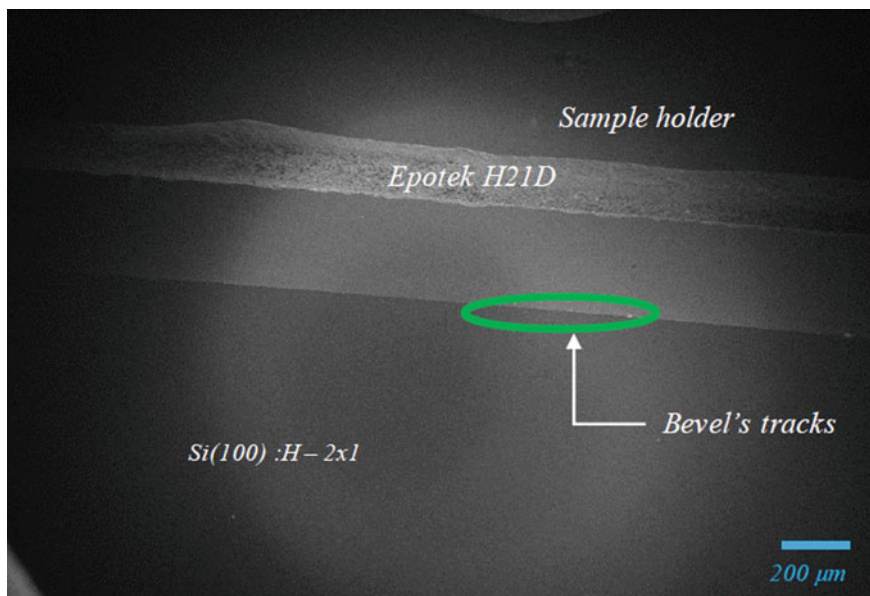


Fig. 12 An SEM image obtained at room temperature at the bevel-side edge of a debonded Si(100)H passivated surface. This is a quite uniform area without any kind of large damage even in the area where the blade hit the bevel. Similar images can be recorded at each edge and at all the surface indicating that apart from the large dusts observed in Fig. 11, this surface was not damaged after the debonding step

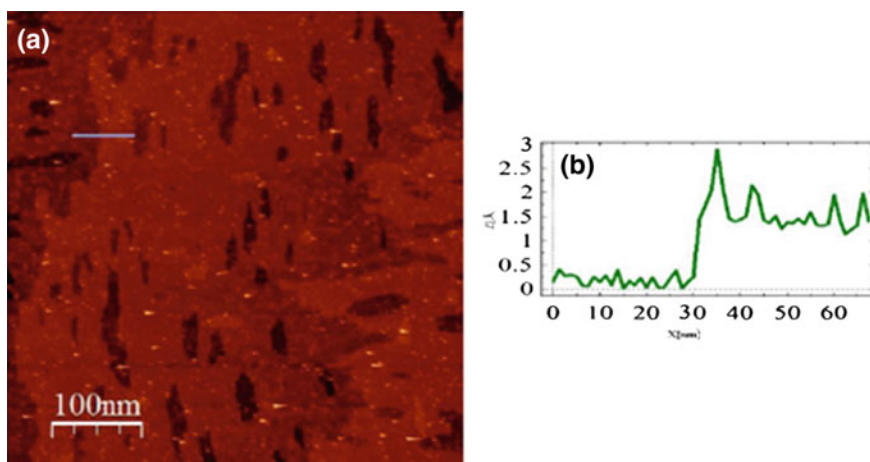


Fig. 13 a A large-scale constant current STM image ($500 \text{ nm} \times 500 \text{ nm}$) of a UHV debonded Si(100)H surface recorded at 77 K using a vertically positioned tungsten tip with $V = 1.9 \text{ V}$ and $I = 5 \text{ pA}$. The scanned area is relatively cleaned. There are large parallel more than 300 nm in width mono-atomic terraces running along this area of the surface. As presented in (b), the terrace STM image corrugation is below 50 pm with a characteristic mono-atomic step height for Si(100)H of about 150 pm. The large bumps on the top terrace as observed on (b) are due to very local atomic-scale impurities which remain to be identified

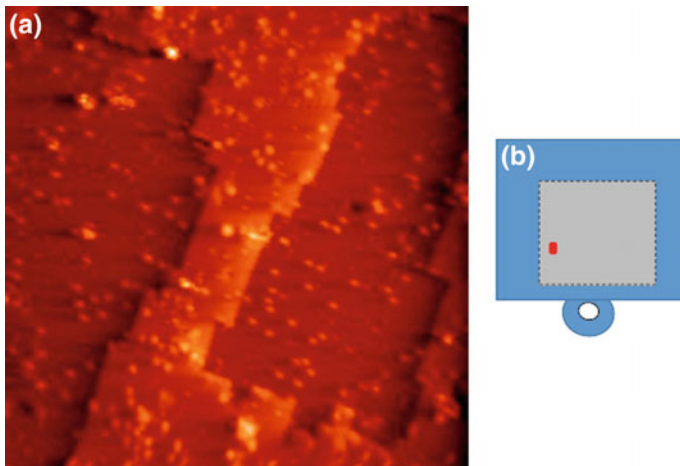


Fig. 14 a 50 nm \times 50 nm constant current STM image recorded at 77 K on an area close to the edge of the Si(100)H debonded chip (scanning location indicated by the *red rectangle* on **b**) for 2.0 V and $I = 20$ pA. This image is indicating how the surface of this particular chip was not uniformly clean at its edge. In particular, it was difficult to scan over the multiple steps while maintaining a stable tip apex

Further investigations aim at understanding the origin of the defects and reducing the defect density. In order to reduce the particle level due to the dicing step of the chips, a chemical cleaning has been added in order to reduce the contamination during the opening. The optimization of the sample opening protocol is a key parameter and several tests are conducting which will enhance the defect density. Concerning the local atomic-scale impurities and mono-atomic stepped depletion areas, several studies could be started on the reconstruction surface treatment described in the Sect. 2.2.1, especially using a percent of Hcl gas during the reconstruction process providing a better smoothing and a lower incorporation of contaminant in the RP-CVD reactor. Nevertheless, the STM characterization at 77 K in the center of the sample has demonstrated a very high surface quality with flat and large Si(001):H terraces separated by single atomic steps. Consequently, surface analysis with a higher resolution has been successfully carried out with LT-UHV-STM at temperature of 4 K.

5 LT-UHV-STM Atomic-Scale Images

Atomic-scale images of the hydrogenated Si(001):H surface have been performed first with a single tip LT-UHV-STM after on the LT-UHV-4-STM whose head is equipped with 4 STM tip able to scan in parallel on the same surface.

5.1 LT-UHV-STM-IP Probe Surface Studies

The characterizations were carried out in a Krakow UHV system from Omicron NanoTechnology GmbH with a base pressure of 5×10^{-11} mbar. The UHV system consists of three interconnected chambers incorporating high-resolution SEM, LEED optics and low-temperature STM (LT-STM). All STM measurements were performed thanks to an Omicron LT-STM operating at the cryogenic temperature of 4 K with electrochemically etched polycrystalline tungsten tips used as probes. All values of bias voltage in STM experiments presented in the report are given with respect to the sample. SPIP and WSxM [26] software were used for image processing and STM data analysis.

For LT-UHV-STM characterization samples are transferred immediately after the debonding process to the LT-STM cryostat, where they are cooled down to 4 K. Because the samples prior to opening under UHV are protected by a bonded cap, we do not apply any additional preparation process. It is worth noting that this is a quite new approach in cooperation between industrial type of material processing site and the research laboratory. We are able to reach down lower temperature with the system such as liquid helium temperature (4.2 K). At a large scale, we are able to switch the tip bias voltage from positive (filled-state images) to negative one (empty-state images), chasing the differences between the charged defects, as dangling bonds, an atom or cluster laying on the surface as illustrated in Fig. 15.

Results are shown on the representative $100 \text{ nm} \times 100 \text{ nm}$ filled-state images presented in Fig. 16. It has been confirmed that the surface crystallographic structure of the hydrogenated Si(001):H is relatively well preserved for large, flat, and single-terrace areas. The high-resolution STM nm-scale scans of the debonded

Fig. 15 High-resolution LT-STM image (STM scanning parameters: $V_{\text{bias}} = -2 \text{ V}$, and $I = 10 \text{ pA}$; $100 \text{ nm} \times 100 \text{ nm}$) of the Si(001):H surface after debonding of the sample no. H-dimer rows are clearly visible

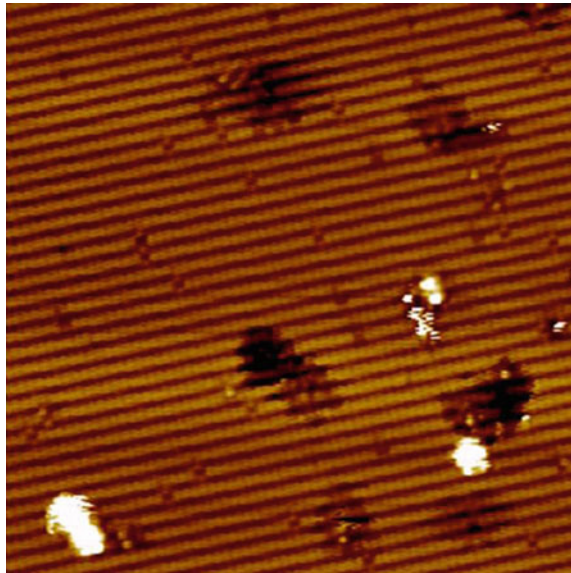
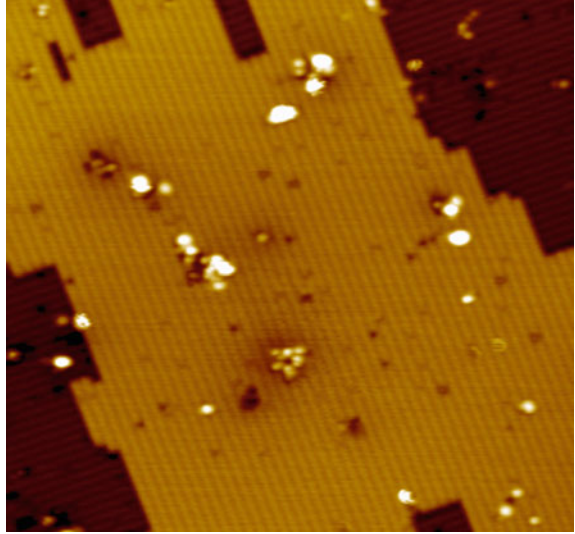


Fig. 16 High-resolution LT-STM image (STM scanning parameters: $V_{\text{bias}} = -2.5$ V, and $I = 10$ pA; $100 \text{ nm} \times 100 \text{ nm}$) of the Si(001):H surface after debonding of sample. H-dimer rows and atomic step edges are clearly visible



sample clearly show that the surface is passivated by a monolayer of hydrogen atoms, which form a stable monohydride (2×1) phase in which each Si surface atom is bound to one H atom. The agglomeration of defects (white corrugations) observed on the atomically clean terraces in both figures could be due to the chemical processing used during the surface preparation or the wafer debonding procedure itself. In fact, Si vacancy agglomerations with the similar structures and density (black contrast) indicate that the defects could be formed during the debonding process and white corrugations consist of the Si adatom agglomerates. The average defect densities estimated from several STM scans on the debonded surfaces are about 1 defect per $40\text{--}50 \text{ nm}^2$. The average defect densities estimated from several STM scans on the debonded surfaces are about 1 defect per 50 nm^2 . Even if these defects have been reported and the density has been consistent with the literature [27], further investigations are running to discriminate the surface reconstruction impact and the debonding effect. To conclude, the reconstructed Si(001)-(2×1):H surfaces have been successfully observed at the atomic scale and can be used for nanodevice fabrication.

Another characteristic feature of the analyzed sample structure is lack of any dangling bond defects. The overall high quality of the surface allows for surface DB structures construction by hydrogen atoms desorption with the use of a STM tip.

5.2 LT-UHV-4 STM Surface Studies

Another Si(100)-H:(2×1) surface study at the atomic resolution has been conducted using a more recent STM tool built by Scienta Omicron GmbH and containing 4

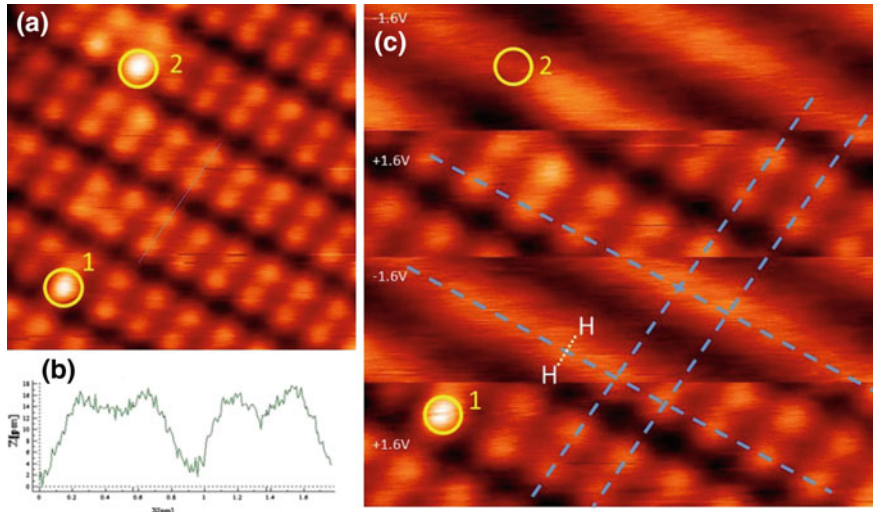


Fig. 17 Atomically resolved constant LT-UHV-STM images **(a, b)** recorded with scanner 4 of the LT-UHV-4STM head at small scanning range ($4 \text{ nm} \times 4 \text{ nm}$) using a vertical tip configuration. The *left image* in **(a)** was recorded at $+1.6 \text{ V}$ for $I = 35 \text{ pA}$. The **(b)** image was recorded alternatively shifting the bias voltage between $+1.6 \text{ V}$ and -1.6 V during one image recording with the sequence indicated on **(b)**. The *blue dotted line* is indicating the positions of the SiH dimers parallel and perpendicular to the 2×1 reconstruction of the Si(100)H surface. The *yellow-circled defects* are underlined to prove that **(a)** and **(b)** are exactly the same scanned areas. **c** is giving a scan line extracted from **(a)** $+1.6 \text{ V}$ image with a 15-pm corrugation. On **b**, the position of the two hydrogen atoms of the same SiH dimer is represented

piezoelectric scanners. The whole UHV-4 STM chamber was maintained at a base pressure of $3 \times 10^{-11} \text{ mBar}$ during this study. After having located rather free of defects large-terrace areas on the chip, the LT-UHV-4-STM was cooled down to 4.2 K keeping the Si(100)H debonded sample on its sample stage. At 4.2 K , the Toulouse PicoLab (CEMES) LT-UHV-4 STM had already demonstrated a Δz noise level better than 2 pm on an Au(111) surface [28]. Figure 17a is presenting a small $4 \text{ nm} \times 4 \text{ nm}$ area constant current image of the small portion of Si(100)H surface selected in the center of the chip. This is a typical positive bias voltage image of the 2×1 monohydride rows reconstruction. A scan line was extracted from this image perpendicular to the row (Fig. 17c) confirming the nice 2 pm noise level of our LT-UHV-4-STM.

Care must be taken to interpret Fig. 17a STM image in the prospect of determining the exact atomic-scale structure of this imaged portion of the Si(100)H surface. For this purpose and to explore further the surface contrast variation as a function of the bias voltage, a systematic change of the bias voltage was performed switching alternatively the bias voltage between $+1.6$ and -1.6 V during the recording of a constant current STM image. As presented in Fig. 17b and at -1.6 V , the maximum STM contrast perpendicular to the rows is exactly located in between the 2 small maxima obtained at $+1.6 \text{ V}$. This half-row apparent shift has

been analyzed in detail in [29] (see also Chapter [Atomic Wires on Ge\(001\):H Surface](#)). At positive bias voltage, the tunneling conductance in between the two hydrogens of the same SiH dimer is larger than the direct conductance through a single SiH bond [29]. As a consequence, the good way to locate the SiH dimer on the Si(100)H surface is to record its STM image at negative bias voltage and not at positive.

To better characterize the existing defects on the Si(100)H passivated silicon surface after its debonding, Fig. 18 is pointing out defects larger in size as compared to the 2 atomic-scale defects imaged in Fig. 17 and located by a yellow circle. They can be classified by size and electronic properties [30]. In Fig. 18, the defects circled in green are smaller than those circled in blue and give the same apparent contrast in the empty- and filled-state STM images. They are also easy to manipulate with the STM tip. They are superficial impurities coming from the sample environment and are not chemisorbed on the Si(100)H surface. On the contrary, the blue-circled impurities cannot be manipulated during scanning but are

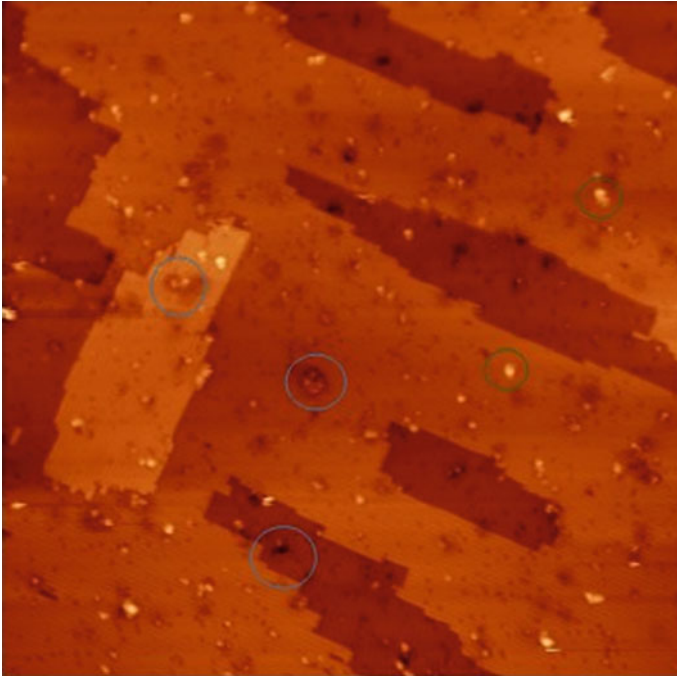


Fig. 18 A large 100 nm \times 100 nm constant current STM images recorded in the center of the debonded Si(100)H chip at 4.2 K for -1.67 V and $I = 15$ pA. Several nanoscale surface defects have been *circle* in *blue* and *green*. The *blue-circled* defects are surrounded by a native dark hallow indicative of a LDOS-depleted areas induced by the impurity itself. The *green-circled* defects can normally be manipulated by the STM tip during a scan. Scanned areas as presented in this figure are clean enough not to contaminate the tip. On this debonded chip, those are the best places to start constructing atomic-scale circuits

electronically unstable by changing the bias voltage. In the filled-state images, they are generally surrounded by a dark shadow (Fig. 18) indicating a LDOS depletion around such a defect, a signature of an acceptor-like type of defect. It can be residual native doping species surfacing from the bulk during the thermal treatment of the fabrication process or simply some residual oxygen remaining in the chamber. Large-size defects with an apparent diameter of 10 nm or more may be coming from surrounding dusts deposited on the surface during the debonding. They are quite rare over the surface of the imaged chips.

Coming back to atomic-scale defects, we have observed that the chip surface is covered by a few native Si single dangling bonds (DBs) and also by dihydride SiH₂ defects that can be observed both in filled- and empty-state images as presented in Fig. 19. For filled-state images, each DB is appearing as a bright protrusion along a dimer row with generally the DB protrusion being shifted off the SiH dimer center as presented in Fig. 19. In empty-state images, a single DB is spotted as a dark depletion and can be imaged surrounded by a dark halo [31] depending on the tip, the doping level of the silicon substrate and on the bias voltage. Bare silicon dimers and dihydride dimers can also be easily imaged on the Si(100)H surface as presented in Fig. 19a, b. Those are STM imaged as bright asymmetric protrusions

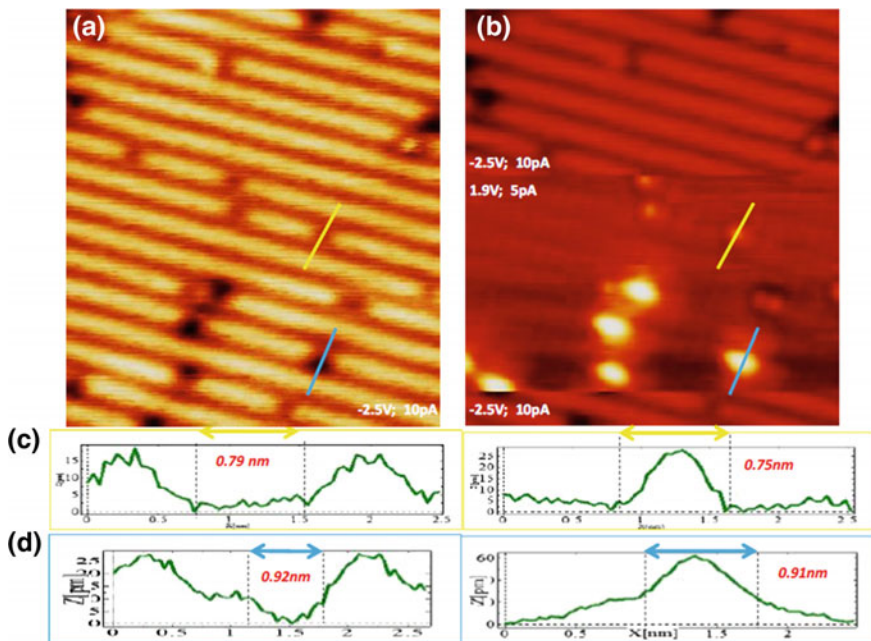


Fig. 19 **a** 9 nm × 14 nm constant current STM image recorded at -2.5 V, $I = 10$ pA. **b** The same Si(100)H surface location imaged now at +1.9 V, $I = 10$ pA. The surface defects along the dimers rows appearing as a depletion for negative bias voltage and as large protrusion for positive one. Scan lines were extracted in both cases as presented in (c) and (d) (yellow and blue lines in **a** and **b**, respectively). Corrugation of these images is about 60 pm maximum

along the dimer row for empty-state images and as a dark depletion in the filled-state images. The asymmetry in the STM images is due to the buckling of the silicon dimers.

Finally, returning on a clean Si(100)H surface area, single I - V curves were recorded to measure the surface apparent electronic gap relative to the bulk Fermi level position which must be located in the middle of the valence band-conduction band gap since the used silicon wafer is intrinsic. I - V curves can be recorded on many location on this Si(100)H surface showing different tunneling conductance for the same feedback current. In the case presented in Fig. 20, the STM tip apex was positioned above a hydrogen atom of a single DB dimer marked in Fig. 20A by a white star. Our LT-UHV-4 STM head being stable enough for long time single shot I - V recording, the feedback loop was turned off during more than a tenth of seconds to ramp the bias voltage starting from -1.6 V up to $+2.0$ V and back to record the consequent tunneling current intensity. After the recording of the final I - V point, the feedback loop is turned on again to recontrol the tip apex height relative to the surface. Following this process, the apparent Si(100)H surface energy

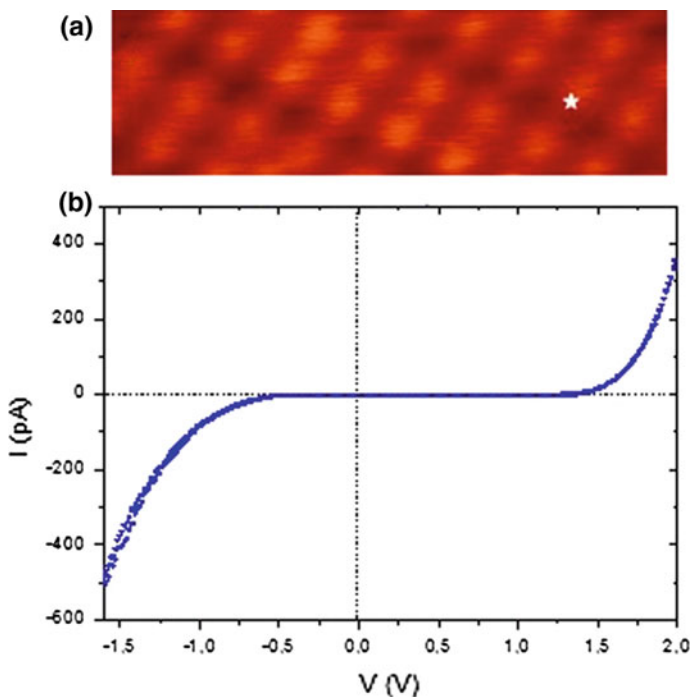


Fig. 20 **a** $4 \text{ nm} \times 1.3 \text{ nm}$ constant current STM image recorded at 4.2 K for $+1.6$ V and $I = 35$ pA. **b** A one shot I - V curve recorded on a single hydrogen atom location for a setup current of 35 pA with a bias voltage scanned from -1.6 V to $+2.0$ V both with the feedback loop off during this recording. The apparent gap is about 1.7 eV for this initial $+1.6$ V and $I = 35$ pA tip apex to surface relative distance

band gap was found to be about 1.7 eV. This value is smaller than the known 2.1 eV surface gap for the Si(100)H surface because Fig. 20 I - V characteristics was recorded in the z direction (sample grounded) meaning with a true k_z direction 1.1 eV electronic bulk silicon gap. The surface 2.1 eV gap in the k_x (k_y) gap direction of the surface band structure can only be measured using a floating 2 STM tip surface measurement, i.e., with the back sample ground disconnected. Depending on the setup feedback current, this apparent 1.7 eV gap can vary from larger than 2.1 eV to its minimum of 1.1 eV.

6 Summary and Conclusion

In conclusion, this chapter clearly demonstrated the interest of a nanopackaging approach for the UHV environment applications. A technology has been developed on 200-mm Si or SOI wafer in a standard industrial-like clean-room way enabling to obtain a hydrogenated Si(001):H-(2 \times 1) reconstructed surface, protected by a temporary silicon cap. After opening, the surface can be used without applying any additional preparation process usually applied in a UHV chamber requiring a complex protocol. This surface preparation is composed of a chemical cleaning and a hydrogen silicon surface passivation which provides a low particle density and a well-ordered reconstructed surface. FTIR characterization has demonstrated a full SiH monohydrides surface passivation of the silicon surface. A hydrophobic direct bonding between SOI substrate and a silicon wafer has been conducted and which protects the surface against contamination due to the atmospheric air exchange such as hydrocarbons or particles. The bonded wafers are diced into 1-cm² samples in order to be loaded in a STM holder. The nanopackaged samples can thus be stored during several months before its opening and use by the research laboratory. To remove the cap, a robust cleaving blade must be positioned at the bonding interface in a UHV chamber. The samples are transferred immediately after the debonding process to the UHV- LT-STM chamber and then on its sample stage, where they are cooled down to 4 K.

An atomic resolution has been obtained and demonstrated that the surface crystallographic structure of the hydrogenated Si(001):H is relatively well preserved for large-, flat-, and single-terrace areas. The high-resolution STM scans at the atomic scale have clearly shown that the surface is passivated by a monolayer of hydrogen atoms, which forms a stable monohydride (2 \times 1) phase and in which each Si surface atom is bound to one hydrogen atom. Agglomeration of defects has been observed on the atomically clean terraces, with a higher density in the edge of the samples. However, the quality of the surface is convenient in the major part of the surface for molecule grafting or surface nanoscale device fabrication.

Further investigations are under way in order to improve the surface, focusing on reconstruction step or chemical cleaning step on the die. These process changes should positively improve the Si(001):H surface quality in the foreseeable future. Others works concern the surface studies after a dopant implantation. In order to

connect the nano-object on an implanted area, the doped surface damages must be removed by the reconstruction treatment while carefully controlling the dopant diffusion effects. These product developments have demonstrated the fabrication of such structures on an industrial scale and directly usable for atomic electronic devices or technologies based on molecular logic circuits thanks to the collaboration between clean room microelectronics players and research laboratories.

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