

Chapter 2

Fabrication Techniques

The microelectronic industry uses several fabrication methods in order to deposit layers of dielectric and metallic materials. Besides, lithography processes and temperature treatments are needed to define the active areas and improve the electrical characteristics of the devices.

In this chapter, the different fabrication techniques used during this thesis are described. The core of this thesis was the fabrication of metal-insulator-semiconductor (MIS) capacitors using high κ dielectrics in order to perform structural and electrical characterizations of these materials.

The technique used for the deposition of thin films of high κ materials was high pressure sputtering (HPS). This system was widely studied and here it is described in depth. Glow discharge optical spectroscopy (GDOS) was employed as a tool to study the species presented in the plasma during the deposition.

The metallic electrodes were grown by means of the electron beam (e-beam) evaporation system. This technique was also used for the growth of a thick SiO_x layer that acts as field oxide (FOX).

In order to define the top metal electrodes, two different lithography processes were used, depending on the particular conditions of each MIS device fabrication.

The temperature treatments were carried out in a rapid thermal annealing system (RTA) using a forming gas atmosphere.

Two types of semiconductors (Si and InP) were used to fabricate MIS devices. The characteristics of these substrates and the cleaning procedures are also described at the end of this chapter.

2.1 High Pressure Sputtering (HPS)

During this thesis, the system used for the deposition of high κ materials was HPS. As it was commented in the former chapter, this system works with a pressure in the mbar range, which is two or three orders of magnitude higher than conventional

sputtering systems. The main advantage is that this high working pressure avoids the degradation of the semiconductor surface because the particles suffer many collisions and get thermalized before reaching the substrate.

The HPS system used in this thesis, and shown in Fig. 2.1, was initially purchased from Forschungszentrum Jülich (Germany), where it was designed for the deposition of superconducting films [1] and was adapted by the *Thin Film and Microelectronic Group* [2–4] for the deposition of several high κ materials from oxide targets [5–9].

In Fig. 2.2, a scheme of the HPS system is presented. The targets used during this thesis are metallic Gd and Sc, with the maximum purity available of 99.9%, purchased from *Kurt J. Lesker*. The diameter of both targets is 2 in. (~ 5 cm) and the thickness is 1/8 in. (~ 0.3 cm). Both materials are glued to the cathode of the system with a *Varian* Torr-seal low vapor-pressure epoxy resin. The targets are fixed to a mechanical arm that can hold up to three different targets and its movement in one axis is controlled and can be automated using a motorized system from *Isel Automation*. This allows sputtering the target surface away from the substrate (thus, “conditioning” the target), preventing deposition during this process without needing shutters that can become contaminated over time. The mechanized arm also permits nanolaminates deposition [10] and an excellent control of layer thickness by controlling deposition time. To avoid the degradation of the glue, due to the heating of the targets, the system is refrigerated by a water circuit.

The plasma is generated with a radiofrequency (rf) source model *PFG 300* from *Hüttinger* at a standard frequency of 13.56 MHz. The connection to the system is made through an impedance matchbox. This matchbox adapts the plasma

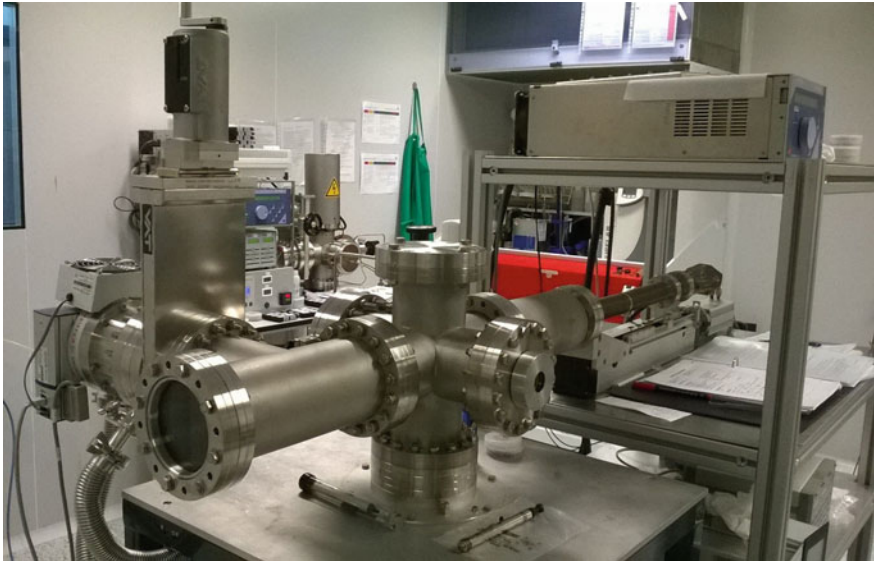


Fig. 2.1 Picture of the high pressure sputtering used for high κ materials deposition

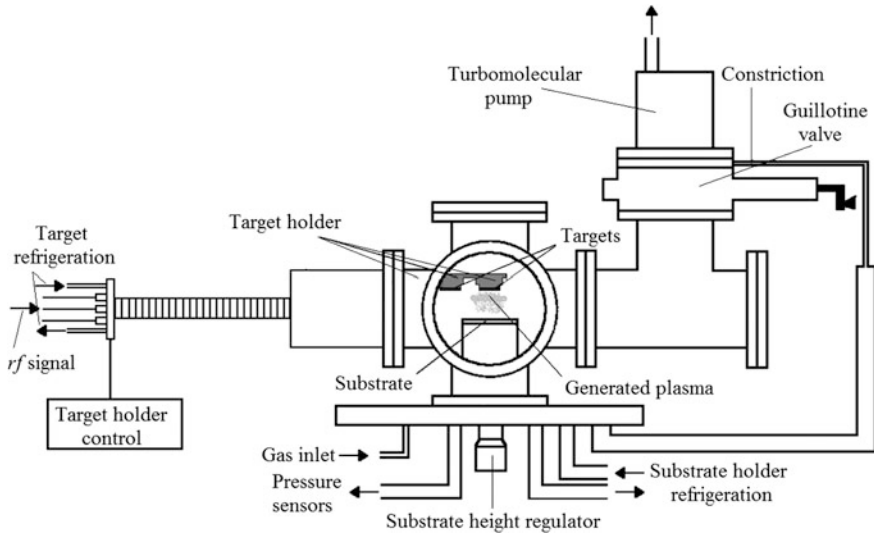


Fig. 2.2 Scheme of the high pressure sputtering used

impedance to the source impedance and it is placed close to the cathode to prevent *rf* losses. It consists in several capacitances in parallel with inductors. Two of the capacitors can be adjusted manually for obtaining the minimum reflected power. The reason of using *rf* and not DC power is because the system is prepared to deposit insulators [2–4]. The use of the *rf* signal is mandatory in those materials in order to avoid a charge accumulation on the surface of the target that would switch off the plasma [11–13]. In this work, the targets used are metallic, so the *rf* signal should not be necessary. But, if the metallic surface of the target would be oxidized (even locally) this could produce high voltage discharges, producing plasma instabilities and possibly damaging the devices. Also, the epoxy used to glue the targets to the cathode is insulating and it would be necessary to use a conducting one. Therefore, in order to keep the know-how of the system operation, achieved in previous works, we decided to stick to the same *rf* system and epoxy glue.

The chamber, that reaches a base pressure in the order of 1.0×10^{-6} mbar, is connected to a *Pfeiffer TMU 261* turbomolecular pump supported with a roughing system. During the first part of this thesis, the support pump was a compact model *Drytel 31* from *Alcatel*, which was replaced afterwards by a modern *Hi Cube* model from *Pfeiffer Vacuum*. Both systems have the same structure: a small turbomolecular pump and a membrane pump. After pump substitution, there were no differences in the system behavior. Between the vacuum system and the chamber, there is a guillotine valve that allows regulating the effective pumping speed. This valve is fully opened when there is no deposition, to achieve the base pressure. However, keeping the valve opened during sputtering would imply excessive gas flow (that would heat the turbomolecular pump to the point of self-stopping to avoid permanent damage). Thus, when the deposition is taking place the position of

the guillotine valve is manually regulated, controlling the chamber pressure with a fixed gas flow.

Three different pressure sensors are used to measure the pressure of the chamber. For pressures close to the atmospheric pressure (between 10^3 and 10 mbar) a *Leybold-Heraeus Kat. Nr. 160 40* sensor is used. For the range between 10^3 and 10^{-3} mbar, a thermal conductivity based sensor with a constant resistance is utilized. For the medium-high vacuum range (10^{-3} – 10^{-9} mbar), a *Balzers IKR 250* cold cathode gauge sensor is used. This way, all the pressure range can be covered, from atmospheric pressure to high-vacuum.

The system allows us working up to three different gases. In this thesis only two of them have been used: Ar and O₂ from *Praxair* with a purity of 99.999%. These gases are introduced using a mass flow controlled (MFC) from *Bronkhorst*. Also, an additional line for dry Ar is available to fill the chamber before breaking its vacuum.

To load and unload the samples into the chamber, it is necessary to open it to the clean room atmosphere. This could produce a contamination of the targets and the chamber. To reduce this contamination, a constant flow of Ar is maintained while the chamber is open, and also the target is conditioned for at least 60 min away of the substrate before the actual deposition processes.

The substrates are placed on a substrate holder that can hold wafers up to 2 in. in diameter. The target to substrate distance is controlled by a micrometric screw. This height has been kept fixed during this thesis, so the distance between the target and the substrate is 2.5 cm. This is much higher than the mean free path of the plasma species (around 5×10^{-2} cm for Sc and Gd or 3×10^{-1} cm for Ar, according some calculations made using references) [14, 15] in order to prevent surface damage of the semiconductor. The heater can reach temperatures up to 975 °C and is controlled by a *Eurotherm 810* automat, which permits programming complex temperature profiles. The temperature is measured with a thermocouple.

The HPS system used for the high κ dielectric deposition is placed inside the clean room of the *Departamento de Física Aplicada III: Electricidad y Electrónica* from *Universidad Complutense de Madrid*.

2.2 Glow Discharge Optical Spectroscopy (GDOS)

This technique was used to analyze the emissions of the *rf* plasma in order to choose the optimal working conditions. Using this spectroscopy system, the presence of atoms and molecules of different materials can be identified by observing the wavelengths of the emitted light.

A plasma is a gas containing an equal number of positive and negative particles (such as electrons and ions), usually together with neutral gas-atoms [12]. The neutral density is much higher than the charged density. On average, the plasma is electrically neutral. In the electronic industry, the most common plasma is the glow discharge. This is a weakly ionized plasma that is self-sustaining and emits light. This emitted light is due to the excitation or recombination processes of the

electrons of the plasma, atoms, ions or molecules. Since these transitions are between well defined energy levels, depending on the transition and the species, the photon has a particular energy (or wavelength). Thus, by measuring the wavelengths emitted by the glow discharge, information on the species that compose the plasma can be obtained.

Two different spectroscopy systems were used during this thesis with the purpose of analyzing the light emitted by the plasma inside the HPS system. The light was collected through a sapphire window, which is transparent to the measured wavelengths. These systems are briefly described in the next sections.

2.2.1 System I (Monocromator)

In the experimental setup of this first system (shown in Fig. 2.3), a monochromator (model *Jobin Yvon H-25*) is used. This system was used to measure the wavelengths ranging between 280.0 and 550.0 nm with a resolution of 0.1 nm. This monochromator consists in an input and output slits, a system of collimating lenses and a diffraction grating that permits the selection of a determined wavelength. The photons with that wavelength are directed to the photomultiplier. For each incident photon in the photocathode, an electron is emitted. This electron is directed by an electric field to a dynode (fabricated with a material with a high emission of secondary electrons). Thus, for each electron, there are two electrons that are directed to another dynode. These electrons cross several dynodes and, therefore,

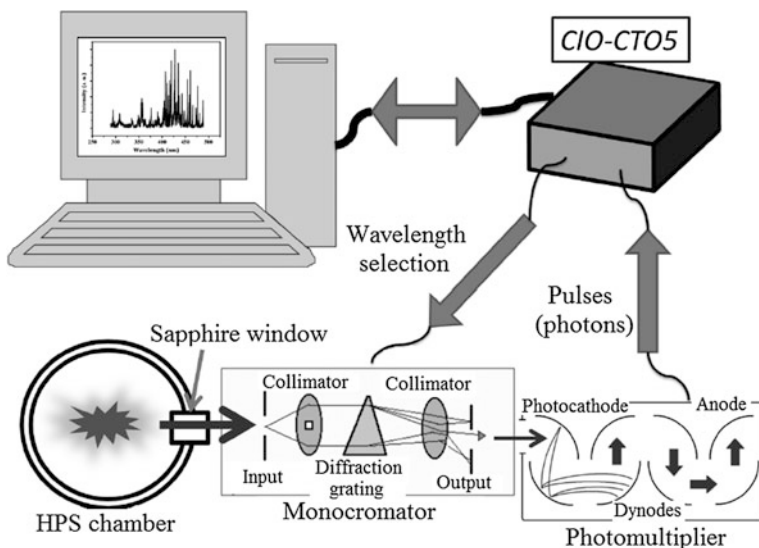


Fig. 2.3 Scheme of the glow discharge optical spectroscopy system I (monochromator)

they are multiplied. In the anode, a pulse signal is generated and, thus, each pulse corresponds to a single photon. This signal is processed by a card *CIO-CTO5* that counts the number of pulses during a determined time. Besides, it sends a signal to the stepper motor that controls the diffraction grating of the monochromator and thus, selects the wavelength. With the help of a *Labview* program designed to control the card, we can determine the wavelength sweep and the scanning results are stored. The typical measurement has a total duration of around 40 min.

2.2.2 System II (Spectrometer)

In this case, instead of mechanically sweeping the wavelength with a monochromator (that is a slow process), a spectrometer is used to provide an instantaneous spectral image from a highly sensitive charge coupled device (CCD) with 2048 pixels from *StellarNet*. Wavelengths ranging from 200.00 to 1000.00 nm can be measured with a resolution of 0.25 nm. The main advantage of this system is that the data can be acquired in ~ 1 s, thus, a real-time analysis of the spectra can be made.

In Fig. 2.4 a schematic of this system is presented. An optical fiber directs the emitted light to the CCD, which is protected inside a rugged metal enclosure, together with the spectrograph. This box is connected to the computer via USB. Using the *SpectraWiz* program, the spectrum is obtained and the data can be saved to analyze the emission lines.

Figure 2.5 represents a GDOS spectrum obtained with the spectrometer, in which the presence of H_2O (a broad band located at wavelengths ranging from 310 to 320 nm) [16] and also peaks corresponding to N_2 (the main peaks at around 336 and 358 nm) [16] can be observed. In this example, these features indicate that there is contamination in the plasma that might affect the deposited film. This way, GDOS can be used as a deposition quality check. In the following chapters, the

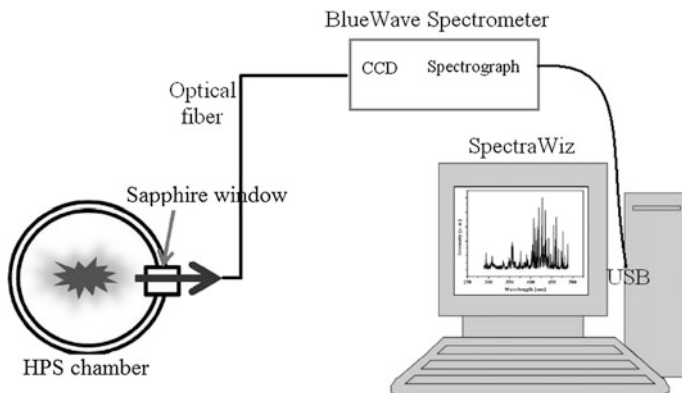
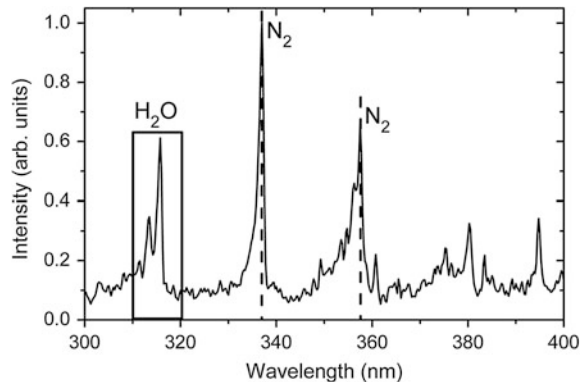


Fig. 2.4 Scheme of the system II (spectrometer) to analyze the GDOS

Fig. 2.5 GDOS emission spectrum of a target sputtered in Ar during the conditioning process. H_2O band and N_2 peaks are marked in the figure. The remaining peaks are related to ArI and ArII



shown spectra will not have these contamination bands. Finally, the remaining peaks present in this spectrum are related to ArI and ArII [17, 18].

2.3 Electron Beam (e-beam) Evaporation

This system was used along this thesis for MIS fabrication with two different goals: to deposit SiO_x as field oxide and to evaporate the metallic electrodes, using Al, Ti or Pt. This technique is another form of PVD, since no chemical reactions are involved. It consists in melting the material to evaporate by the bombardment with a high intensity electron beam. This beam is produced by a heated tungsten filament biased with a high voltage and is directed magnetically to the melt by regulating the current of deflecting coils. Once this beam melts the material, the vapor pressure produces the evaporation of this material [19]. The evaporated atoms travel in straight lines because the system works in high vacuum, until reaching a surface, where they become fixed.

Figure 2.6 is a picture of the e-beam evaporation system used during this thesis, while in Fig. 2.7, a scheme of the system is shown. The samples are glued to the cover upside down with capton film. The chamber reached a base vacuum around 5×10^{-7} mbar due to the help of a turbomolecular pump, *Balzers TPH 330*, supported by a rotary pump, *Balzers DUO 30A*. The tungsten filament, which is protected by a shield, is biased with a high potential of ~ 6 kV. Regulating the current through this filament, the intensity of the e-beam can be controlled. The magnetic field created by the coils deflects the beam and directs it to the material target, which lies within a crucible. This crucible can hold up to four different materials and it is refrigerated by water in order to avoid damages. When the material is melted, the atoms are evaporated through the chamber and a thin film is deposited. The thickness of the evaporated layer can be controlled by means of a quartz crystal: the shift of the resonance frequency of this crystal is proportional to

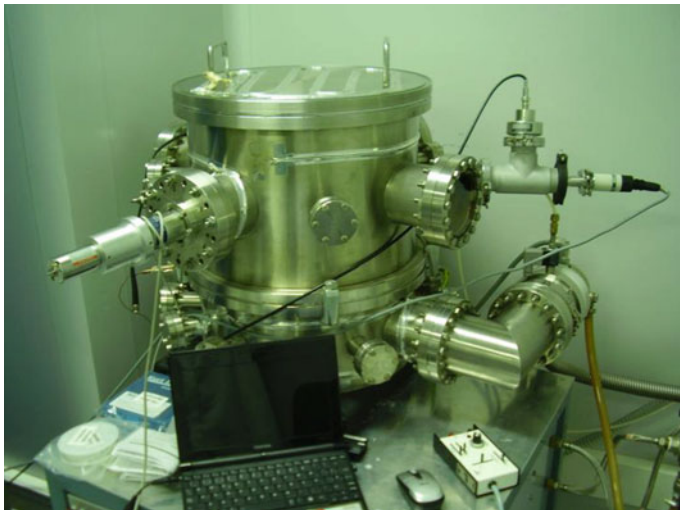
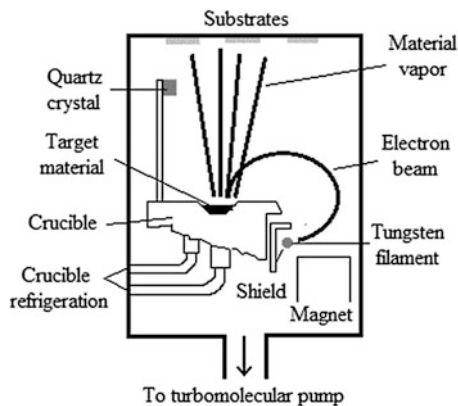


Fig. 2.6 Image of the e-beam evaporation system used in this thesis

Fig. 2.7 Scheme of the electron beam evaporation system



the thickness. The growth rate can be controlled with the beam intensity and it is obtained with a program controlled by a computer. The accuracy is 0.1 nm/s.

The distance between the samples and the material which will be evaporated is around 50 cm. The atoms must reach the surface of the wafers without neither colliding nor scattering. Therefore, the mean free path of particles must be larger than the target-substrates distance. To achieve this, a pressure in the order of 10^{-6} – 10^{-7} mbar is needed during the evaporation. Thus, the pumps are switched on during this process.

Between the crucible and the samples, there is a shutter that can be opened or closed to permit or block the evaporation of the material to the substrates. This

shutter avoided the contamination of the samples in the first stages of the evaporation, when the target melting is performed.

As it was mentioned, two different processes were carried out with the e-beam evaporation system and are listed below.

2.3.1 *SiO_x Acting as Field Oxide*

The reason of performing this process will be further analyzed later in Sect. 2.6. It consists in the evaporation on the semiconductor surface of a thick layer of SiO_x (around 200 nm), obtained from a high purity SiO₂ source (99.999%), purchased from *Test Bourne Super Vac*. The evaporation rate of this process was low to avoid adhesion problems.

2.3.2 *Metallic Electrodes*

For MIS fabrication, different metallic stacks were used. On the one hand, for the Si bottom contact, the whole backside surface of the wafers was covered with ~ 70 nm of Al or a stack formed with 50 nm of Ti/100 nm of Al. On the other hand, for InP substrates, the back electrode was 100 nm of AuGe and 100 nm of Au. In both cases, these metals ensure ohmic contact to n-Si and n-InP wafers, respectively.

To define the top contacts, a lithography process was performed and several electrodes were investigated: pure Al gates (with a thickness around 40–70 nm), a stack formed with a thin Pt layer (less than 10 nm in order to avoid adhesion problems due to stress), capped with Al (to ensure a thick contact with the aim of avoiding the perforation of the metal gate when probing), ~ 25 nm of pure Pt electrodes and different thicknesses of Ti (to explore the scavenging effect) capped with 25 nm of Pt to avoid nitridation or oxidation problems. In the next chapters, the effects of using these different top electrodes will be explained.

The e-beam evaporation system used is placed inside the clean room.

2.4 Lithography Process

This optical process is used to transfer a mask pattern to the surface of the samples using ultraviolet light [20]. This method was used during this thesis to define the shape and size of the metallic top electrodes. To achieve that transfer, a thin film of photoresist, which is a light sensitive material, must be homogeneously deposited over the surface with a spinner (from *Headway Research*). This system is showed in the left hand side of Fig. 2.8. After a soft bake (that removes almost all of the solvents from the photoresist coating), the mask is aligned to the previous processes, and the



Fig. 2.8 Image of the *Headway Research* spinner (in the left hand side) and the *MJB3 UV400* alignment system (in the right hand side), used for the lithography process

photoresist is exposed with high intensity ultraviolet light (produced by a mercury lamp). The system used was a *Karl Suss MJB3 UV400* and it is also presented in Fig. 2.8. This system allows a maximum resolution of $0.8\ \mu\text{m}$. Finally, the image is developed. A post exposure bake (or a hard bake) was necessary in order to harden the photoresist and improve the adhesion of this material to the wafer surface. This step was accomplished before or after the development, depending on the type of the photoresist. Due to the strict cleanliness needed, these processes were performed in a class 1000 clean room.

Two different types of photoresist were used and the procedure followed is explained in the next sections.

2.4.1 Positive Photoresist

In this type of photoresist, the areas exposed to the light become soluble in the developer. Thus, the pattern of the mask is transferred to the substrate. This process was used to open windows in the field oxide deposited over the semiconductor.

A description of this procedure is shown below:

- (a) The photoresist used was the *AZ 4533* from *Microchemicals*. The spin coating was performed at 4000 rpm during 30 s. Prior to this photoresist deposition, it was necessary an adhesion promoter: *TI Prime* also from *Microchemicals*, spinned at 6000 rpm for 30 s.
- (b) The soft bake was carried out at a temperature of $100\ ^\circ\text{C}$ for 3 min.
- (c) A rehydration at room temperature of the photoresist was required in order to allow the photoreaction. The duration of this step was around 30 min.
- (d) After the ultraviolet exposition with a dose of $6\ \text{mW}/\text{cm}^2$, the development was performed for ~ 3 min. The developer used was *MIF 826*, bought from

Microchemicals. Afterwards, the wafers were rinsed in deionized (DI) water and blown with nitrogen to dry the water.

- (e) A hard bake was carried out for 5 min at 130 °C.
- (f) In order to remove the SiO_x from the exposed areas, the samples were immersed in a buffered oxide etching (BOE) solution for 2 min.
- (g) The last step was to remove the photoresist with dimethyl sulfoxide (DMSO) and followed by an isopropyl alcohol (IPA) bath.

BOE, DMSO, and IPA were purchased at *Technic* with the maximum quality available (VLSI grade).

2.4.2 Negative Photoresist

In this case, the behavior of the photoresist with light is the opposite of the former section. Here, the exposition to the light caused that the photoresist becomes polymerized and, therefore, more difficult to dissolve. Thus, the image transferred to the substrate is the negative of the mask image. This process was used to define the metal contacts by a lift-off process.

The steps followed in this process are summarized below:

- (a) The photoresist was the *AZ nLof 2070* from *Microchemicals*. It was spinned at 3000 rpm during 30 s.
- (b) The soft bake was carried out for 1 min at 110 °C.
- (c) After the ultraviolet exposition using a dose of 8 mW/cm², a post exposure bake at 110 °C during 2 min was performed.
- (d) The development was carried out for ~3 min followed by a rinse in DI water and a nitrogen blow to dry the samples.
- (e) After the metal evaporation, the last step was to eliminate the photoresist using DMSO followed by an IPA bath. In this process the metal deposited on the photoresist is lifted-off the surface, leaving only metal on the exposed areas.

2.5 Rapid Thermal Annealing (RTA)

This system was used for two objectives: to reduce the series resistance associated to the backside contact and to passivate the dangling bonds formed at the interface between the high κ and the semiconductor, thus to reduce the interface trap density. Briefly, a RTA system can increase its temperature within seconds (with a fixed ramp and in a controlled atmosphere) up to around 1000 °C, and keeps it stable for a certain period, typically seconds or minutes.

An image of the RTA system used is shown in Fig. 2.9. It is a *RTP-600* model fabricated by *Modular Process Technology*. The maximum achieved temperature is

Fig. 2.9 Image of the RTA system



higher than 1000 °C and it can reach it in only some seconds (less than 1 min). The heating is carried out with several tungsten halogen lamps and the temperature is controlled by a type *K* thermocouple. The chamber is made of quartz and inside it, a graphite susceptor is placed [20].

During this thesis, after the top and bottom electrode evaporation, the samples were annealed in the RTA furnace using a forming gas atmosphere (a high-purity mixture of 90% of N_2 and 10% of H_2). This process was usually performed at different temperatures, from 300 to 450 °C during 20 min. In the following chapters, other temperatures and durations were also used and those details will be mentioned there.

2.6 MIS Fabrication

Two different processes were followed to fabricate MIS devices during this thesis. Both fabrication methods are summarized below:

2.6.1 Process Without Field Oxide (FOX)

This first procedure was the simplest method to fabricate MIS capacitors. This fabrication method was used to produce devices for process development with minimal manufacturing complexity. It was employed for thick dielectric films where the leakage was not very significant.

The process consisted in the definition of the top metallic electrodes directly on the dielectric (deposited previously by means of HPS) with a negative lithography

process (explained in Sect. 2.4.2). After the metal e-beam evaporation and the lift-off of the top electrodes, the devices were finished with the e-beam evaporation of the backside contact. Figure 2.10 shows one dice of the lithography mask employed. The complete mask consists in the repetition of the dice several times to cover the complete wafer surface. The defined squares have sizes ranging from $630 \times 630 \mu\text{m}^2$ to $50 \times 50 \mu\text{m}^2$.

It was observed that, especially for thin dielectrics, the pressure applied by the needles of the probe station on the metallic contacts during the electrical characterization influenced significantly the obtained curves. In many cases, the leakage current density as a function of the gate voltage ($J-V_{\text{gate}}$) measured applying high pressure to the needles was several orders of magnitude higher than the $J-V_{\text{gate}}$ curve measured with low pressure. Figure 2.11 presents two $J-V_{\text{gate}}$ characteristics of the same sample, with the only difference of the applied pressure to the needles during the measurement. More than four orders of magnitude between both measurements could be seen there. This could be explained as follow: due to the small thickness of the dielectric used (around 5–6 nm), if the pressure applied to the needles is high enough to pierce the dielectric, then the dielectric is permanently damaged. However, for moderate leakage, the capacitance measurement is only slightly affected, thus this process can be used for preliminary process assessment. For accurate electrical characterization, other process must be used, more mechanically robust at the cost of process complexity.

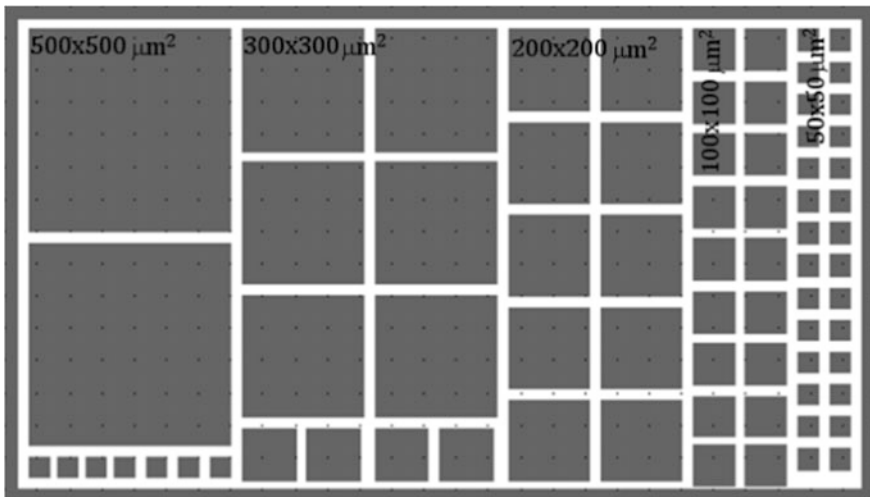
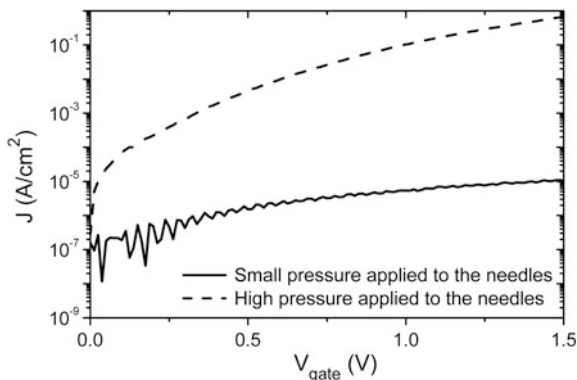


Fig. 2.10 Dice of the lithography mask of the process without field oxide to define the top electrodes

Fig. 2.11 J - V_{gate} characteristics for the same sample measured applying more or less pressure to the needles



2.6.2 Process with FOX

This fabrication method was more complex because it included a thick SiO_x film acting as field oxide in order to avoid the degradation observed in the former paragraph. The introduction of contacting pads (little contacts attached to the devices and grown over a thick insulator layer) allows measuring the electrical characteristics without damaging the high κ dielectric with the needles.

In this process, once the wafers were cleaned, a thick SiO_x used as insulator layer was grown with two different methods: SiO_2 obtained with a dry thermal oxidation or SiO_x deposited by e-beam evaporation.

In the first case, the FOX was grown with a dry oxidation process on the Si wafers. The oxidation gas was pure O_2 without H_2O (to guarantee the maximum oxide quality). This dry oxidation was performed at a temperature of 1100°C for almost 3 h, which provided a SiO_2 layer ~ 200 nm thick. This process was carried out by Prof. Enrique Iborra from the *departamento de Ingeniería Electrónica* of *E. T.S.I. de Telecomunicación* from *Universidad Politécnica de Madrid*. The main advantage of this process is the high quality of the insulator film grown, but it is only possible for Si substrates. However, for the InP wafers, this oxidation process was not possible, thus other alternative must be explored. For that reason, the SiO_x was obtained by e-beam evaporation.

The results obtained by both field oxides were analyzed and no differences were observed between them. Therefore, for simplicity and to reduce thermal budget, most devices were fabricated with evaporated field oxide.

To define the SiO_x windows, a positive lithography process (explained in Sect. 2.4.1) was performed, using the mask of the left hand side of Fig. 2.12. The opened windows had areas from $700 \times 700 \mu\text{m}^2$ to $50 \times 50 \mu\text{m}^2$. After the HPS deposition, a second lithography process was carried out, in this case, using negative photoresist and the mask presented in the right hand side of Fig. 2.12. This mask included the pads, little devices placed over the thick SiO_x film with a size ranging from $150 \times 150 \mu\text{m}^2$ to $50 \times 50 \mu\text{m}^2$. The top metal contacts were

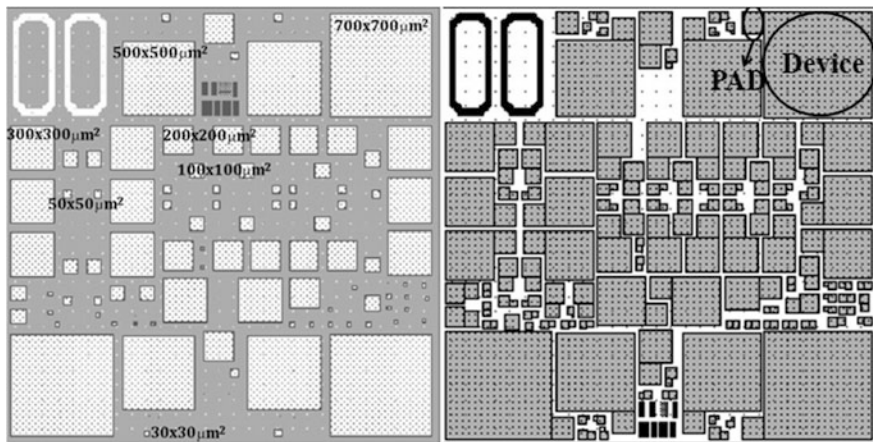


Fig. 2.12 Lithography mask used for the process with field oxide. In the *left hand side* is the mask used for opening the SiO_x windows and in the *right hand side* is for defining the top contacts. A pad and a device are marked in the figure

e-beam evaporated and, afterwards, the lift-off was performed. MIS devices were finished after the evaporation of the bottom contact in the whole backside of the wafer.

For both processes, a forming gas anneal (FGA) performed in the RTA furnace was carried out to improve the backside electrode and to passivate the interface traps.

In Fig. 2.13 it is presented the cross-sections of two MIS devices fabricated without FOX and with FOX and pad, following the steps of Sects. 2.6.1 and 2.6.2, respectively. The total capacitance of the MIS capacitor of Fig. 2.13b is the device capacitance (the same that in Fig. 2.13a) and the pad capacitance. Thus:

$$C_{total} = C_{device} + C_{pad} \quad (2.1)$$

Therefore, the C_{pad} should be much lower than the C_{device} in order to ensure that this contribution does not affect the total capacitance. The C_{pad} is around 9×10^{-12} F, while the measured capacitance is $\sim 4 \times 10^{-10}$ F, more than two

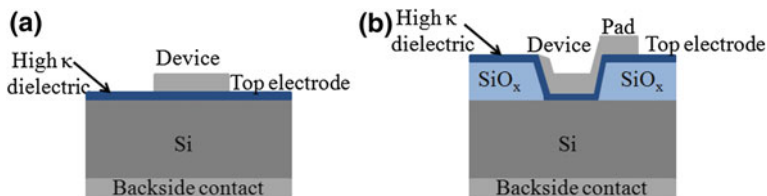


Fig. 2.13 Cross-section of MIS devices **a** without FOX and **b** with FOX (and pad) fabricated following the steps from Sects. 6.1 and 6.2, respectively

orders of magnitude higher than the C_{pad} . Hence, including the pad produces a small capacitance increase of around 2%, which is irrelevant for device characterization.

2.7 Substrates

2.7.1 Semiconductor Materials

The semiconductor materials used during this thesis for growing the MIS structures were Si and InP wafers. Both kinds of semiconductors were n-type, with a diameter of 2 in. (~ 5 cm), a thickness of 300 μm and (100) surface orientation. The InP wafers were unintentionally doped but the fabrication process led to n-type behavior.

2.7.1.1 Si Wafers

For Si, two different types of substrates were selected depending on the characterization technique. On the one hand, for optical measurements, double side polished (DSP) and high resistivity (from 1100 to 3000 $\Omega\text{ cm}$) wafers were used. These samples had low doping density with the aim of avoiding the photon absorption by free charge carriers. On the other hand, for electrical characterization, MIS devices were grown on single side polished (SSP) wafers with a resistivity between 1.5 and 5 $\Omega\text{ cm}$. The reason of using these values of the resistivity was to avoid a high series resistance that could cause distortions during the electrical measurements.

Besides, Si wafers used were grown by two different methods: float zone (FZ) [21] that provided a high purity Si with low density of defects and Czochralski (CZ) [22] which is now the most dominant method for growing Si crystals [23]. Both types of substrates were fabricated by the *Institute of Electronic Materials Technology, ITME*. MIS devices grown on Si wafers fabricated with the FZ and CZ techniques were measured and no significant differences were obtained in the electrical characteristics.

2.7.1.2 InP Substrates

In the case of InP, only one kind of wafers were used because only MIS devices were fabricated with this substrate. Thus, SSP samples were utilized with a resistivity ranging from 1 to 5 $\Omega\text{ cm}$ and fabricated by *InPACT*.

2.7.2 Substrate Surface Cleaning

The electrical properties of the dielectric/semiconductor interface can be strongly affected by the morphological structure and chemical integrity of the semiconductor surface before dielectric deposition [24]. For that reason, prior to the deposition, it was necessary and crucial a proper cleaning of the semiconductor surface in order to remove contamination and defects and to obtain a high quality interface. Since in this thesis Si and InP wafers were used, two different cleaning procedures were carried out for each semiconductor.

2.7.2.1 Si Wafers

The Si wafers were cleaned following the standard RCA (*Radio Corporation of America*) procedure [25]. The steps for this cleaning method are:

- (a) An immersion in DMSO followed by an IPA bath. Both processes were carried out at room temperature for some minutes. This step removes the organic contaminants.
- (b) Standard clean 1 (SC1): the wafers were immersed in a solution of $\text{H}_2\text{O}:\text{H}_2\text{O}_2:\text{NH}_4\text{OH}$ (5:1:1) for 10 min at a temperature between 70 and 80 °C. This solution oxidizes the Si surface and dissolves the growing oxide, removing different organic contaminants and metals such as Na, K, Al and Cu.
- (c) DI water rinse (with a resistivity of 18.2 M Ω cm) to reduce wafer temperature and remove residues.
- (d) $\text{HF}:\text{H}_2\text{O}$ (1:50) dip for 30 s at room temperature to remove the thin native oxide film formed during the SC1 step together with the contaminants trapped.
- (e) Standard clean 2 (SC2): samples were immersed in a dissolution of $\text{H}_2\text{O}:\text{H}_2\text{O}_2:\text{HCl}$ (6:1:1) at 70–80 °C for 10 min. Again, this solution forms a native oxide by the oxidation of the Si surface and traps the remaining heavy metallic (ionic) contaminants.
- (f) The last step consists on dipping the wafers in DI water and a nitrogen blow.

Just before loading the samples into the chamber, the Si substrates were immersed in an $\text{H}_2\text{O}:\text{HF}$ (1:50) solution for 30 s, in order to remove the native oxide grown during the SC2 process, and then a DI water dip. This step provided a Si surface with a hydrogen passivation (and the surface becomes hydrophobic). It is important to perform this step as fast as possible to minimize the time that the sample is exposed to the atmosphere. Additionally, once the samples were inside the HPS system, the substrates were heated at 500 °C for 5 min in vacuum with the aim of surface desorption and to improve the cleaning of the chamber after exposing it to the atmosphere.

2.7.2.2 InP Wafers

These type of substrates were cleaned with a 10% diluted iodic acid solution (HIO_3 ; H_2O) during 1 min and followed by a dip in DI water for rinsing [26, 27]. With this step, the first InP layers were removed and, therefore, the surface contamination was eliminated [28].

Besides, before the introduction of these samples into the HPS system, the same cleaning carried out for the Si wafers (HF-cleaning) were performed for 30 s in order to remove the native oxides and then the samples were washed in DI water. In this case, no heating of the samples in vacuum was carried out to avoid In diffusion and surface degradation.

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