

Preface

This book contains extended and revised versions of the highest quality papers selected from those presented during the 24th IFIP/IEEE WG10.5 International Conference on Very Large Scale Integration (VLSI-SoC), a global System-on-Chip design and CAD conference. The 24th conference was held at the Park Inn in the Radisson Meriton Conference and Spa Hotel in Tallinn, Estonia, September 26–28, 2016. Previous conferences took place in Edinburgh, Scotland (1981); Trondheim, Norway (1983); Tokyo, Japan (1985); Vancouver, Canada (1987); Munich, Germany (1989); Edinburgh, Scotland (1991); Grenoble, France (1993); Chiba, Japan (1995); Gramado, Brazil (1997); Lisbon, Portugal (1997); Montpellier, France (2001); Darmstadt, Germany (2003); Perth, Australia (2005); Nice, France (2006); Atlanta, USA (2007); Rhodes, Greece (2008); Florianopolis, Brazil (2009); Madrid, Spain (2010); Kowloon, Hong Kong, China (2011); Santa Cruz, USA (2012); Istanbul, Turkey (2013); Playa del Carmen, Mexico (2014); and Daejeon, South Korea (2015).

The purpose of this conference, which was sponsored by IFIP TC 10 Working Group 10.5, the IEEE Council on Electronic Design Automation (CEDA), and by IEEE Circuits and Systems Society, with the cooperation of ACM SIGDA, is to provide a forum for the presentation and discussion of the latest scientific and industrial results and developments as well as future trends in the field of System-on-Chip (SoC) design, considering the challenges of modern nano-scaled state-of-the-art and future manufacturing technologies. The down-scaling of the feature sizes of modern semiconductor technologies imposes numerous new challenges on physical and system-level design of SoCs. Increasing reliability challenges demand new concepts in fault-tolerance and testing. While classically, based on the bathtub fault rate model, testing has been applied after manufacturing only, in the nano-era, built-in testing concepts have to monitor the system's health status during its lifetime. Sophisticated design and architectural measures are required to cope with wear-out, and system lifetime health management and active fault-resilience are also required. VLSI-SoC addresses these future challenges and provides an internationally acknowledged platform for scientific contribution and industrial progress within this field.

For VLSI-SoC 2016, 36 papers out of 93 submissions were selected for presentation at the conference.

Out of these 36 full papers presented at the conference, 11 papers were chosen by a Selection Committee to have an extended and revised version included in this book. The selection process of these papers considered the evaluation scores during the review process as well as the review forms provided by members of the Technical Program Committee and session chairs as a result of the presentations.

The papers in this proceedings volume have authors from Belgium, China, France, Germany, Hong Kong, Iran, Israel, Italy, Singapore, and the USA. The Technical Program Committee for the regular tracks comprised 95 members from 25 countries.

VLSI-SoC 2016 was the culmination of the work of many dedicated volunteers: paper authors, reviewers, session chairs, invited speakers, and various committee chairs. We thank them all for their contribution.

This book is intended for the VLSI community, mainly those persons who did not have the chance to attend the conference. We hope you enjoy reading this book and that you find it useful in your professional life and for the development of the VLSI community as a whole.

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VLSI-SoC: System-on-Chip in the Nanoscale Era -

Design, Verification and Reliability

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Papers

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