

# Preface

The advent of cheap electronic sensors, cloud computing, IoT, smart devices, mobile computing platforms, driverless cars, drones, etc., has led to generation of enormous amounts of data. Some characteristics central to this big data are its asynchronous and non-standardized nature. The vast amount of data by itself is of less value; however, the ability to effectively and efficiently process it in real-time leading to meaningful patterns, trends, and interpretation is the real treasure trove.

Several upcoming unconventional (non-Von Neumann) computing paradigms, where memory (storage) and processing are not isolated tasks in themselves or rather *memory is intelligent*, offer promising capabilities to this problem of massive non-synchronous, non-standardized data treatment. Techniques such as software artificial neural networks (ANNs), artificial intelligence (AI), and machine learning (ML) have been proving their mettle in fields as diverse as autonomous navigation, to robotics to analytics since a while. However the full potential of these computing paradigms can only be realized when they are directly implemented on dedicated low-power, compact, reconfigurable, programming-free hardware.

When it comes to dedicated hardware, some first contenders are CMOS-ASICs, DSPs, GPUs, and FPGAs. However, most of these implementations rely on a layer of digital (Von Neumann modified) abstraction even if some grassroots computing arises out of purely analog traits.

To this end, over the last few years there has been a lot of activity across research groups postulating efficient hybrid CMOS-“nanodevice” computing hardware architectures. The “nanodevice” in these hybrid systems cover a vast range of technologies such as organic nanoparticle transistors (NOMFETs), carbon nanotubes (CNTs), atomic nanogap switches, silicon thin-film transistors (TFTs), magnetic spin-based devices, to families of emerging non-volatile resistive memory including phase-change memory (PCM), conductive bridge memory (CBRAM or PMC), metal-oxide-based memory (OxRAM), theoretical memristor, and so on, to name a few.

This book is a selective collection of recent works from some of the leading research groups across the globe working to achieve dedicated hybrid (CMOS + nanodevice) hardware for neuromorphic computing. The book in its present form is

certainly not exhaustive of all the research in the field, but is an attempt to get started; bringing valuable and diverse approaches on the subject matter under one roof.

While curating the valuable contributions for the present edition, special attention was paid to create a right mix of conceptual (primarily simulation-based studies) and experimental (technology-based studies) works.

The book may be used as teaching material for undergraduate and postgraduate course work, or a focused read for advanced researchers working in the domain and related areas.

Key building blocks for neuromorphic systems would comprise of hardware implementations of—(i) the *neuron* or *neuron-like* functionality and (ii) the *synapse* or *synapse-like* functionality, where both are powered by relevant *learning rules*.

Chapter “[Hardware Spiking Artificial Neurons, Their Response Function, and Noises](#),” by researchers at *Korea Institute of Science and Technology*, provides an overview of silicon hardware implementation of the first essential block of neuromorphic systems, i.e., the *neuron*.

Chapter “[Synaptic Plasticity with Memristive Nanodevices](#),” by researchers at *University of Lille—France*, offers the reader a strong overview or primer on different techniques of emulating forms of synaptic plasticity using various memristive nanodevices.

Chapter “[Neuromemristive Systems: A Circuit Design Perspective](#),” by researchers at *University of Rochester—USA*, focuses on hybrid circuit design perspectives of emerging neuromemristive architectures and systems.

Chapter “[Memristor-Based Platforms: A Comparison Between Continuous-Time and Discrete-Time Cellular Neural Networks](#),” by researchers at *Politecnico di Torino—Italy*, focuses on analysis and comparison of memristive continuous-time and discrete-time cellular neural networks.

Chapter “[Reinterpretation of Magnetic Tunnel Junctions as Stochastic Memristive Devices](#),” by researchers at *University Paris-Sud—France*, discusses how spin-transfer torque magnetic random access memory (STT-MRAM) can be used to realize stochastic neuroinspired hardware architectures.

Chapter “[Multiple Binary OxRAMs as Synapses for Convolutional Neural Networks](#),” by researchers at *French Alternative Energies and Atomic Energy Commission (CEA-LETI and CEA-LIST)*, presents the implementation of convolutional neural networks exploiting metal-oxide-based OxRAM technology.

Chapter “[Nonvolatile Memory Crossbar Arrays for Non-von Neumann Computing](#),” which is a joint effort of researchers at *EPFL—Switzerland*, *IBM Almaden—USA*, and *Pohang University—Korea*, presents neuromorphic implementations that utilize chalcogenide-based phase-change memory (PCM), and non-filamentary RRAM (PCMO)-based nanodevices.

Chapter “[Novel Biomimetic Si Devices for Neuromorphic Computing Architecture](#),” by researchers at *Indian Institute of Technology Bombay*, presents novel SiGe-based nanodevices for neuron and synaptic implementations inside the neuromorphic hardware architectures.

Chapter “[Exploiting Variability in Resistive Memory Devices for Cognitive Systems](#),” by researchers at *Indian Institute of Technology—Delhi*, presents implementation of extreme learning machines (ELM) and restricted Boltzmann machines (RBM) using RRAM nanodevices.

Chapter “[Theoretical Analysis of Spike-Timing-Dependent Plasticity Learning with Memristive Devices](#),” by researchers at *University Paris-Sud—France*, and *Alternative Energies and Atomic Energy Commission (CEA-LIST)*, presents the underlying theoretical framework behind STDP-based learning and its equiv

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