

Preface

In the present decade, the complexity of the ASIC and FPGA design has grown rapidly. Due to that there is need of the intelligent and complex devices, and hence the FPGA prototyping area has evolved during this decade.

Major FPGA vendors such as XILINX and Altera (Intel FPGA) have come up with the complex FPGAs which are required for design and realization of the system on chip (SOC). During this decade, the era of miniaturization has lot many challenges. The major challenges are to design and deliver the intelligent products for lesser cost, high speed, less area, and less power.

Under such circumstances for the idea or product feasibility, the complex FPGAs are used and the complexity of FPGA architecture has grown in the past decade. Even the multiple FPGA designs are used to validate the complex SOC's. For easy understanding of the FPGA designs and ASIC prototyping using FPGAs, this book is organized. This book covers the design for the lower gate count to higher gate count designs. Even this book is written in such a way that it can give information about the VHDL, synthesis, FPGAs, and ASIC prototyping.

Chapter 1 of this book discusses the evolution of the logic design, need of HDL, and differences between the VHDL and other higher level languages, and even this chapter describes about the different modeling styles using VHDL.

Chapter 2 of this book describes about the basic combinational elements and their use in the design. Even this chapter describes how to write synthesizable RTL using the VHDL constructs. This chapter is useful for the beginners to understand about the basic VHDL constructs and the synthesis outcome of few low gate count designs.

Chapter 3 discusses the key VHDL constructs such as processes, signals, and variables, when else, with select, if-then-else and case. Even this chapter covers the practical scenarios and use of these constructs.

Chapter 4 describes the how to write an efficient RTL using VHDL. Even this chapter covers the design for the combinational logic such as multibit adders, multiplexers, decoders, and encoders. The synthesis for the RTL design using VHDL is covered with the detailed explanation and practical scenarios.

Chapter 5 covers the sequential design scenarios and the RTL using VHDL for the latches and flip-flops. Even this chapter covers the BCD counters, binary counters, gray counters, ring counters, Johnson counters and the RTL design and synthesis for the same. This chapter has information about the timing parameters and timing analysis for the synchronous sequential designs. This chapter even gives information about the basics of asynchronous and multiple clock domain designs and the issues like metastability and how to overcome those during design cycle.

Chapter 6 covers the PLD-based designs and the detail practical-oriented examples and scenarios for the design using SPLDs, CPLDs, and FPGAs. This chapter covers the XILINX and ALTERA (Intel) FPGA architectures and their use in the design and prototyping. The vendor-specific design guidelines are covered in this chapter.

Chapter 7 covers the VHDL constructs and the use of VHDL for the verification and simulation of the design. This chapter is useful to understand the test benches and how to simulate the design for early detection of bugs. Even this chapter covers the practical issues in the design verification using practical scenarios and examples.

Chapter 8 covers the design and coding guidelines for the PLD-based designs. How to use the VHDL for the efficient design is explained in detail with the practical scenarios and synthesizable VHDL constructs. This chapter covers techniques such as grouping, parallel and concurrent logic, logic duplications, and resource sharing. Even this chapter covers the low-power basics as clock gating and clock enabling.

Chapter 9 discusses the finite state machines (FSMs) using the VHDL. The Moore and Mealy machines and their use to code the sequence detectors and counters are described in this chapter. Even the FSM synthesis issues and how to improve the design performance are discussed with the practical scenarios. Even this chapter covers the FSM synthesis guidelines and FSM optimization techniques used while prototyping ASICs using the complex FPGAs.

Chapter 10 covers the complex designs such as multipliers, barrel shifters, arbiters and the processor logic as ALU, and the other basic protocols. This chapter is useful to understand the synthesis issues in the complex designs and how to overcome those using the techniques described in Chap. 7.

Chapter 11 covers VIVADO based design flow and case study using VIVADO for the design implementation. The case study of FIFO is covered in this chapter.

Chapters 1–11 are organized in such a way that it covers the small gate count RTL using VHDL to the complex design using VHDL with the meaningful scenarios. This book is useful for the beginners, RTL design engineers, and professionals. I hope that this book can give you the excellent understanding of VHDL constructs and use of VHDL in ASIC prototyping!

PLD Based Design with VHDL

RTL Design, Synthesis and Implementation

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2017, XXI, 423 p. 246 illus., Hardcover

ISBN: 978-981-10-3294-3