

Chapter 2

c-Si Solar Cells: Physics and Technology

This chapter presents the main stream technology of c-Si solar cells. It explores development in design and technology of the c-Si solar cells from traditional to advanced device architecture. It highlights the historical development in cell design and technology along with the technological approach which are being researched for next generation c-Si solar cells. Starting from most general cell architecture to complex architecture design, like HIT and PERL cells, has been covered. In this chapter, both mono- as well as multi c-Si wafer-based cells and their development have been discussed along with the manufacturing process sequence which is widely followed. Some basics on solar cell performance and corresponding cell performance tracking parameters like open circuit voltage, short circuit current, maximum power point, FF, Efficiency, EQE and IQE, etc., and their interdependence has also been discussed. Toward the end of the chapter, International Technology Roadmap for Photovoltaic (ITRPV) has been introduced. Also, discussion on next-generation c-Si wafer-based solar cells technology has been done highlighting the complications and importance of study on advanced light trapping in such structures.

2.1 Overview of c-Si Solar Cells

First c-Si solar cell was made in 1941. Back then the c-Si solar cell was merely 1% efficient (Green 2009). The c-Si-based solar cell technology has now reached 25% efficiency mark and even crossed this mark (Green et al. 2015). This development has come due to continuous efforts to make solar cell design, material quality, passivation technologies, and light tapping architectures better and better. The cost reduction with better efficiency has been the focus of the c-Si-based solar cell technology development to make solar cells more cost-effective and affordable to the masses. Today, c-Si solar cell-based modules; mainly mono c-Si and multi c-Si, shares 85–90% global market (Tanaka 2010). The first solar cell was fabricated

using mono c-Si wafers, however, multi c-Si-based solar cell technology, as the cheaper and available alternative, came into existence in 1974 (Treble 1998). Improvement in slicing technology and reduced kerf loss leads to manufacturing of solar cell on 180 μm wafers compared to 400 μm thickness wafers used in early years. The cost of c-Si-based cells has been declining over the years as the technology becoming more mature (see Fig. 2.1). This is also in sync with reduction in wafer prices. The processing cost of cell manufacturing was further reduced after introduction of screen printing technology for contacts in 1975. The cell size also played a role in reduction in cell prices. In the beginning (around 1970s), the industrial cell size used to be mono c-Si wafer-based 50 mm circular cells (Treble 1998). These days, 125 and 156 mm pseudosquare cells are available in the market. Even up to 300 mm multi c-Si-based cells has also been produced by some manufacturers (Treble 1998).

Figure 2.1 shows the trend of annual fall in prices of multi c-Si based solar cells and wafer in the recent years in USD/W_p.

Note that the multi c-Si-based solar cells are relatively less efficient than the mono c-Si-based cell, however, the lower processing cost of multi c-Si-based cells makes it more preferable. In 1985, the best multi c-Si cell efficiency was in the range of 15–16%, whereas mono c-Si-based cell were shown to have efficiency about 19%. As per recent reports, best multi c-Si-based cell have reached 21.3% efficiency mark and mono c-Si-based cell at 25% mark having large area (Green et al. 2015; NREL 2016). Figure 2.2 shows research cell or laboratory cell efficiency improvements of mono- and multi c-Si-based cells over the years.

Though the best efficiency in labs has crossed the 25% mark, the industrial cells are in 21–22% efficiency range (Green et al. 2015). Continuous efforts are being given to make this technology more efficient and affordable by researching and implementing the noble technologies for wafer manufacturing and cell processing.

Fig. 2.1 Price trend of multi c-Si wafer and cells in recent years (after Ref. (www.itrpv.net/Reports/Downloads/2014/2014))

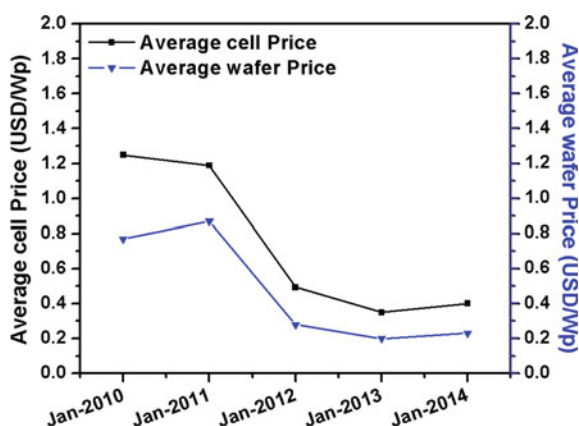
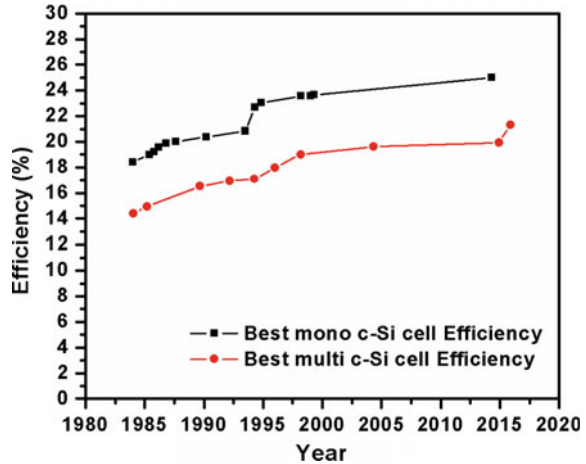


Fig. 2.2 Improvement trend in research cell efficiency of mono- and multi c-Si-based cells over the years (after Ref. (NREL 2016))



2.2 c-Si Solar Cell: Design and Technology

2.2.1 Classification of c-Si-Based Solar Cells

c-Si solar cells are mainly divided into two categories, e.g., mono c-Si solar cell and multi-crystalline Si solar cells. This classification is based on the type of wafer used in fabrication of the cell.

i. Mono c-Si solar cell:

In mono c-Si solar cells, mono-crystalline wafers are used. These wafers have well-arranged atoms in crystallographic structure which is free from any grain boundaries. Figure 2.3a shows the plain view of a typical mono c-Si wafer and Fig. 2.3b shows symbolic microscopic view of wafer where atoms of Si are arranged in periodic manner and connected with each with covalent bond. Czochralski (Cz) technique and float zone (FZ) techniques are most commonly used for manufacturing mono c-Si ingots from high-purity polycrystalline Si. The typical manufactured mono c-Si wafers have circular shape due to technicality involved in manufacturing of ingots which comes out in cylindrical shape (see Fig. 2.4a). But for economic benefits in making PV modules, the wafers are cut from ingots such that it gets pseudosquare shape, as much as possible. While making the mono c-Si ingots, dopants are added to make it either p-type (mainly B (Boron) is used as dopants) or n-type (mainly P (Phosphorus) is used as dopant). Both p-type and n-type mono c-Si wafers are used for making solar cells.

ii. Multi-/poly-crystalline solar cells:

In multi/poly c-Si solar cells, multi-crystalline wafers are used. These wafers have many well-arranged atoms in crystallographic structure; crystal size typically varies in the range from mm to cm, separated by grain boundaries. Figure 2.3c shows the

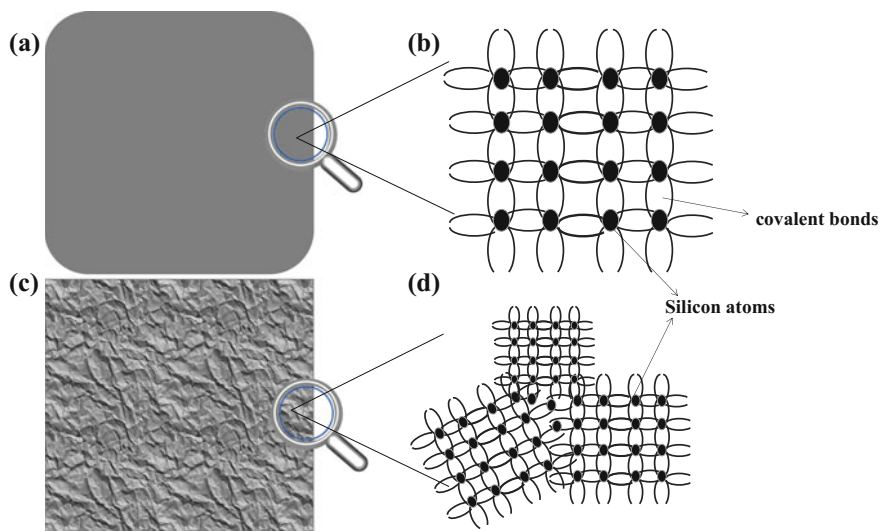


Fig. 2.3 **a** Plain view of a mono c-Si wafer; **b** symbolic microscope view for atomic arrangements in mono c-Si wafer; **c** plain view of a multi/poly c-Si wafer; **d** symbolic microscope view for atomic arrangements in multi c-Si wafer

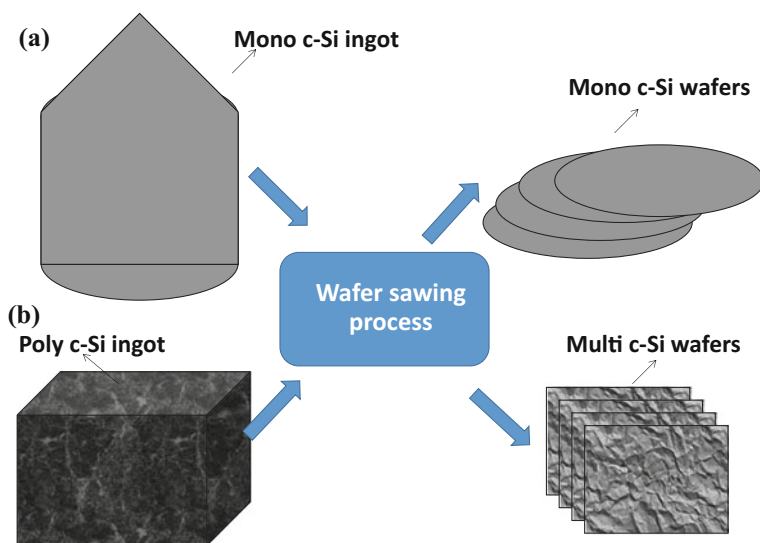


Fig. 2.4 Schematic of **a** Mono c-Si ingots and circular wafers after sawing process; **b** multi c-Si ingots and rectangular wafers after sawing process

Figure 2.3c shows a typical multi/poly c-Si wafer and Fig. 2.3d shows symbolic microscopic view of wafer where atoms of Si are arranged in periodic manner in small grain sizes separated by grains of different sizes. Due to presence of grains, the wafer looks nonuniform in color across the wafer and grain boundaries can be easily distinguished. The method for making purified poly-Si for multi c-Si wafers is the same as that of mono c-Si wafers; however, conversion of poly-Si into crystalline Si is done by directional solidification method. In this method, it is possible to make square-shaped ingots and hence square and rectangular wafers (see Fig. 2.4b) which are beneficial when manufacturing PV modules. Just like mono c-Si wafers, the multi c-Si wafers can also be p-type and n-type. The process used for manufacturing the poly/multi c-Si wafers are simpler and cost-effective, however, the efficiency achieved in these types of wafer-based cells are typically 1–2% lower than that of mono c-Si wafer-based cells produced with the same process.

Figure 2.5a shows a typical 5-inch mono c-Si solar cell and Fig. 2.5b shows a typical 5-inch multi c-Si solar cells. Clear difference can be seen from surface and edges, mainly corners.

2.2.2 Architecture of c-Si Solar Cells

A typical c-Si solar cell has a p-type or n-type base which is also known as base or substrate and is moderately doped with impurity (B or P respectively) doping concentration of $\sim 10^{15}$ – $10^{16}/\text{cm}^3$. The junction (also called Emitter) is formed by highly doped region (impurity concentration $\sim 10^{20}/\text{cm}^3$). The Emitter is of n-type for p-type base and p-type for n-type base. In order to reduce the reflection from the surface there is textured surface with anti-reflection coating, which also acts as

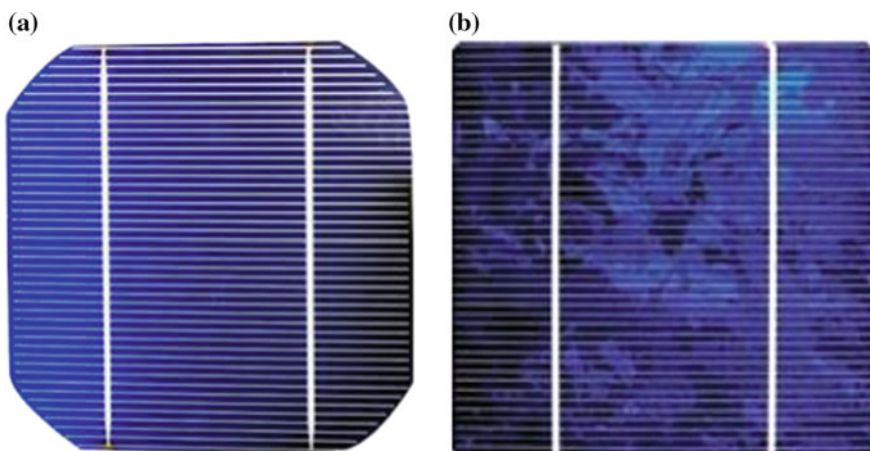


Fig. 2.5 Front view camera image of a typical **a** mono c-Si solar cell; **b** multi c-Si solar cell

surface passivation layer. And, then there are metal contacts at the front and at the rear side.

Figure 2.6a shows schematic of a typical p-type c-Si solar cell and Fig. 2.6b shows schematic of a typical n-type c-Si solar cell. In p-type c-Si solar cell as in Fig. 2.6a, base is p-type and emitter is made by heavy doping of pentavalent dopant usually phosphorus which form n^+ region and makes p-n junction. The p-n junction helps to separate the charge carriers (electrons (e) and holes (h)) which are generated when light is absorbed in the base. Cell surface is textured to enhance the light absorption in solar cell. Dielectric coating is done to passivate the dangling bond present at the surface of Si. If the surface is not passivated, the dangling bonds would act as recombination centers for photogenerated charge carriers and would reduce the electrical performance of the cell. The dielectric, usually silicon nitride (SiN_x) or silicon oxide (SiO_x)/silicon nitride (SiN_x) stack, also act as anti-reflection coating. For back contact usually Aluminum (Al) is used. When cell is annealed to form proper contact, Al reacts with Si and form p^+ region at based which serves the purpose of passivation at back surface, known as back surface field passivation (BSF). For front contact, usually silver (Ag) is used to make fingers and bus bars (see Fig. 2.5).

Similarly in n-type cells (Fig. 2.6b), base is n-type and emitter is made by doping trivalent dopant usually boron which form p^+ region. In this case also surface is textured to enhance the light absorption and dielectric coating (SiN_x or $\text{SiO}_x/\text{SiN}_x$ or aluminum oxide (Al_2O_3)) is done to passivate the dangling bond present at the surface which also acts as anti-reflection coating. For back contact, usually Aluminum (Al) is used here also. However, for BSF in this case, phosphorus doping is preferred to form n^+ region which acts as BSF. For front contact, usually Al or Ag is used to make fingers and bus bars. Please note that the architecture shown here for n-type solar cell is more generic. There are many other possible architectures which are followed.

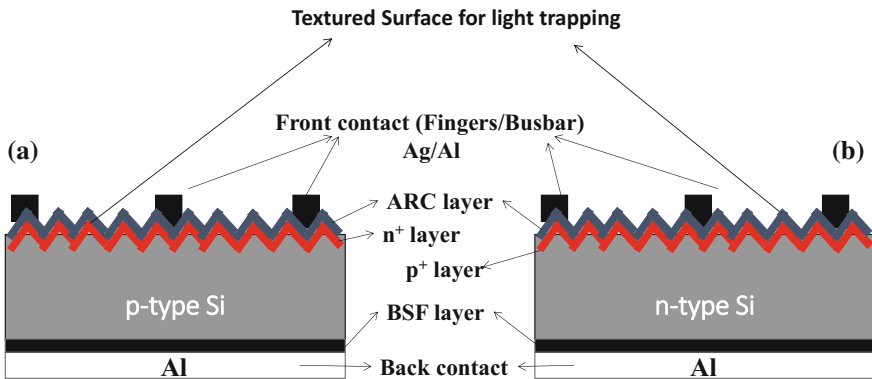


Fig. 2.6 Schematic of a typical **a** p-type c-Si solar cell; **b** n-type c-Si solar cell

2.2.3 Historical Development

The early c-Si-based p-n junction solar cell came into existence in 1941 at Bell Laboratory by Russel Ohl (Green 2002). The reported solar cell has “grown-in” junction which is formed by impurity segregation in slowly recrystallized silicon melts. Figure 2.7 shows schematic of a typical “grown-in” p-n junction solar cell reported in 1941. The efficiency of such cell was less than 1% (Green 2009).

The history of modern c-Si solar cell starts from 1954, when Fuller, Pearson, and Chaplin found that a diffuse p-n junction generated current when it is exposed to light (Treble 1998). The cell analysis then indicated 4.5% efficiency (Treble 1998). In 1956, a team led by Dr. Morton Prince at Hoffman Electronics of Evanston started commercial production of p/n junction cell which was 7% efficient (Treble 1998). The cell size was 1 cm × 2 cm and had single positive strip contact. The schematic of the cell is shown in Fig. 2.8. The cell also had silicon oxide (SiO_x) coating at the top.

In the beginning, the cell cost was very high and use for terrestrial application was not practically encouraging. After first public trial of silicon solar cell in 1956 in Bell rural carrier system, the next application is found in Vanguard I (first solar-powered satellite launched in 1958) to power 5 mW back-up transmitter (Treble 1998). By 1961, the production level cell efficiency reached 11% with improvement in series resistance and fabrication processes. For space application, it was a necessity to use solar power and the issue of cell price was secondary. However, for terrestrial application, solar cell cost was driving force for its further development. After 1972, solar cells started getting attention as an alternate energy source for terrestrial applications when oil prices increased significantly.

In 1972, the concept of back surface field passivation is introduced by NASA Lewis Research Center. In BSF, p^+ impurity (e.g., aluminum) is driven into the back of the silicon wafer which results in impurity concentration gradient and helps to accelerate minority carriers generated in the base of the cell toward the junction and also improves the red response of the cell. With the help of BSF, it became possible to make thinner cells of thicknesses from 100 to 200 μm (Treble 1998).

In 1974, a major improvement came from COMSAT Laboratories where they introduced surface texturing concept (Green et al. 1999). For surface texturing, the

Fig. 2.7 Si solar cell based on “grown-in” junction due to segregation of impurities in slow recrystallization of silicon melt reported in 1941 (after Ref. (Green 2002))

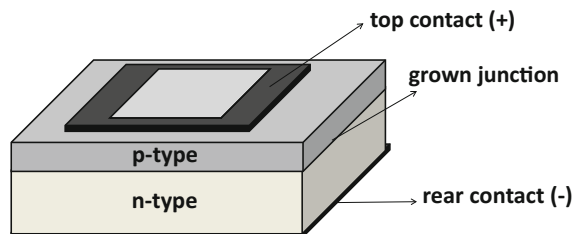
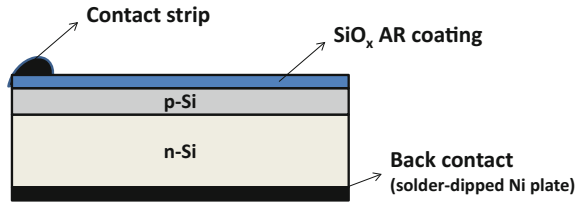


Fig. 2.8 Early p/n junction cell (1956) by Hoffman Electronics of Evanston (after Ref. (Treble 1998))



surface was selectively etched to form pyramids to eliminate the reflection losses from the cell surface. The combination of BSF and surface texturing along with introduction of junction depth reduction concept resulted in solar cell efficiency up to 15% in air mass (AM) zero condition (AM0) which is meant for space applications. These types of cells shown 16–17% efficiency in air mass 1.5 global (AM1.5G) radiation, i.e., for terrestrial applications (Green et al. 1999).

In the direction of manufacturing cheaper cells, multi-crystalline silicon (c-Si) wafers were introduced in 1974 as an alternative to mono c-Si wafers for producing cells (Treble 1998). Also, improvement in wafer cutting technique led to manufacture thinner wafers (400–250 μm). Dramatic reduction in cell manufacturing cost was seen after introduction of screen printing technology for contacts which replaced the costly photolithographic masking and vacuum deposition process requirements. By 1980s, screen printing technology had become well adapted for contact fabrication in cells. The multi c-Si wafer-based cell with screen printed contact made the cells commercially viable for terrestrial applications. In 1975, the terrestrial c-Si solar cells had achieved 10% efficiency (under AM 1.5 conditions) for mono c-Si- and 8% multi c-Si-based materials.

In 1982, Passivated Emitter Solar Cell (PESC) was reported by Dr. M.A. Green research group from UNSW. It had 2–3 nm thin SiO_2 insulator on the front surface (see Fig. 2.9a). The thin SiO_2 insulator was used to reduce the recombination of generated carriers at front. This design modification resulted in improvement in open circuit voltage enhancement from 614 to 690 mV under standard test conditions (STC) which resulted in achieving the 16% efficiency mark (Treble 1998).

Further design modifications were done in PESC cell structure, e.g., reduction in front contact metallization (see Fig. 2.9b) and process refinement, which helped to achieve the 19.1% efficiency mark under AM1.5 condition by 1985. Incorporation of microgrooved surface further raises the efficiency to 20.9%. These cells were fabricated using float zone wafers and contacts were made using photolithographic mask and vacuum deposition technique. Though the techniques used in these cell fabrications were costly, but it showed the way and the potential to achieve high efficiency. In 1985, Dr. M.A. Green research group from UNSW came up with cheaper process option to fabricate high-efficiency cells. These cells were called buried contact cell (see Fig. 2.9c) made from mono c-Si p-type Czochralski (CZ) Si wafers which were much cheaper than float zone wafers. These cells have textured surface, an oxide layer, BSF layer, plated Ni/Cu contact buried in laser scribed slots

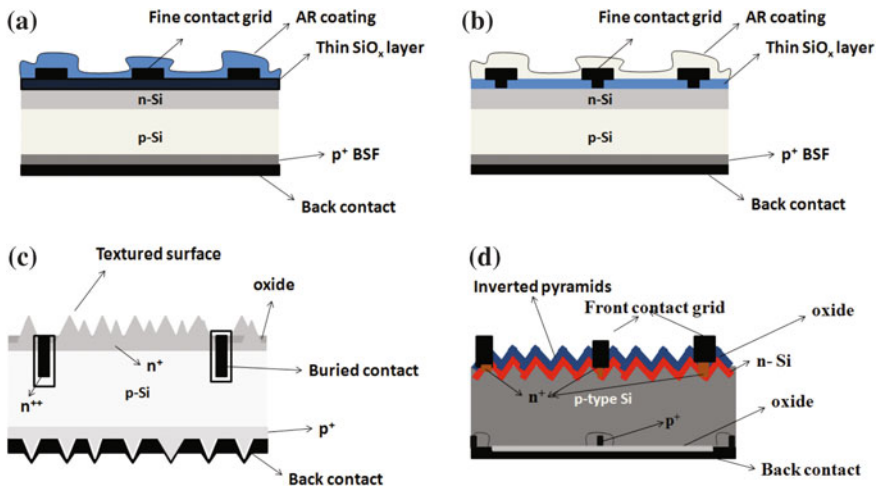


Fig. 2.9 Schematic of **a** Passivated Emitter Solar Cell (PESC); **b** Modified Passivated Emitter Solar Cell; **c** buried contact cell; **d** PERL (passivated emitter and rear locally diffused) cells (after Ref. (Treble 1998)) (images not to scale)

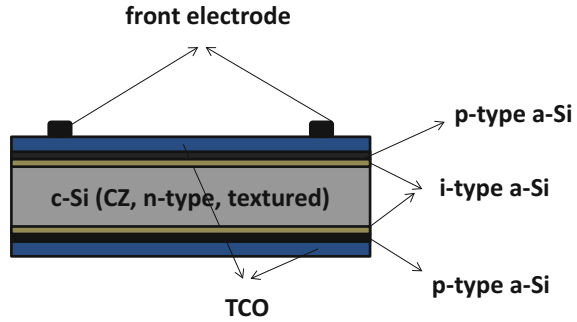
(Treble 1998; Green et al. 1999). This cell design was shown to give 19.6% efficiency and was adopted by BP solar for industry scale production.

M.A. Green's group in 1991 made PERL (passivated emitter and rear locally diffused; see Fig. 2.9d) cells having efficiency of 23.3% (Blakers et al. 1990; Treble 1998). It was fabricated using float zone mono c-Si wafer and had inverted pyramids for reflection reduction and thin oxide layer on front as well as back for surface passivation (Green et al. 1999). It also had small contact area with highly doped p⁺ and n⁺ regions. Further process modification and use of double layer antireflection (DLAR) coating in PERL cell resulted in 24–25% efficiency (Zhao et al. 1996; Green 2009). Today, best multi c-Si-based cells have reached 21.3% efficiency mark and mono c-Si-based cells at 25% mark having large area (NREL 2016).

c-Si-based solar cell with new cell design having heterojunction, known as HIT (heterojunction with intrinsic thin layer) cell, was also reported by Panasonic. It has marked world record efficiency of 25.6% (Green et al. 2015) which had been first announced in 2013 with record efficiency of 24.7%. In HIT cell, an intrinsic (i-type) a-Si layer and a p-type a-Si layer deposited on a randomly textured n-type CZ c-Si wafer to form a p/n heterojunction as shown in Fig. 2.10 (Taguchi et al. 2014).

The i-type and n-type a-Si layers deposited on the opposite side of the wafer resulted in a back surface field structure (see Fig. 2.10). On both sides of the doped a-Si layers, transparent conductive oxide (TCO) layers and metal grid electrodes were used (Taguchi et al. 2014).

Fig. 2.10 Schematic of a HIT cell (after Ref. (Taguchi et al. 2014))



2.3 Manufacturing Process of c-Si Solar Cells

c-Si solar cell was the first among various types of solar cells which came into existence and became widely used solar cell technology. The main reason behind becoming most preferred technology and its fast development was:

- a. Presence of well-established microelectronic industry.
- b. Simple processing requirement.
- c. Well understood physics behind its operation and performance impacting parameters.
- d. Stability and reliability of the device.

The manufacturing of a c-Si solar cell has many unit processes depending upon the planned device structure. However, it is much lesser than the unit processes involved in many microelectronics device fabrications. For better and efficient solar cell, each unit processes requires proper optimization. Here, we will discuss in brief the process steps involved in fabricating a typical solar cell to have a basic understanding of c-Si solar cell device fabrication.

For fabricating c-Si wafer-based solar cell, start with c-Si wafer. It can be mono c-Si wafer or multi c-Si wafer. For manufacturing wafer, silica (SiO_2), also known as sand, is used as raw material which is made from second most earth abundant element available on earth, i.e., silicon (Si). Silica is molten at high temperature and reduction with carbon gives metallurgical grade silicon which is about 97% pure. Further purification process is done to reduce the elemental impurities and electronic grade Si is achieved when the impurity present is less than parts per billion (ppb). Hydrogen chloride (HCl) is used to make trichlorosilane (SiHCl_3) which is an intermediate compound of polysilicon manufacturing. SiHCl_3 is further vaporized and diluted with hydrogen (H_2) while passing it through deposition reactor, which transforms the material into elemental silicon which has impurity level less than 0.001 ppb. After this, the electronic grade poly silicon is used for fabricating mono- or multi c-Si ingots. For mono c-Si ingot manufacturing, the most widely used techniques are Czochralski (CZ) technique or Float Zone (FZ) technique. For multi c-Si ingot manufacturing the most widely used technique is Siemens

technique. The details of these techniques are not being discussed here as it is beyond the scope of the book. After manufacturing the ingots, the wafers are produced by wire sawing. Technological advancement in wafer cutting is important to make wafers thinner and with low kerf loss. Kerf loss is the loss of material (usually indicated in width) while cutting the wafers from ingots. Many techniques like wire electrical discharge machining and other kerf loss less processes are being explored (Dongre et al. 2015). Manufacturing of the wafers constitute a complete industry which supplies the wafers of desired quality and quantity to solar cell manufactures.

Once the wafer is available, further process of manufacturing solar cell begins. Figure 2.11 shows the steps involved in manufacturing of a typical cell having geometry as shown in Fig. 2.12.

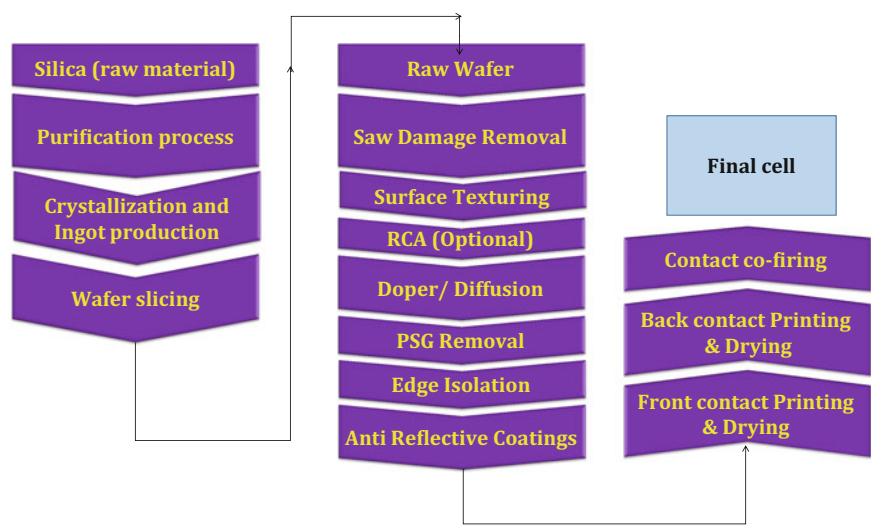
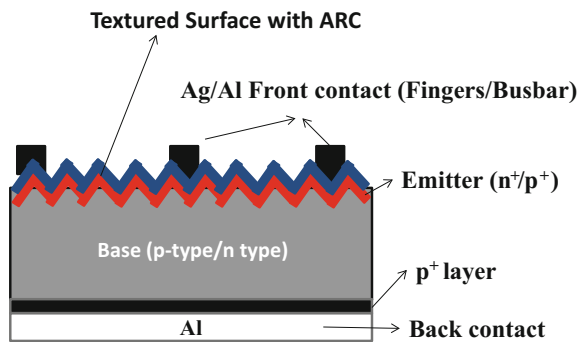


Fig. 2.11 Process flow/steps involved in manufacturing of a typical c-Si based solar cell

Fig. 2.12 Schematic of a typical cell structure under consideration



First, the wafer received as per desired base doping/resistivity, usually in as-cut form, is subjected to chemical process for saw damage removal. For saw damage removal, usually sodium hydroxide (NaOH) or potassium hydroxide (KOH) solution in deionized (DI) water is used at temperature of 70–80 °C.

After saw damage removal, surface roughening/texturing process is done to reduce the reflection from the surface. In case of mono c-Si wafers, directional etching using chemical solution usually NaOH/KOH in DI water in the presence of isopropyl alcohol (IPA) is used. In case of multi c-Si wafers, acidic solution for texturing is used to form honeycomb-like structure on surface. In this case chemical solutions like hydrofluoric acid (HF) and nitric acid (HNO₃) are widely used.

After surface texturing, RCA cleaning step can be used. RCA process was first developed at Radio Corporation of America and that is why the name RCA. RCA processes have two types. One is called RCA-1 which is a combination of DI water, ammonium hydroxide (NH₄OH), and hydrogen peroxide (H₂O₂). This process helps to remove residue of organic solvents from the surface of Si wafer. The other type is RCA-2 which is a combination of DI water, hydrogen chloride (HCl), and H₂O₂. It helps to remove crucial contaminant like gold (Au) which can introduce mid-gap trap states, which can severely impact the solar cell performance. This step is usually optional in industry process as it adds up to the cost of the cell.

The next step is dopant diffusion for p/n junction formation. Phosphorous-based dopant (usually liquid source like phosphoryl trichloride (POCl₃)) is used for p-type cells and boron-based dopant (usually liquid source like boron tribromide (BBr₃)) for n-type cells. Diffusion process is done at high temperature usually 800–900 °C. Diffusion process optimization is done depending upon the requirement of the concentration of doping in the emitter of the cell.

After diffusion process, glass removal (phosphorus silicate glass (PSG) in case of phosphorous-based dopant/borosilicate glass (BSG) in case of boron-based dopant) process is done. Usually, dilute HF solution is used for PSG/BSG removal.

After glass removal step, edge isolation is done which helps to remove the conduction path from top and bottom layers which may have resulted in shunt. This step basically results in electrical isolation between emitter and rear base of the cell. Usually, laser/plasma etching-based techniques are used for edge isolation. In laser technique, edges of the cell are finely cut. In plasma technique, reactive ion etchant are used for etching the edges.

After edge isolation, anti-reflection coating layer is used. The thickness and the refractive index is optimized such that it suits with the texture surface and result in minimum reflection from the surface. It also serves the purpose of passivation which is important for better performance of the cell. Depending upon the type (p-type/n-type), dielectric material is chosen. Usually, thermal oxide (SiO₂), silicon nitride (SiN_x), aluminum oxide (Al₂O₃), titanium dioxide (TiO₂) are used. Also, combination of the dielectric layers of different thicknesses has been used for better cell performance. Most widely used technique for dielectric deposition is chemical vapor deposition (CVD).

After dielectric layer deposition, contact printing is done. The most widely used technique for contact printing is screen printing. In cell contact printing, the back

surface is fully covered with metal and the front surface has fingers and bus bars with optimized thickness and width so that it offers minimum series resistance and minimum metal shading to allow maximum light to reach the cell. For screen printing, usually aluminum (Al) and silver (Ag) paste is used which contain an organic binder, solvent, glass frit, and Ag/Al nanoparticle. Screen which used to print the contact on cell surface has wire netting usually stainless steel coated with emulsion. After printing, drying is done at 200–250 °C to remove the solvent.

After contact printing and drying, contact co-firing is done to ensure the ohmic contact of metal contacts with semiconductor. Usually, belt furnace is used which has different temperature zones ranging from 400 to 900 °C. The cell move through the furnace on belt and passes through different temperature zones. In this process, the metal contacts get through dielectric layer at front surface and make contact with Si. And at the same time, Al at the back side, reacts with Si and forms BSF. Cell is ready now for measurement.

2.4 Photovoltaic Effect in c-Si Solar Cells and Important Parameters

2.4.1 Photovoltaic Effect in c-Si Solar Cells

When light shines on a c-Si solar cell, the photons are absorbed in Si material and results in generation of electron–hole (e-h) pairs. These e-h pairs move within the material until it sees a potential gradient, i.e., electric field which is sufficient to break the e-h pairing. This phenomenon happens at p/n junction where there is potential gradient. In a p-type cell, the holes moves toward the back electrode and the electron are collected at front electrode as shown in Fig. 2.13a. Figure 2.13b

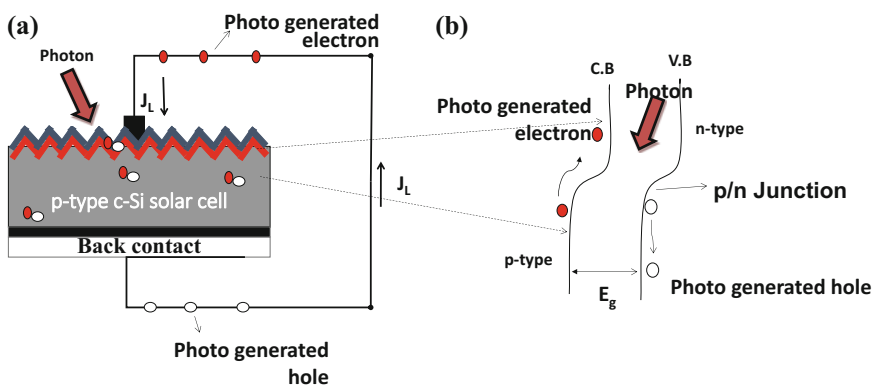


Fig. 2.13 **a** Schematic of a e-h pair generation and collection in typical p-type c-Si solar cell; **b** energy band diagram of a photovoltaic operation. C.B indicates conduction band and V.B indicates valance band. (Images not to scale)

shows the energy band diagram of a typical p-type c-Si solar cell photovoltaic operation. When light falls on solar cell, e-h pair is generated. The e-h pair moves toward the junction where it gets separated and is collected from electrodes. Here to note that only photons having energy larger than or equal to the band gap of Si (≥ 1.12 eV) are absorbed (neglecting phonon-assisted absorption) and contribute to the e-h pair generation and photogenerated current (J_L).

2.4.2 Current–Voltage Characteristics

In solar cell, the photogenerated current is maximum when there is no connected load. When the load is connected to the cell, the photogenerated current (J_L) due to cell illumination results in voltage drop (V) across the load which biases the p/n junction in forward direction. The equivalent circuit diagram of a solar cell is shown in Fig. 2.14a in ideal case, where solar cell is combination of constant current source and a p/n junction diode in parallel as shown with load resistance (R_L).

The forward-biased p/n junction results in forward bias diode current (J_D). But the photogenerated current (J_L) is much larger than the forward bias diode current (J_D) and it is in opposite direction to J_D . Therefore, the net solar cell current under illuminated condition is in reverse direction of generated forward bias voltage. The solar cell operation is given by Eq. (2.1) where J_0 is reverse saturation current density of the diode, q is electron charge, k is Boltzmann constant and T is temperature.

$$J = J_D - J_L = J_0 \left[\exp\left(\frac{qV}{kT}\right) - 1 \right] - J_L. \quad (2.1)$$

The net current shown in Eq. (2.1) is in ideal case. But in realistic case, series and shunt resistance comes into picture which impacts the cell performance. A realistic case solar cell equivalent circuit diagram is shown in Fig. 2.14b. Here a shunt resistance (R_{sh}) is considered in parallel to the p/n junction diode which accounts for the various leakage currents in the solar cell due to different recombination effects. The series resistance (R_s) in series accounts for the various ohmic

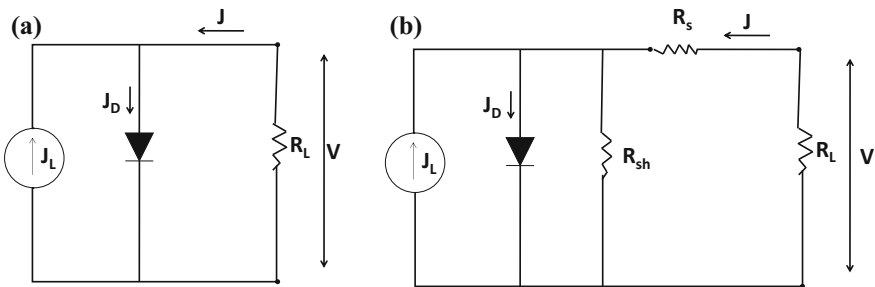


Fig. 2.14 Solar cell equivalent circuit diagram in **a** ideal case; **b** realistic case

losses in the bulk material, at metal–semiconductor interface and contacts during current collection. In light of series and shunt resistance presence, the current–voltage equation under illuminated condition is modified as given in Eq. (2.2) where the new variable n (ideality factor) is introduced which accounts for the nonideal p/n junction diode and R_s , R_{sh} are series and shunt resistance respectively.

$$J = J_0 \left[\exp\left(\frac{q(V - J.R_s)}{n k T}\right) - 1 \right] + \frac{V - J.R_s}{R_{sh}} - J_L. \quad (2.2)$$

Above Eq. (2.2) is based on single diode model, however multi diode models are also considered in order to account the various recombination phenomenon in the solar cell and the Eq. (2.2) is further modified and is given by Eq. (2.3) where each term of J_{0k} and n_k represent a particular recombination mechanism (Altermatt et al. 1996).

$$J = \sum_{k=1}^m J_{0k} \left[\exp\left(\frac{q(V - J.R_s)}{n_k k T}\right) - 1 \right] + \frac{V - J.R_s}{R_{sh}} - J_L. \quad (2.3)$$

In typical solar cell, the widely used model is two diode model which was first introduced in 1963 by Wolf and Raushenbach (1963). The two diode model-based equivalent circuit is shown in Fig. 2.15a. And for illuminated condition, the current–voltage characteristic is given in Eq. (2.4).

$$J = J_{01} \left[\exp\left(\frac{q(V - J.R_s)}{n_1 k T}\right) - 1 \right] + J_{02} \left[\exp\left(\frac{q(V - J.R_s)}{n_2 k T}\right) - 1 \right] + \frac{V - J.R_s}{R_{sh}} - J_L. \quad (2.4)$$

Here J_{01} and J_{02} are the saturation current densities through the two modeled diodes which separately represent recombination current densities of emitter/base, which dominates at high forward bias, and space charge region, which dominates at low forward bias, respectively (Pysch et al. 2007). Also, n_1 and n_2 are the ideality

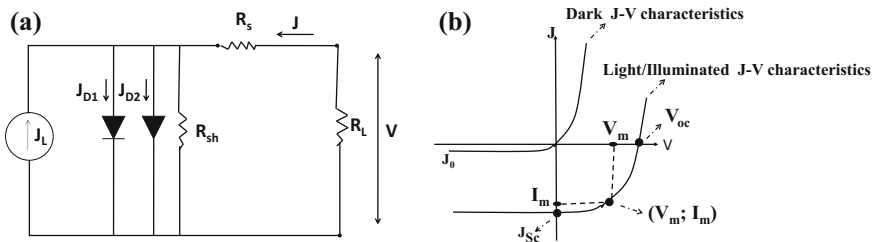


Fig. 2.15 **a** A typical solar cell equivalent circuit diagram with two diode model; **b** Current–voltage characteristics of a typical cell in dark and illuminated condition

factors representing for the two modeled diodes of the solar cell. A typical current–voltage (J-V) characteristic for a solar cell can be seen in Fig. 2.15b for both light/illuminated and dark measurement conditions. In dark condition, the photo-generated current (J_L) would be zero.

2.4.3 Important Solar Cell Parameters

2.4.3.1 Open Circuit Voltage (V_{oc})

When cell is illuminated and no current is drawn from the cell, the voltage obtained from the cell is called open circuit voltage (V_{oc}) (at $J = 0$ in Fig. 2.15b). V_{oc} is function of photogenerated current (J_L), reverse saturation current (J_0), ideality factor (n), and cell temperature (T). It is expressed in mathematical form as in Eq. (2.5).

$$V_{oc} = \frac{nkT}{q} \ln\left(\frac{J_L}{J_0} + 1\right). \quad (2.5)$$

Here V_{oc} dependence on J_0 makes it dependent on recombination effect in the cell. For better V_{oc} from the cell, the recombination in the cell should be avoided. V_{oc} is also influenced by temperature. Per degree centigrade increase in temperature of the cell results in about 1.7 mV reduction in V_{oc} in case of c-Si-based solar cells (Goetzberger et al. 1998).

2.4.3.2 Short Circuit Current (J_{sc})

When cell is illuminated and short circuited, the current obtained from the cell is called short circuit current (J_{sc}) (at $V = 0$ in Fig. 2.15b). It is the maximum current that can be drawn from the cell. For Si-based cell, if all the photons are absorbed, about 46.6 mA/cm² current can be expected (neglecting all electrical and optical losses) in AM 1.5G radiation (radiation falling on earth surface is 100 mW/cm² in AM 1.5G condition).

2.4.3.3 Maximum Power (P_{max})

Maximum power (P_{max}) indicates the maximum achievable power from the solar cell when it is illuminated. It is the product of voltage (V_m) and current (J_m) at optimal operating point (see Fig. 2.15b). At P_{max} , $d(J.V)/dV = 0$ and P_{max} can be also be expressed in terms of V_{oc} as given in Eq. (2.6).

$$P_{\max} = V_m \cdot J_m = \frac{nkT}{q} \ln \left[\frac{\left(\frac{J_s}{J_0}\right) + 1}{1 + \left(\frac{nkT}{q}\right) V_m} \right]. \quad J_m \approx \left[V_{oc} - \frac{nkT}{q} \ln \left(1 + \frac{V_m}{\left(\frac{nkT}{q}\right)} \right) \right] \cdot J_m. \quad (2.6)$$

2.4.3.4 Fill Factor (FF)

Fill factor is defined as the ratio of maximum achievable power (P_{\max} , i.e., $V_m \cdot J_m$) from the device to the maximum power generation capacity of the device (i.e., $V_{oc} \cdot J_{sc}$). It is expressed as Eq. (2.7).

$$FF = \frac{V_m \cdot J_m}{V_{oc} \cdot J_{sc}}. \quad (2.7)$$

FF of the cell is influenced by resistive losses and nonideal recombination in solar cells. It is also a measure of the p/n junction quality and series resistance (R_s) of the cell. Also, significant shunt effect ($R_{sh} < 1000 \, \Omega\text{-cm}^2$) in the cell would impact FF of the cell. In practical c-Si solar cells, FF mostly observed between 0.78 and 0.80 depending upon the quality of contact on the cell fabricated and the cell manufacturing process. Note that the poor contact quality may result in much lesser FF.

2.4.3.5 Efficiency (η)

Quantitatively, efficiency is defined as the ratio of output from a device to the input and is important parameter to quantify the device performance. In solar cell, the efficiency is defined as ratio of maximum achievable power to the input power. It depends on the incident light intensity and spectrum as well as temperature of the cell. Terrestrial cells are measured under standard test conditions (STC) with simulated AM1.5G radiation. The cell temperature is kept at 25 °C. For AM 1.5G spectrum, incident power (P_{in}) is 100 mW/cm² and maximum achievable power from a device is P_{\max} ($=V_m \cdot J_m$).

Mathematically, Efficiency(η) is expressed as Eq. (2.8):

$$\eta = \frac{P_{\max}}{P_{in}} = \frac{V_m \cdot J_m}{P_{in}} = \frac{FF \cdot V_{oc} \cdot J_{sc}}{P_{in}}. \quad (2.8)$$

2.4.3.6 Quantum Efficiency (QE)

Quantum efficiency (QE) is used as a diagnostic tool to evaluate the solar cell performance. It helps in analyzing the cell performance quantitatively as well as

qualitatively. Solar cell responds to different wavelengths differently. Photon of particular wavelength absorbed in solar cell generate e-h pair and depending upon the number of photons in spectrum for a particular wavelength, number of e-h pairs are generated. Percentage of photons of particular wavelength converted into e-h pairs which contribute to electrical current (collected from device) when the cell is short circuited is called quantum efficiency (QE). QE is further divided into two categories known as external quantum efficiency (EQE) and internal quantum efficiency (IQE).

- (i) **External Quantum Efficiency (EQE):** EQE is defined as the ratio of number of electrons collected from solar cell under short circuit condition to the number of photons of particular wavelength incident on the cell. It is also known as Incident Photon to Current Efficiency (IPCE). EQE (in %) can be mathematically expressed as Eq. (2.9):

$$EQE(\lambda) = \frac{1240 \times J_L}{\lambda \times P_{in}} \times 100, \quad (2.9)$$

where λ is incident photon wavelength in nm, J_L is photogenerated current from the incident photon (in mA/cm²) and P_{in} is incident photon power (W/m²).

- (ii) **Internal Quantum Efficiency (IQE):** IQE is defined as the ratio of number of electrons collected from solar cell under short circuit condition to the number of photons of particular wavelength absorbed by the cell. Note that IQE does not include the reflected or transmitted photons in account. IQE (in %) can be mathematically expressed as Eq. (2.10):

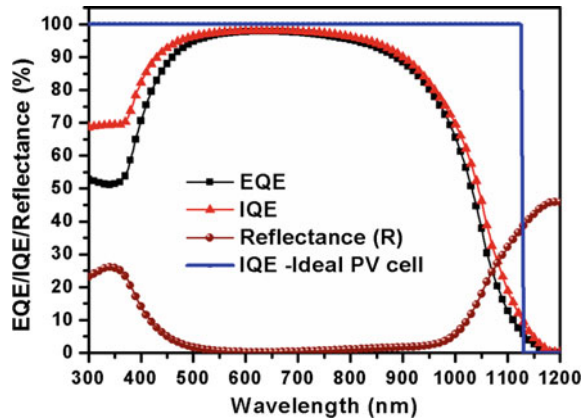
$$IQE(\lambda) = \frac{EQE(\lambda)}{(1 - R - T)} \times 100, \quad (2.10)$$

where R is reflectance from the cell and T is transmittance through the cell. In case of c-Si solar cell, back surface is fully covered with metal contact which makes $T = 0\%$ and the IQE is generally expressed as Eq. (2.11):

$$IQE(\lambda) = \frac{EQE(\lambda)}{(1 - R)} \times 100. \quad (2.11)$$

Here to note that IQE is corrected form of EQE which does not account for reflection losses in the cell and it is considered as better indicator of solar cell bulk material, the p-n junction, front and back surface passivation quality, etc. Since high-energy photons are absorbed near front surface of the cell, IQE at high-energy wavelengths indicates the junction and front surface passivation quality. Also, low-energy photons travel deep into the cell, IQE at lower energy wavelength

Fig. 2.16 EQE, IQE and reflectance graph plot of a typical c-Si solar cell and IQE of a ideal c-Si PV cell



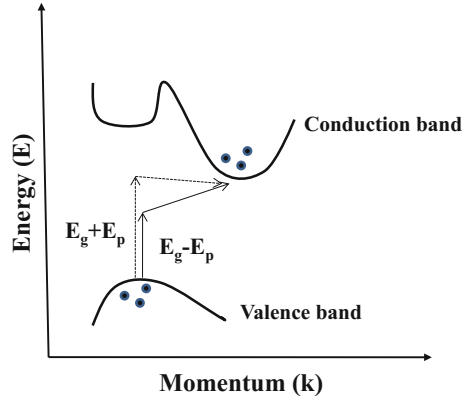
indicates the bulk property of the cell as well as the back surface passivation quality. In ideal case, IQE should be 100%, however, in realistic case; it is always less than 100% reflecting the loss of generated e-h in recombination. To get maximum performance from the cell, the cell should be designed such that the IQE be maximum for the wavelengths which are in abundance in the incident light spectrum. QE curve of a typical c-Si-based solar cell is shown in Fig. 2.16.

One can see that for high-energy photons, IQE is less and this loss can be attributed to front surface recombination. Also, nonactive absorbing layer, e.g. ARC layers, may result in parasitic absorption leading to IQE loss. Also, at low-energy wavelengths, IQE loss can be seen which can be attributed to low absorption, low minority carrier lifetime, back surface recombination, etc.

2.5 Role of Light-Trapping Structures

c-Si wafers are made up of silicon (Si) which is an indirect band gap semiconductor. Light absorption and corresponding excitation of an electron from valance band to conduction band is weak in indirect band gap semiconductor as it does not satisfy the requirement of momentum conservation since top of the valance band and bottom of the conduction band does not occur on same momentum (k) in energy (E)–momentum (k) diagram as shown in Fig. 2.17. To conserve the momentum, the optical absorption is assisted by phonon which is quantized lattice vibration. A phonon is either emitted or absorbed during the process of photon absorption (Pankove 1971) and result in electron transition from valance band to conduction band. Due to involvement of phonons in optical absorption, the absorption coefficient of an indirect band gap semiconductor is proportional to energy band gap (E_g) and phonon energy (E_p) as per relation as given in Eq. 2.12 where E is photon energy (Sze and Ng 2006).

Fig. 2.17 E-k diagram of a typical indirect band semiconductor (after Ref. (Pankove 1971))



$$\alpha(E) \propto (E - E_g \pm E_p)^2. \quad (2.12)$$

Due to indirect band gap nature of Si, it weakly absorbs light especially at longer wavelength near its band gap where the absorption coefficient is very small (Fig. 2.18a). Figure 2.18a shows the absorption coefficient (α) of Si in cm^{-1} along with absorption length ($1/\alpha$), a length required to absorb light completely for a particular wavelength. It can be noticed that a 100- μm -thick c-Si wafer would be sufficient to absorb light up to 950 nm wavelength. However, above 950 nm till band gap of Si (1.12 eV), much thicker material is required. For 1150 nm wavelength, the required thickness of material is about 10 mm. Using such thick material is infeasible, particularly from the perspective of cost.

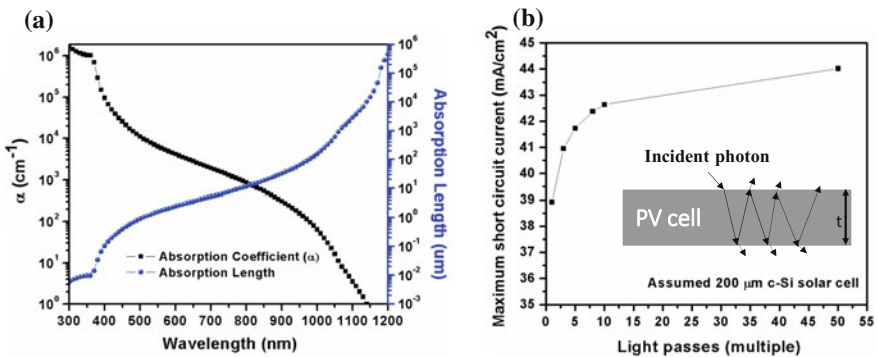


Fig. 2.18 **a** Wavelength dependence of absorption coefficient (α) of Si in cm^{-1} (after Ref. (Green and Keevers 1995)) along with absorption length; **b** Maximum short circuit current that can be generated after multiple light passing through active absorbing material of c-Si solar cell of 200 μm thickness

When targeting cell using c-Si wafer, the wavelengths in solar spectrum which are of interest are 300–1200 nm. In order to absorb this entire wavelength range, large thickness of wafer would be required. However, if light is made to travel back-and-forth in the solar cell (in active absorbing material), the optical thickness of the solar cell can be increased while keeping the geometrical thickness same. This can be used useful in reducing the thickness of the wafer required, which can be obtained by suitably optimized light-trapping structure. Figure 2.18b shows the maximum short circuit current that can be generated after multiple light passes through active absorbing material of c-Si solar cell of 200 μm thickness. For single pass, the maximum expected short circuit current is 38.9 mA/cm^2 which is increased to 42.4 mA/cm^2 for 8 passes and 44.0 mA/cm^2 for 50 passes. It can be noticed that how an efficient light-trapping structure can result in optical thickness increment of the cell keeping the same geometrical thickness (200 μm in present case), and hence increase in current generation capacity. This indicates the necessity of a suitable light-trapping structure in Si-based cell where cost-effectiveness and efficiency both are desired.

The Si flat surface results in reflection in the range of 35–50%. In order to reduce reflection from Si surface, surface texturization is done where Si surface is intentionally made rough. In 1974, Haynos reported the first evidence of reflection reduction in Si solar cell using Si surface texturing (Haynos et al. 1974). The cells were made using (100) Si wafer and anisotropic etching. These texturing-based cells resulted in efficiency of 15.0–15.5% under AM0 radiation which would be equivalent to 16.7–17.2% under AM1.5G radiation (Green et al. 1999). Yablonovitch and Cody (1982), Yablonovitch (1982) theoretically showed using statistical ray optics approach that light-trapping absorption can be enhanced maximum up to $4n^2$, where n is the refractive index, for weakly absorbing wavelengths by surface roughening of a semiconductor surface.

2.6 ITRPV Roadmap for c-Si Solar Cell Development

Global leaders in manufacturing of c-Si products, e.g., wafers, cells and modules, came together and created International Technology Roadmap for Photovoltaic (ITRPV). The first ITRPV report result was published in 2010. The aim of ITRPV was to ensure constant efficiency increase along with the cost reduction with the help of technology advancements. ITRPV provides a common platform to discuss the sustainable PV market; guideline for whole c-Si PV technology supply chain (includes silicon, c-Si wafer, c-Si module, inverter, and PV system, etc.); ground for cooperation among the supply chain; guideline for material and equipment suppliers; target for R&D centers and PV standardization source; which are regularly updated.

The topics presented in the ITRPV report are divided into three main areas, i.e., materials, process, and products. In this section we would discuss some of the proposed improvements in near further at cell level only.

The recent 2014 ITRPV reports (ITRPV 2015) indicate that poly silicon price has been reduced from 67 USD/kg in 2010 to 16.6 USD/kg in 2014, i.e., about 75% reduction in price in just 4 years and even further reduction in prices is indicated. In wafer sawing technology, slurry-based wafer sawing is dominating. However, diamond wire sawing is expected to gain market in near future with targeted kerf loss of less than 20 μm . Further, as per latest poly Si prices and wafer manufacturing technology, wafer still accounts for 51% of the cost in cell price and need for technology to reduce the thickness of the wafer has been envisioned. Wafer thickness of 100–120 μm range would possibly be in mass production made by 2025.

Improvements in process technology have been aimed to reduce recombination losses in solar cells. Reduction in bulk recombination current ($J_{o,\text{bulk}}$) of the solar cell has been targeted from 350 to 100 fA/cm^2 for p-type multi c-Si solar cell and from 250 to 50 fA/cm^2 for p-type mono c-Si solar cells. Emphasis to improve rear side passivation of the cell has been given to improve the cell performance. Silicon oxynitride (SiON_x)/Aluminum oxide (Al_2O_3) has been indicated as potential dielectric for back surface passivation.

Also, reduction in silver mass by reducing contact finger width for contacts has been proposed along with introduction of copper (Cu) plating technology for contact fabrication as an alternative to Ag to make solar cell even more cheaper.

2.7 Next Generation c-Si Solar Cells

For making solar cell cheaper, thinner wafer is being targeted for solar cell manufacturing and it is expected to be available in mass production by 2025. Top-down as well as bottom-up approaches are being actively researched for fabricating thin wafer-based c-Si solar cells. In bottom-up approach, epitaxial grown c-Si layer on substrates using porous layer transfer method are being explored. Layer transfer techniques consist of three important steps which are (Petermann et al. 2012):

- i. HF acid-based electrochemical pores etching into a silicon substrate wafer.
- ii. Epitaxial growth of mono c-Si layer on the porous silicon.
- iii. Separation of the epitaxial layer from the growth wafer.

Recently, a 16.8% efficient 18- μm silicon solar cell on steel substrate was demonstrated using such method where the 18 μm n-type silicon as active absorbing layer was epitaxially grown with 2 μm front surface n^+ layer and 1 μm rear p^+ layer with shallow texturing on the top (front surface) (Wang et al. 2014). The cell was having architecture more like PERL cells where the front contact was made using Ni-Cu plating through dielectric opening at front. Also, in another effort to make thin c-Si wafer-based cells, similar technique of porous layer transfer was followed to fabricate 43 μm thin c-Si solar cell which resulted in 19% efficiency. The schematic of the solar cell device structure is shown in Fig. 2.19a.

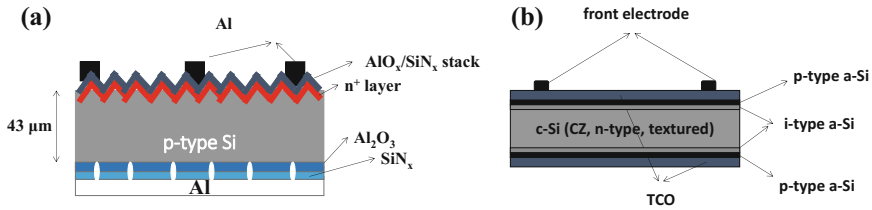


Fig. 2.19 **a** Schematic of porous layer transfer based 43 μm thin c-Si solar cell (after Ref. (Petermann et al. 2012)); **b** schematic of HIT cell using less than 100 μm thin c-Si wafer (after Ref. (Taguchi et al. 2014))

The cell has rear surface passivation using dielectric which is necessary for efficient thin wafers-based solar cells. The back contact was made using local opening in dielectric and subsequent Al evaporation. Also, the front surface was textured and had about 4 μm random pyramids for light trapping.

In top-down approach, different wafers cutting techniques are being explored to manufacture thin wafers with minimum kerf loss and ITRPV projects to have 100–120 μm thin wafers in mass production by 2025. Up to 25% efficiency cell on less than 100 μm thin c-Si wafer has been demonstrated recently (Taguchi et al. 2014). The solar cell is known as heterojunction with intrinsic thin layer (HIT) cell. The typical schematic of the HIT cell is shown in Fig. 2.19b. In HIT solar cell, p/n heterojunction is formed using intrinsic (i-type) amorphous silicon (a-Si) layer and a p-type a-Si layer deposited on a randomly textured n-type CZ c-Si wafer. The a-Si (n-type and i-type) deposited on the opposite side of the wafer provide back surface field passivation. The high-quality intrinsic a-Si layer between the c-Si wafer and the doped a-Si layer helps to achieve very good surface passivation which is crucial in thin wafer-based solar cells. For contacts, transparent conductive oxide (TCO) layers and metal grid electrodes are fabricated on both sides.

The trend of fabricating cost-effective and efficient cell indicates that the next generation solar cells are going to be fabricated on much thinner (50–100 μm) wafers. In such case, rear surface passivation and light-trapping structure would be

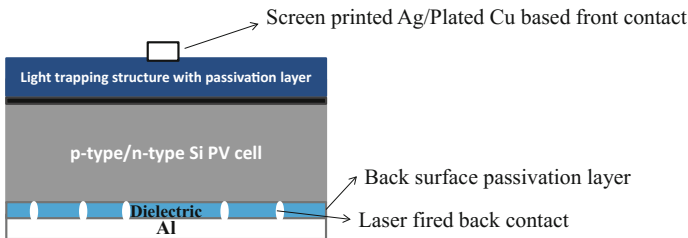


Fig. 2.20 Schematic of a typical next generation thin c-Si solar cell

playing important role in manufacturing efficient and cost-effective solar cells. The next generation cell would have typical device structure as shown in Fig. 2.20. The back surface passivation would be essential part of the cell and laser firing-based contact (LFC) would be preferable option for back contact formation (Schneiderlochner et al. 2002; Sánchez-Aniorte et al. 2010; Petermann et al. 2012; Wang et al. 2014). Front contact can be screen printed Ag/Al or plated Cu based contacts.

The front surface would have light-trapping structure with antireflection coating. Advanced light-trapping structure would replace texturing-based light-trapping structure since texturing of surface increases surface recombination which is more crucial when thinner wafer are being aimed. Texturing-based light-trapping structures also consume material and also results in reduction in absorption in active material. Traditional light-trapping structure as well as advanced alternative light-trapping structures favorable for next-generation thin c-Si solar cells has been explored in this book in greater detail in subsequent chapters.

2.8 Questions and Problems

1. Discuss the role of wafer prices on solar cell manufacturing cost over the years?
2. Classify the different c-Si-based solar cell technology in detail?
3. Mono c-Si solar cells generally perform better than multi c-Si solar cells. Why?
4. Discuss the evolution of c-Si solar cell technology?
5. How modification in c-Si solar cell design and processes impacted the cell performance over the years?
6. What are the main factors which drove the c-Si solar cell cost down over the years?
7. What do you understand by HIT cell? How is different from mono and multi c-Si solar cell technology?
8. Discuss the fabrication steps involved in solar cell manufacturing of a typical c-Si solar cell?
9. What do you understand by photovoltaic effect in c-Si solar cell?
10. Discuss the performance parameters of a solar cell. How are they interrelated?
11. The short circuit current of a c-Si solar cell at room temperature is 36 mA/cm^2 and the reverse saturation current is 10^{-8} mA/cm^2 . Calculate the maximum output power and efficiency of the cell under AM1.5G radiation. Consider that the device ideality factor is 1 and the fill factor is 76%.
12. What do understand by ITRPV? How does it play role in c-Si solar cell technology development?
13. Discuss the next generation c-Si solar cells and the role of light-trapping structures?

References

- Altermatt PP, Heiser G, Aberle AG et al (1996) Spatially resolved analysis and minimization of resistive losses in high-efficiency Si solar cells. *Prog Photovolt Res Appl* 4:399–414. doi:[10.1002/\(sici\)1099-159x\(199611/12\)4:6<399::aid-pip148>3.0.co;2-4](https://doi.org/10.1002/(sici)1099-159x(199611/12)4:6<399::aid-pip148>3.0.co;2-4)
- Blakers AW, Zhao J, Milne AM et al (1990) Characterization of 23-percent efficient silicon solar. *Technology* 37:331–336
- Dongre G, Zaware S, Dabade U, Joshi SS (2015) Multi-objective optimization for silicon wafer slicing using wire-EDM process. *Mater Sci Semicond Process* 39:793–806. doi:[10.1016/j.mssp.2015.06.050](https://doi.org/10.1016/j.mssp.2015.06.050)
- Goetzberger A, Knobloch J, Voss B (1998) Crystalline silicon solar cells. Wiley (1998)
- Green MA (2009) The path to 25% silicon solar cell efficiency: history of silicon cell evolution. *Prog Photovolt Res Appl* 17:183–189. doi:[10.1002/pip.892](https://doi.org/10.1002/pip.892)
- Green MA (2002) Photovoltaic principles. *Phys E Low-Dimensional Syst Nanostruct* 14:11–17. doi:[10.1016/S1386-9477\(02\)00354-5](https://doi.org/10.1016/S1386-9477(02)00354-5)
- Green MA, Emery K, Hishikawa Y et al (2015) Solar cell efficiency tables (version 46). *Prog Photovolt Res Appl* 23:805–812. doi:[10.1002/pip.2637](https://doi.org/10.1002/pip.2637)
- Green MA, Zhao J, Wang A, Wenham SR (1999) Very high efficiency silicon solar cells-science and technology. *IEEE Trans Electron Devices* 46:1940–1947. doi:[10.1109/16.791982](https://doi.org/10.1109/16.791982)
- Green MA, Keevers MJ (1995) Optical properties of intrinsic silicon at 300 K. *Prog Photovolt Res Appl* 3:189–192. doi:[10.1002/pip.4670030303](https://doi.org/10.1002/pip.4670030303)
- Haynos J, Allison J, Arndt R, Meulenbergh A (1974) The COMSAT nonreflective silicon solar cell: a second generation improved cell. In: International conference on photovoltaic power generation, p 18
- International technology roadmap for photovoltaic (ITRPV) 2013 results (2014) www.itrpv.net/Reports/Downloads/2014/
- ITRPV (2015) International technology roadmap for photovoltaic (ITRPV) 2014 results
- NREL (2016) Best research cell efficiencies. http://www.nrel.gov/ncpv/images/efficiency_chart.jpg
- Pankove JI (1971) Optical processes in semiconductors. Dover
- Petermann JH, Zielke D, Schmidt J et al (2012) 19%-efficient and 43 μm -thick crystalline Si solar cell from layer transfer using porous silicon. *Prog Photovolt Res Appl* 20:1–5. doi:[10.1002/pip.1129](https://doi.org/10.1002/pip.1129)
- Pysch D, Mette A, Glunz SW (2007) A review and comparison of different methods to determine the series resistance of solar cells. *Sol Energy Mater Sol Cells* 91:1698–1706. doi:[10.1016/j.solmat.2007.05.026](https://doi.org/10.1016/j.solmat.2007.05.026)
- Sánchez-Aniorte I, Colina M, Perales F, Molpeceres C (2010) Optimization of laser fired contact processes in c-Si solar cells. *Phys Procedia* 5:285–292. doi:[10.1016/j.phpro.2010.08.148](https://doi.org/10.1016/j.phpro.2010.08.148)
- Schneiderlochner E, Preu R, Ludemann R, Glunz SW (2002) Laser-fired rear contacts for crystalline silicon solar cells. *Prog Photovolt Res Appl* 10:29–34. doi:[10.1002/pip.422](https://doi.org/10.1002/pip.422)
- Sze SM, Ng KK (2006) Physics of semiconductor devices, 3rd edn. Wiley, Hoboken
- Taguchi M, Yano A, Tohoda S et al (2014) 24.7% record efficiency HIT solar cell on thin silicon wafer. *IEEE J Photovolt* 4:96–99. doi:[10.1109/JPHOTOV.2013.2282737](https://doi.org/10.1109/JPHOTOV.2013.2282737)
- Tanaka N (2010) Technology roadmap: solar photovoltaic energy. OECD Publishing
- Treble F (1998) Milestones in the development of crystalline silicon solar cells. *Renew Energy* 15:473–478. doi:[10.1016/S0960-1481\(98\)00207-9](https://doi.org/10.1016/S0960-1481(98)00207-9)
- Wang L, Lochtefeld A, Han J et al (2014) Development of a 16.8% efficient 18- μm silicon solar cell on steel. *IEEE J Photovolt* 4:1397–1404. doi:[10.1109/JPHOTOV.2014.2344769](https://doi.org/10.1109/JPHOTOV.2014.2344769)
- Wolf M, Rauschenbach H (1963) Series resistance effects on solar cell measurements. *Adv Energy Convers* 3:455–479. doi:[10.1016/0365-1789\(63\)90063-8](https://doi.org/10.1016/0365-1789(63)90063-8)
- Yablonovitch E (1982) Statistical ray optics. *J Opt Soc Am* 72:899–907. doi:[10.1364/JOSA.72.000899](https://doi.org/10.1364/JOSA.72.000899)

- Yablonovitch E, Cody GD (1982) Intensity enhancement in textured optical sheets for solar cells. IEEE Trans Electron Devices 29:300–305. doi:[10.1109/T-ED.1982.20700](https://doi.org/10.1109/T-ED.1982.20700)
- Zhao J, Wang A, Altermatt P et al (1996) 24% efficient perl silicon solar cell: recent improvements in high efficiency silicon cell research. Sol Energy Mater Sol Cells 41–42:87–99. doi:[10.1016/0927-0248\(95\)00117-4](https://doi.org/10.1016/0927-0248(95)00117-4)

Anti-reflection and Light Trapping in c-Si Solar Cells

Solanki, C.S.; Singh, H.K.

2017, XXIX, 186 p. 128 illus., 88 illus. in color.,

Hardcover

ISBN: 978-981-10-4770-1