

Estimating the Maximum Propagation Delay of 4-bit Ripple Carry Adder Using Reduced Input Transitions

Manan Mewada^(✉), Mazad Zaveri, and Anurag Lakhiani

SEAS, Ahmedabad University, Ahmedabad, India
{manan.mewada, mazad.zaveri,
anurag.lakhiani}@ahduni.edu.in

Abstract. Adders are invariably present in arithmetic units, and they are needed for implementing the operations: addition/subtraction, multiplication, division, etc. Due to the crucial role of adder in arithmetic unit, it is necessary to satisfactorily characterize the maximum propagation delay of the adder. To characterize 4-bit Ripple Carry Adder (RCA), ideally 261,632 input transitions are required [1], which is a humongous number. In this paper, we have proposed a method to estimate maximum propagation delay of 4-bit RCA, using only 44 input transitions (applied as primary-secondary and subsequently as secondary-primary). We applied our proposed method on 4-bit RCAs designed using seven different Full Adder (FA) circuits and simulated them in LTspice. The results from our proposed method (reduced input transitions) are compared with the results obtained by applying 261,632 input transitions (all possible transitions) to the 4-bit RCA. The simulation results prove that the maximum delay estimated by our proposed method is very close to the exact maximum delay of 4-bit RCA (found by applying ideal 261,632 input transitions), and has maximum 5.99% deviation.

Keywords: Ripple Carry Adder · Delay estimation

1 Introduction

Almost all processing devices (e.g. microprocessor, DSP processors, etc.) contain arithmetic unit inside them, and adders are the basic building blocks of the arithmetic unit. Apart from addition operation, adders are also used in other operations, such as: subtraction, multiplication, division, etc. The maximum clock frequency of the processing device depends on the delay of the arithmetic unit; hence, it is necessary to satisfactorily characterize the maximum propagation delay of the adder.

Different input test patterns have been suggested in literature to estimate maximum propagation delay of Full Adder (FA) and Ripple Carry Adder (RCA) [1–4] using reduced input transitions; however, all these input test patterns underestimate the delay of RCA, as compared to the exact maximum propagation delay (found by applying all possible input transitions) of FA and RCA. As suggested in [1], to characterize n -bit RCA ideally $2^{(2n+1)}(2^{(2n+1)}-1)$ input transitions are required, which is a humongous number, when n is large.

In this paper, we suggest a new method (modified average delay method) to estimate maximum propagation delay of 4-bit RCA, and we have compared our result with the exact maximum propagation delay found by applying all possible input transitions (261,632 input transitions for 4-bit RCA) and maximum propagation delay estimated by input test pattern suggested in [1]. Rest of the paper is organized as follows: Sect. 2 discusses our input test pattern to estimate maximum propagation delay of individual FA of 4-bit RCA. In Sect. 3, we introduce the average delay method to estimate maximum propagation delay of 4-bit RCA. Simulation environment for 4-bit RCA is shown in Sect. 4. Section 5 includes simulation results and comparison. Finally, conclusion is drawn out in Sect. 6.

2 Input Test Pattern to Estimate Maximum Propagation Delay of Individual FA of 4-bit RCA

To estimate maximum propagation delay of a FA, we need to provide 44 input transitions [1]. An n -bit RCA consists of n FAs. Hence, to estimate maximum propagation delay of each FAs within the RCA, each FA of the RCA should be provided 44 input transitions [1]. All three inputs of FA_0 (i.e. the FA in the Least Significant Bit (LSB) position) of 4-bit RCA can be controlled directly, but the input carry (C_{in}) of the remaining three FAs of 4-bit RCA cannot be controlled directly. Hence, the C_{in} of all FAs (except the LSB FA) of 4-bit RCA should be controlled indirectly. Figure 1 shows our primary-secondary input test pattern pair which contains 44 input transitions in each (as suggested in [1]). These primary-secondary input test patterns are designed such that individual FA of RCA can be forced to all possible 44 input transitions irrespective of its position in RCA. Primary input test pattern contains required 44 input transitions for individual FA and is also capable of regenerating required C_{in} signal for secondary input test pattern. The secondary input test pattern is not used to characterize FA, but used to regenerate required C_{in} signal for primary input test pattern. In other words, the required C_{in} signal of the primary pattern is automatically generated by the previous secondary pattern, and the required C_{in} signal of the secondary pattern is automatically generated by the previous primary pattern. This alternating behavior of patterns, allows us to indirectly apply all the important input transitions to each alternative FAs of 4-bit RCA.

A	0 0 0 0 0 0 0 1 0 1 0 1 0 1 0 0 0 1 0 1 0 1 0 0 0 1 0 1 0 1 0 1 0 1 1 1 1 1 1 1 1 1 1 0
B	0 0 0 1 0 1 0 1 0 0 0 0 0 1 0 1 0 1 0 0 0 1 0 1 1 1 1 0 1 1 1 1 1 0 1 1 0 0 0 1 0 1 0 1 1 1 0
Cin	0 1 0 0 0 1 0 0 0 1 0 0 0 1 1 1 1 1 1 0 1 1 0 1 0 1 0 0 0 1 1 0 1 1 0 1 0 0 0 1 1 1 0 1 0
Primary	
A	0 1 0 0 0 0 0 1 0 1 0 0 0 1 1 0 1 1 1 0 1 1 0 0 0 1 0 0 0 1 0 1 0 1 1 1 1 0 1 1 1 0 1 0
B	0 1 0 1 0 1 0 1 0 0 0 0 0 0 0 1 1 1 1 0 1 0 1 1 1 1 1 0 1 0 1 1 1 0 1 1 0 0 0 0 0 1 0 1 0 1 0
Cin	0 0 0 0 0 1 0 0 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 1 0 1 1 0 1 0 1 0 1 1 1 1 1 1 0
Secondary	

Fig. 1. Primary-secondary input test pattern (44 transitions in each)

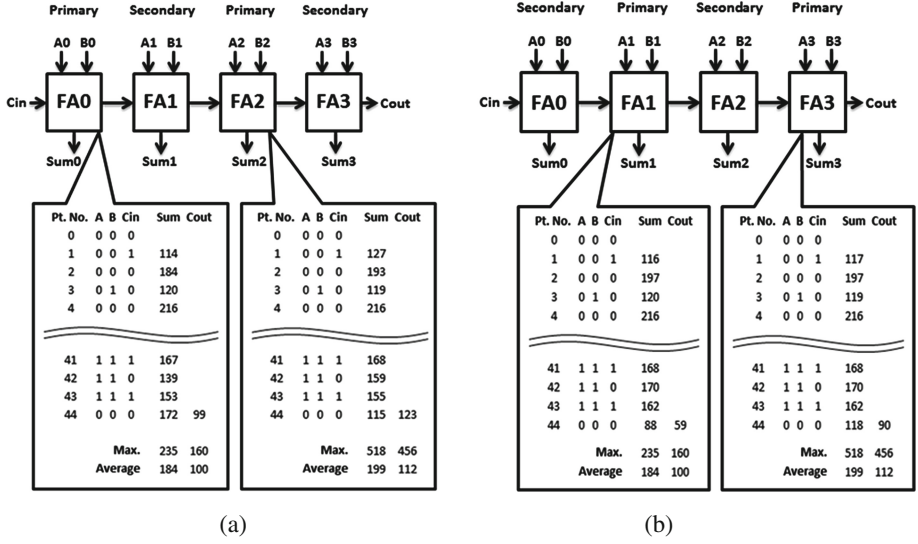


Fig. 2. Example for 28T CMOS [5] based 4-bit RCA (a) Primary-secondary arrangement and measured propagation delay (for Sum and C_{out} signals) of even numbered FAs (b) Primary-secondary arrangement and measured propagation delay of odd numbered FAs [all delays are in ps]

As shown in Fig. 2(a), to find maximum propagation delay of the even numbered FAs in 4-bit RCA, primary input test pattern should be provided to FA_0 (LSB FA) and FA_2 , and secondary input test pattern should be provided to FA_1 and FA_3 . Figure 2(b) shows the arrangement to find out maximum propagation delay of odd numbered FAs (FA_1 and FA_3) in 4-bit RCA. A , B and C_{in} column in dialog boxes of Fig. 2 shows the binary inputs applied to individual FA of 4-bit RCA; and Sum and C_{out} column shows delay for each transition (i.e., {000} to {001}, {001} to {000} etc.). Maximum and average delays of individual FA of 4-bit RCA are shown at the bottom of the dialog boxes.

Using primary-secondary input test pattern, delays of individual FA of 4-bit RCA are measured in two steps; first, delays are measured for even numbered FAs (FA_0 and FA_2) and in second step delays are measured for odd numbered FAs (FA_1 and FA_3). Simply adding maximum propagation delays of individual FAs of 4-bit RCA does not lead to correct estimation of maximum propagation delay of 4-bit RCA. The reason is that, (based on our simulations/observations) the maximum propagation delays of MSB FAs (FA_2 and FA_3) are drastically influenced by the glitches generated from LSB FAs (FA_0 and FA_1), leading to the increase in the maximum propagation delay for MSB FAs. The particular transition(s) that causes the exact maximum propagation delay (among all possible 261,632 input transitions) for 4-bit RCA may not necessarily have glitches due to LSB FAs, and hence, simple addition of maximum propagation delays of individual FAs of 4-bit RCA overestimates the maximum propagation delay of 4-bit RCA. In case of 28T CMOS FA based 4-bit RCA [5], exact maximum carry propagation delay (C_{in} to C_{out}) is found to be 615 ps, whereas, the estimated maximum carry

propagation delay (by adding maximum delays of individual FAs) is 1192 ps, which is an overestimation.

The primary-secondary input test pattern pair also contains 20 input transitions, which cause the carry to propagate from C_{in} to C_{out} and 12 input transitions which cause the carry to propagate from C_{in} to Sum_3 . However, these transitions are very few as compared to all possible carry propagation transitions (causing propagation of C_{in} to C_{out} , and propagation of C_{in} to Sum_3) for the 4-bit RCA. Hence, it may underestimate maximum propagation delay of 4-bit RCA. Maximum carry propagation delay estimated using 20 transitions for 28T CMOS FA based 4-bit RCA is 573 ps, which is an underestimation, as compared to the exact maximum carry propagation delay (615 ps).

3 Average Delay Method to Estimate Maximum Propagation Delay of 4-bit RCA

The average delay of FA (found using the arrangement in Fig. 2) captures its behavior (relative to its position) in the RCA. Some FAs are designed with good driving capacity, and hence, average delay of each FA in RCA is nearly same; while other FAs that do not have good driving capacity, have increasing average delay for each successive FA in the RCA. This statement is supported by the simulations carried out on 4-bit RCAs designed using seven different FAs [5–10]. 28T CMOS FA [5] and Chang FA [6] generate C_{out} using inverters and Mariano FA [7] is designed such that the C_{in} cannot be directly connected to Sum or C_{out} for any input condition. Hence, these FAs have good driving capacity, and simulation results (Fig. 3) shows that the average delay of these individual FAs of 4-bit RCA does not drastically change for each successive FA in the RCA. On the other hand, Narasimha FA [8], Bhattacharyya FA [9], TFA FA [10] and TG CMOS FA [10] have compromised driving capacity, when used within RCA. For these FAs, average delay is increasing for each successive FA in the RCA. From our observations, we can conclude that, average delay of FA provides enough information about its behavior within the RCA.

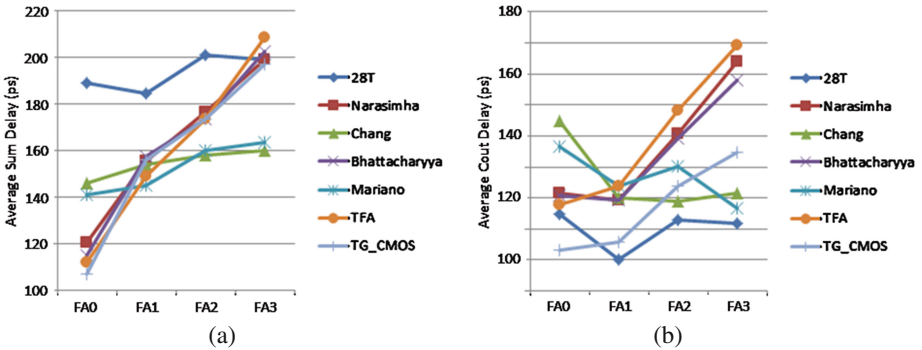


Fig. 3. Average Sum and C_{out} Delay of 4-bit RCA designed using 7 different FAs

Table 1. Calculation steps to estimate maximum propagation delay using average delay method

	Step 2		Step 3		Step 4		Step 5	
	Avg. Sum	Avg. C _{out}	Diff. Sum	Diff. C _{out}	Div. Sum	Div. C _{out}	Max. Sum	Max. C _{out}
FA ₀	189	115	0	0	0	0	235	157
FA ₁	184	100	(184 - 189) = -5	(100 - 115) = -15	(-5/184) = -0.027	(-15/100) = -0.15	(-0.027 * 235) + 235 = 229	(-0.15 * 157) + 157 = 133
FA ₂	201	113	(201 - 189) = 12	(113 - 115) = -2	(12/201) = 0.06	(-2/113) = -0.018	(0.06 * 235) + 235 = 249	(-0.018 * 157) + 157 = 154
FA ₃	119	112	(199 - 189) = 10	(112 - 115) = -3	(10/119) = 0.05	(-3/112) = -0.027	(0.05 * 235) + 235 = 247	(-0.027 * 157) + 157 = 153
Step 6			Max. Propagation Delay				157 + 133 + 154 + 247 = 691 ps	157 + 133 + 154 + 153 = 597 ps

Following steps are carried out to estimate maximum propagation delay of 4-bit RCA (for both, sum and carry), using the average delay of each FA (as per arrangement in Fig. 2) of 4-bit RCA:

1. Provide primary pattern to each FA of RCA using primary-secondary input test pattern (As discussed in Sect. 2).
2. Find the average of the delays (for both, *Sum* and *C_{out}*) for each individual FA of the RCA (See Fig. 2). (Refer columns 2 and 3 of Table 1; example is for 28T CMOS FA based 4-bit RCA).
3. Take the difference of average delays of FA₁, FA₂ and FA₃ of 4-bit RCA, with average delay of FA₀. For FA₀, this difference is zero but for FA₁, FA₂ and FA₃, differences could be either negative, positive or zero. (Refer columns 4 and 5 of Table 1).
4. Divide these differences with the average delays of individual FA of RCA (Refer columns 6 and 7 of Table 1). These values corresponding to individual FAs of RCA are used to estimate maximum *Sum* and *C_{out}* delay for the individual FAs, in the next step (i.e. step 5).
5. Multiply values obtained in step 4 with the maximum *Sum* and *C_{out}* delays of FA₀ (found as per arrangement in Fig. 2), and add it with the maximum *Sum* and *C_{out}* delays of FA₀ (Refer columns 8 and 9 of Table 1). This will provide estimated maximum *Sum* and *C_{out}* delays for each FA of 4-bit RCA.
6. Finally, add maximum *C_{out}* delays of FA₀, FA₁ and FA₂ with the maximum *Sum* delay of FA₃ to estimate maximum sum delay (propagation delay from *C_{in}* to *Sum₃*) of 4-bit RCA. Similarly, add maximum *C_{out}* delays of all FAs to estimate maximum carry delay (propagation delay from *C_{in}* to *C_{out}*) of 4-bit RCA. (Refer last row of Table 1).

Our proposed average delay method (exemplified by above steps) suppresses the effect of glitches, when estimating the maximum propagation delay of individual FA of the RCA. These maximum propagation delay values of FAs (step 5), can be used to estimate maximum propagation delay of 4-bit RCA (as suggested in step 6). The estimated maximum propagation delays (for sum and carry both) for 4-bit RCA

designed using seven different FAs are shown in Table 2. We can clearly see the difference between maximum propagation delay estimated by average delay method and exact maximum propagation delay. Average delay method over estimates maximum propagation delay of sum for most of the cases. This is because, the transition causing the exact maximum propagation delay (for the RCA) may not lead to maximum propagation delay (simultaneously) on all the individual FAs. Hence, it overestimates maximum sum propagation delays of 4-bit RCA in most cases. There same reasoning is true for the maximum carry propagation delay for 4-bit RCA designed using Chang, TFA, TG CMOS and Mariano FAs.

Table 2. Delay estimation for 4-bit RCA using average delay method and modified average delay method (All numbers are in ps)

4-bit RCA designed using	All input transitions		Average delay method		Primary-secondary		Modified average delay method	
	Sum	Carry	Sum	Carry	Sum	Carry	Sum	Carry
28T CMOS [5]	697	615	691	597	653	573	$(691 + 653)/2 = 672$	$(597 + 573)/2 = 585$
Chang [6]	701	744	861	745	541	709	$(861 + 541)/2 = 701$	$(745 + 709)/2 = 727$
Mariano [7]	651	654	825	733	555	633	$(825 + 555)/2 = 690$	$(733 + 633)/2 = 683$
Narasimha [8]	830	846	841	823	788	791	$(841 + 788)/2 = 815$	$(823 + 791)/2 = 807$
Bhattacharyya [9]	936	983	969	935	868	915	$(969 + 868)/2 = 919$	$(935 + 915)/2 = 925$
TFA [10]	971	1058	1099	1071	836	1040	$(1099 + 836)/2 = 968$	$(1071 + 1040)/2 = 1056$
TG CMOS [10]	770	751	860	813	674	736	$(860 + 674)/2 = 767$	$(813 + 736)/2 = 775$

We observed that the average delay method tends to overestimate the maximum propagation delay; and 20 transitions (for C_{in} to C_{out}) and 12 transitions (for C_{in} to Sum_3) of primary-secondary input test pattern (discussed in Sect. 2) underestimates the maximum propagation delay. A more correct estimation of maximum sum and carry propagation delays for 4-bit RCA can be obtained by averaging the sum and carry delay values of average delay method and $18 + 12$ transitions of primary-secondary input test pattern. We call it the modified average delay method. Simulation results and calculations for modified average delay method are also shown in Table 2.

This modified average delay method is only applicable if the input test pattern is able to force all FAs of RCA to all possible 44 input transitions (i.e., input test pattern shown in Fig. 1) Otherwise it calculates wrong average delay of each FA of RCA and draws us towards the wrong estimation of maximum propagation delay.

4 Simulation Environment

4-bit RCAs based on seven different FAs were designed and simulated in LTspice using BSIMv4 22 nm model (level = 54). Maximum frequency of the inputs was 200 MHz. Test bed used for simulation of 4-bit RCA is shown in Fig. 4 [11–15]. Input inverters are used to generate realistic inputs for 4-bit RCA, and the output inverters are used to introduce load at the output of the 4-bit RCA. Numbers in Fig. 4 indicate the gate width in nano meter (nm).

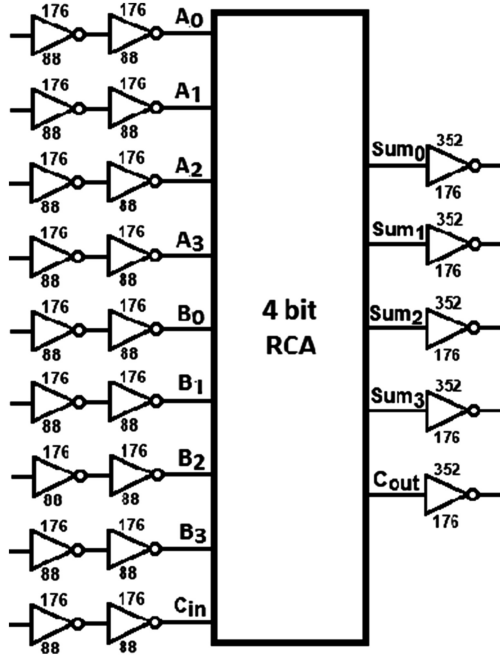


Fig. 4. Test bed used for 4-bit RCA (All numbers are in nm)

As discussed in Sect. 1, to characterize n -bit RCA ideally $2^{(2n+1)}(2^{(2n+1)} - 1)$ input transitions are required. In case of 4-bit RCA, ideally 261,632 input transitions are required. Among these 261,632 input transitions only 24,000 transitions cause carry to propagate throughout the 4-bit RCA (found using analysis done in MATLAB). The Piecewise Linear (PWL) files listing input transitions were also generated using MATLAB. Voltage values/waveforms of all input and output transitions of the 4-bit RCA, from LTspice simulations, were exported, and then analyzed using MATLAB.

5 Simulation Results

Table 3 shows the maximum sum and carry propagation delay results for 4-bit RCA designed using seven different FAs. Maximum sum and carry propagation delay results are obtained by applying all possible 261,632 input transitions, average delay method, modified average delay method, and input test pattern suggested in [1]. Table 4 shows the percentage deviation of the delays estimated by average delay method, modified average delay method and input test pattern suggested in [1], as compared to the exact delays obtained after applying all possible 261,632 input transitions.

As shown in Table 4, modified average delay method shows a maximum 5.99% (overestimation) deviation for sum delay for Mariano FA based 4-bit RCA, and maximum 5.9% (underestimation) deviation for carry delay for Bhattacharyya FA based 4-bit RCA. Results obtained for pattern suggested in [1], shows a maximum

22.82% (underestimation) deviation for sum delay for Chang FA based 4-bit RCA, and maximum 6.92% (underestimation) deviation for carry delays for Bhattacharyya FA based 4-bit RCA.

Table 3. Maximum propagation delay results (All numbers are in ps)

4-bit RCA designed using	All input transitions		Average delay method		Modified average delay method		Pattern suggested in [1]	
	Sum	Carry	Sum	Carry	Sum	Carry	Sum	Carry
28T CMOS [5]	697	615	691	597	672	585	653	572
Chang [6]	701	744	861	745	701	727	541	709
Mariano [7]	651	654	825	733	690	683	555	633
Narasimha [8]	830	846	841	823	815	807	789	791
Bhattacharyya [9]	936	983	969	935	919	925	868	915
TFA [10]	971	1058	1099	1071	968	1056	836	1040
TG CMOS [10]	770	751	860	813	767	775	674	736

Table 4. Percentage deviations in estimated delay compared to exact delay

4-bit RCA designed using	Average delay method		Modified average delay method		Pattern suggested in [1]	
	Sum	Carry	Sum	Carry	Sum	Carry
28T CMOS [5]	-0.86	-2.93	-3.59	-4.88	-6.31	-6.99
Chang [6]	22.82	0.13	0	-2.28	-22.82	-4.7
Mariano [7]	26.73	12.08	5.99	4.43	-14.75	-3.21
Narasimha [8]	1.33	-2.72	-1.81	-4.61	-4.94	-6.5
Bhattacharyya [9]	3.53	-4.88	-1.82	-5.9	-7.26	-6.92
TFA [10]	13.18	1.23	-0.31	-0.19	-13.9	-1.7
TG CMOS [10]	11.69	8.26	-0.39	3.2	-12.47	-2
	26.73	12.08	5.99	5.9	22.82	6.99

6 Conclusion

Our proposed method provides a satisfactory estimation of maximum propagation delay of 4-bit RCA, using only 44 input transitions (primary-secondary input test pattern), and based on our average delay analysis. Our proposed method requires only 44 input transitions (applied as primary-secondary and subsequently as secondary-primary) to find the maximum propagation delay for 4-bit RCA, as opposed to 261,632 input transitions. This is a significant reduction in the characterization time and effort. Our proposed method shows a maximum 5.99% deviation for sum delay and 5.9% deviation

for carry delay, as compared to the exact delays. Our proposed method has satisfactorily worked on RCA based on seven different FA circuits, and hence, our method has the potential to be applied to other FAs not considered in this work.

References

1. Mewada, M., Zaveri, M.: An input test pattern for characterization of a full-adder and n-bit ripple carry adder. In: 2016 International Conference on Advances in Computing, Communications and Informatics (ICACCI), pp. 250–255. IEEE (2016)
2. Shams, A.M., Bayoumi, M.A.: A framework for fair performance evaluation of 1-bit full adder cells. In: 42nd Midwest Symposium on Circuits and Systems, 1999, vol. 1, pp. 6–9. IEEE (1999)
3. Mewada, M., Zaveri, M.: An improved input test pattern for characterization of full adder circuits. *Int. J. Res. Sci. Innov.-IJRSI* **3**(1), 222–226 (2015)
4. Bushnell, M., Agrawal, V.: *Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits*, vol. 17. Springer Science & Business Media, New York (2004) <https://doi.org/10.1007/b117406>
5. Zimmermann, R., Fichtner, W.: Low-power logic styles: CMOS versus pass-transistor logic. *IEEE J. Solid-State Circuits* **32**(7), 1079–1090 (1997)
6. Chang, C.H.: A review of 0.18-um full adder performances for tree structured arithmetic circuits. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* **13**(6), 686–695 (2005)
7. Aguirre-Hernandez, M., Linares-Aranda, M.: CMOS full-adders for energy-efficient arithmetic applications. *IEEE Trans. Very Large Scale Integr. VLSI Syst.* **19**(4), 718–721 (2011)
8. Konijeti, N.R., Ravindra, J.V.R., Yagateela, P.: Power aware and delay efficient hybrid CMOS full-adder for ultra deep submicron technology. In: 2013 European Modelling Symposium (EMS), pp. 697–700. IEEE (2013)
9. Bhattacharyya, P., Kundu, B., Ghosh, S., Kumar, V., Dandapat, A.: Performance analysis of a low-power high-speed hybrid 1-bit full adder circuit. *IEEE Trans. Very Large Scale Integr. VLSI Syst.* **23**(10), 2001–2008 (2015)
10. Shams, A.M., Darwish, T.K., Bayoumi, M.A.: Performance analysis of low-power 1-bit CMOS full adder cells. *IEEE Trans. Very Large Scale Integr. VLSI Syst.* **10**(1), 20–29 (2002)
11. Goel, S., Kumar, A., Bayoumi, M.A.: Design of robust, energy-efficient full adders for deep-submicrometer design using hybrid-CMOS logic style. *IEEE Trans. Very Large Scale Integr. VLSI Syst.* **14**(12), 1309–1321 (2006)
12. Zhang, M., Gu, J., Chang, C.H.: A novel hybrid pass logic with static CMOS output drive full-adder cell. In: *Proceedings of the 2003 International Symposium on Circuits and Systems, ISCAS 2003*, vol. 5, p. V. IEEE (2003)
13. Aranda, M.L., Báez, R., Diaz, O.G.: Hybrid adders for high-speed arithmetic circuits: a comparison. In: 2010 7th International Conference on Electrical Engineering Computing Science and Automatic Control (CCE), pp. 546–549. IEEE (2010)
14. Yeo, K.S., Roy, K.: *Low Voltage, Low Power VLSI Subsystems*. McGraw-Hill, Inc., New York (2009)
15. Shubin, V.V.: New high-speed CMOS full adder cell of mirror design style. In: 2010 International Conference and Seminar on Micro/Nanotechnologies and Electron Devices (EDM), pp. 128–131. IEEE (2010)

VLSI Design and Test

21st International Symposium, VDAT 2017, Roorkee,
India, June 29 – July 2, 2017, Revised Selected Papers

Kaushik, B.K.; Dasgupta, S.; Singh, V. (Eds.)

2017, XXI, 815 p. 486 illus., Softcover

ISBN: 978-981-10-7469-1