

Contents

1	Embedded Memories: Introduction	1
1.1	Increasing Need for Embedded Memories in Low-Power VLSI SoCs	1
1.2	Memory Requirements of Various Low-Power VLSI SoCs	4
1.3	Brief Review of the State of the Art	8
1.4	Book Outline	9
	References	10
2	Gain-Cell eDRAMs (GC-eDRAMs): Review of Basics and Prior Art	13
2.1	Basics of GC-eDRAM	13
2.2	Advantages and Drawbacks of GC-eDRAM	14
2.3	Review of Prior-Art GC-eDRAM Circuit Techniques and Target Applications	16
2.3.1	Categorization of GC-eDRAM Implementations	16
2.3.2	Comparison of the State-of-the-Art Implementations	18
2.3.3	Circuit Techniques for Target Applications	19
2.3.4	Summary and Conclusions	23
	References	24
3	Retention Time Modeling: The Key to Low-Power GC-eDRAMs	27
3.1	Introduction	27
3.2	Choice of Basic 2T GC-eDRAM Bitcell	28
3.3	Analytical GC-eDRAM Retention Time Model	30
3.3.1	Definition of Retention Time	30
3.3.2	Analytical Model of Nominal EDRT	31
3.3.3	Statistical Distribution of EDRT	32
3.4	Model Validation Through Circuit Simulations	33
3.4.1	Nominal EDRT	33
3.4.2	Statistical EDRT Distribution	35

3.5	Model Validation Through Silicon Measurements of 0.18 μm CMOS Test Arrays	36
3.5.1	Test Chip Design	36
3.5.2	Measurement Results	37
3.6	Sensitivity Analysis of GC-eDRAM Retention Time	41
3.6.1	Plackett-Burman Design of Experiment (PB-DOE)	41
3.6.2	PB-DOE Applied to GC-eDRAM RT	42
3.6.3	Impact of Process Corner	44
3.7	Best-Practice 2T GC Design	45
3.8	Conclusions	46
	References	46
4	Conventional GC-eDRAMs Scaled to Near-Threshold Voltage (NTV)	49
4.1	Introduction	49
4.2	2T GC, Array, and Macrocell Optimized for NTV Operation	51
4.2.1	2T Two-Port GC and Array Architecture	51
4.2.2	Operation Principle	52
4.3	Impact of Voltage Scaling on GC-eDRAM Retention Time	54
4.3.1	Worst-Case Access	54
4.3.2	Retention Mode	56
4.4	Macrocell Implementation Results	57
4.5	Conclusions	58
	References	59
5	Novel Bitcells and Assist Techniques for NTV GC-eDRAMs	61
5.1	Introduction	61
5.2	Single-Supply Transmission-Gate (TG) 3T-Bitcell GC-eDRAM	62
5.2.1	Proposed 3T TG Gain-Cell	63
5.2.2	Peripheral Circuits	66
5.2.3	Macrocell and Test Chip Design	69
5.2.4	Lab Setup and Silicon Measurements	71
5.3	Impact of Body Biasing (BB) on Retention Time	73
5.3.1	Bitcell Design for Body Biasing Experiment	74
5.3.2	Macrocell Architecture and Test Chip Design	75
5.3.3	Silicon Measurements	76
5.4	Replica Technique for Optimum Refresh Timing	78
5.4.1	Conventional Design for Worst-Case Retention Time	78
5.4.2	Replica Technique Concept	81
5.4.3	Replica Technique Integration into Gain-Cell Array	82
5.4.4	Testing and Characterization Procedure	84
5.4.5	Silicon Measurements	85
5.5	Conclusions	87
	References	89

6 Aggressive Technology and Voltage Scaling (Down to the Subthreshold Domain)	91
6.1 Introduction	91
6.2 Retention Time Model Validation for 28 nm CMOS	92
6.3 2T Gain Cells Optimized for Subthreshold Operation	93
6.3.1 2T Gain-Cell Implementation Alternatives	93
6.3.2 Best-Practice Write Transistor Implementation	96
6.3.3 Best-Practice Read Transistor Implementation	99
6.3.4 Storage Node Capacitance and WWL Underdrive Voltage	100
6.4 Macrocell Implementation in 0.18 μm CMOS	104
6.5 Macrocell Implementation in 40 nm CMOS	106
6.6 Conclusions	109
References	110
7 Novel Bitcells for Scaled CMOS Nodes and Soft Error Tolerance	113
7.1 Introduction	113
7.2 4T GC with Internal Feedback (IFB) for Scaled CMOS Nodes	114
7.2.1 Cell Structure and Operating Mechanism	114
7.2.2 Implementation and Simulation Results	117
7.3 Redundant 4T GC for Soft Error Tolerance	120
7.3.1 Radiation-Hardened Memories	121
7.3.2 Proposed 4T CDMR Dynamic Memory Array	123
7.3.3 Implementation	126
7.4 Conclusions	132
References	133
8 Conclusions	135
8.1 Summary	135
8.1.1 Near- V_T GC-eDRAM Techniques	136
8.1.2 Sub- V_T and Deeply Scaled GC-eDRAM Techniques	137
8.2 Outlook	138
Glossary	141
Index	143

Gain-Cell Embedded DRAMs for Low-Power VLSI
Systems-on-Chip

Meinerzhagen, P.; Teman, A.; Giterman, R.; Edri, N.;
Burg, A.; Fish, A.

2018, IX, 146 p. 84 illus. in color., Hardcover

ISBN: 978-3-319-60401-5