

Chapter 2

ADC Architecture

2.1 Introduction

While lots of Nyquist-rate ADCs are proposed to resolve resolutions at different speeds throughout the years, there are three types of architectures most widely used and they are the pipelined ADC, the SAR ADC, and the flash ADC. Furthermore, the three ones all have the potential to achieve the high performance and the high-power efficiency, via the adjustment in the architecture level or with the aid of useful techniques.

2.1.1 Traditional Architectures

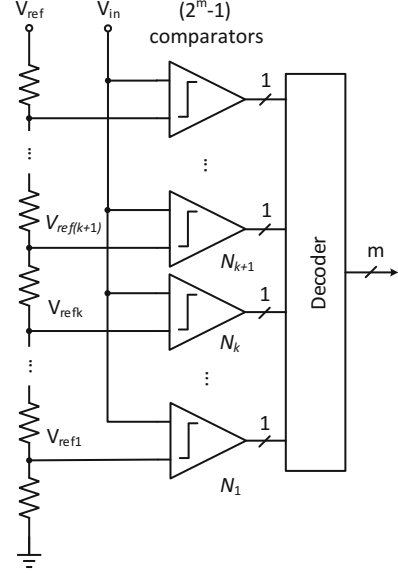
The three architectures all date back to 1900s. To authors' best knowledge, the first flash ADC was built in 1963 at Columbia University [1], and it has the property of the high speed. In 1971, the pipelined ADC was first proposed by Texas Instrument in a patent [2], the all-MOS one appears later in [3], and since then becomes flourish. Its advantage lies in the competitive tradeoff between the speed and the resolution. As to the SAR ADC, while the earliest SAR topology can be found in a 1947 paper by Bell Laboratories [4], the all-MOS SAR ADC was reported in the 1970s [5] and lays dormant until the 2000s, benefiting from the all digital implementation.

2.1.1.1 Flash ADC

A m -bit flash ADC is depicted in Fig. 2.1, consisting of $2^m - 1$ comparators, a resistor ladder and a decoder. The resistor ladder is composed of 2^m equal segments and generates $2^m - 1$ reference voltages, which compare with the analog input at the same time. Thanks to the parallelism, the architecture achieves a high-conversion rate.

Here is an example. If the input is between V_{refk} and $V_{ref(k+1)}$, the comparator N_1 , N_2, \dots , and N_k output 1, and the remaining ones output 0. The $(2^m - 1)$ -bit thermometer code is converted to the m -bit binary code via the decoder.

Fig. 2.1 Basic flash ADC architecture



2.1.1.2 Pipelined ADC

A pipelined ADC consists of cascade low-resolution stages, which are similar or identical, the synchronous block, and the correction block, as shown in Fig. 2.2. Every stage accomplishes the operation in two phases, the sampling phase and the amplification phase. When one stage amplifies the residue via the multiplying digital-to-analog converter (MDAC), the following stage samples its input and converts that to the digital code, which is described in Fig. 2.3a. The digital code is sent to the correction block through the synchronous block to obtain the final output, and the residue attaches to the following stage as its input.

Figure 2.3a illustrates the implementation of cascade 1-bit stages. A single stage consists of a sub-ADC and a MDAC. Here, 1-bit sub-ADC is implemented by one comparator. The MDAC is composed of the capacitive digital-to-analog converter (DAC) and the opamp, and the S/H block shown in Fig. 2.2 is merged in the capacitive DAC (CDAC), where $C_1 = C_2$. As shown in Fig. 2.3a, the first stage amplifies the difference between the input and the DAC's output and V_{res} is

$$V_{res} = \begin{cases} 2V_{in} - V_{ref} & V_{in} > 0 \\ 2V_{in} + V_{ref} & V_{in} < 0 \end{cases} \quad (2.1)$$

which is plotted in Fig. 2.3b. Meanwhile, V_{res} is sampled by the second stage as its input.

The amplification provided by the MDAC enables the pipelined ADC to achieve the high accuracy. The residue of the coarse conversion is so small that it is difficult to

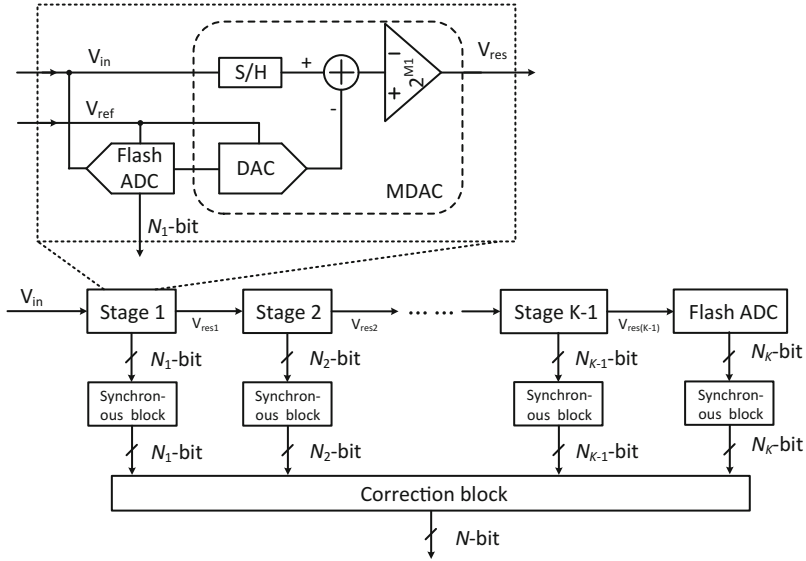


Fig. 2.2 Basic pipelined ADC architecture

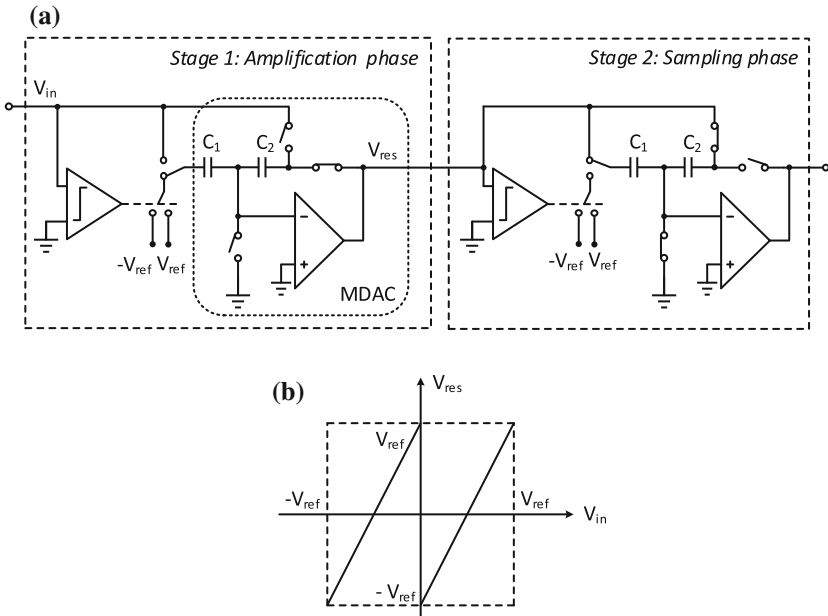


Fig. 2.3 Cascade stages: **a** the first stage operating in the amplification phase and the second one operating in the sampling phase, and **b** the input/output characteristics

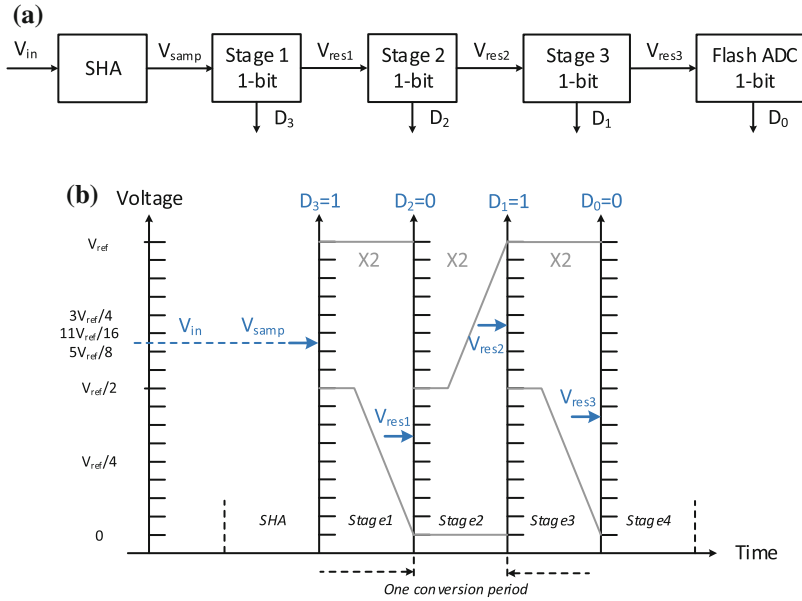


Fig. 2.4 a A 4-bit pipelined ADC and b its operation versus time

convert it precisely. Thanks to the amplification, the original residue is enlarged and the equivalent error from the following stages is compressed. Take a 4-bit pipelined ADC as an example. The ADC consists of a sample-and-hold amplifier (SHA), followed by three 1-bit stages and a 1-bit flash ADC, as shown in Fig. 2.4a. Besides, its operation versus the time is depicted in Fig. 2.4b, which can be described as follows.

1. The analog input is sampled and held by the SHA as V_{samp} .
2. The first stage compares V_{samp} with the comparator threshold, 0 Volts, outputs the code, 1, and then amplifies the original residue by 2.
3. The similar operation is accomplished by the following stages and the digital codes are 0, 1, 0, respectively.

It is noted that the amplification is absent in the last stage, because its residue does not contribute the information anymore. Due to five conversion periods spent to obtain a 4-bit code, the delay is introduced between the input and its code. Fortunately, the interval between two codes is still one period. In summary, in the pipelined ADC, every stage scales the original residue up by 2^{N_i} (N_i is the effective resolution of the i th stage shown in Fig. 2.2) to the full scale, and then the enlarged residue is converted to improve the accuracy.

2.1.1.3 SAR ADC

The interest in the SAR ADC increases for it is as digital as it can get. It derives the beauty from three properties: the ability to achieve high resolutions, the absence of opamps, and the ability to consume no static power dissipation [6].

In the view of the sampling and quantification, a SAR ADC is conceptually shown in Fig. 2.5. It is composed of a DAC, a comparator, and some logic, which are in a feedback loop. The CDAC is commonly adopted, because it can accomplish the sampling besides the digital-to-analog conversion.

For a N -bit ADC with 1 bit per cycle in Fig. 2.5, the conversion time is approximately $N(T_{COMP} + T_{DAC} + T_{logic})$, where T_{COMP} , T_{DAC} , and T_{logic} are the response time of the comparator, the DAC, and the SAR logic.

An example is taken to illustrate the operation in one period, as shown in Fig. 2.6. Once the input voltage is frozen to V_{samp} , the feedback loop begins to search its quantified value, which can be described as follows.

1. The analog input is sampled and held as V_{samp} .
2. The feedback loop sets V_{DAC} to $V_{\text{REF}}/2$ in the first cycle. Comparing V_{DAC} with the input, the first bit, 1, is generated.
3. Based on the first bit, the feedback loop sets V_{DAC} to $3V_{\text{REF}}/4$ in the second cycle. Comparing V_{DAC} with the input, the second bit, 0, is generated.
4. The similar operation is accomplished in the third and fourth conversion cycles.

After four conversion cycles, the digital output is 1010. Compared with the operation of the pipelined ADC in Fig. 2.4, in the SAR ADC, the amplification of the residue is removed and the comparator's threshold voltages change with more and more resolutions resolved.

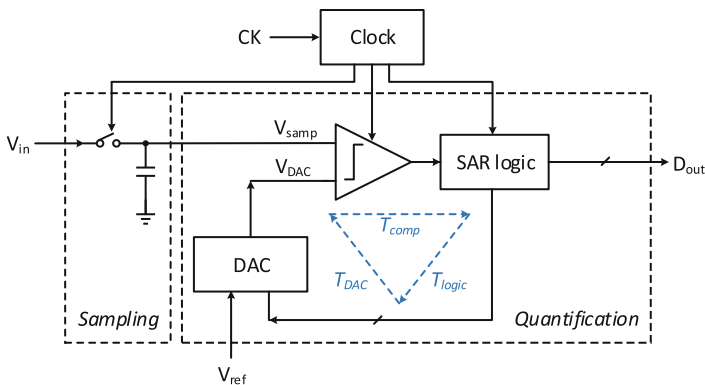


Fig. 2.5 Basic SAR architecture

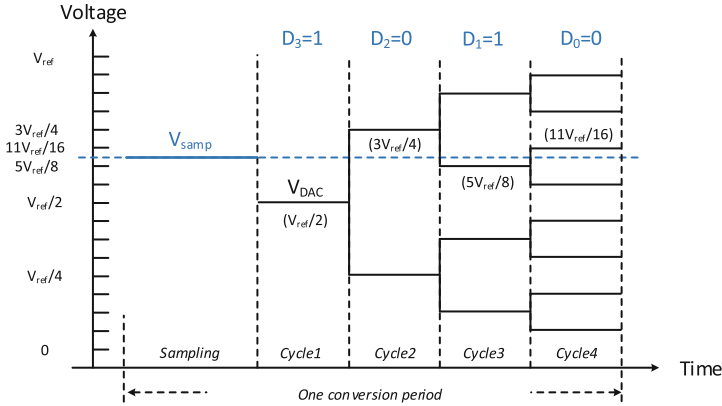


Fig. 2.6 SAR operation versus time

2.1.2 Limitations

There are limitations for the traditional architectures, the flash ADC, the pipelined ADC and the SAR ADC, to realize the high performance and the high-power efficiency.

For the flash architecture, while the parallelism helps the converter to achieve a high speed, it makes the architecture suffer from the problem of area. To obtain m -bit code, $(2^m - 1)$ comparators are needed and hence the area is enlarged at an exponential rate with the resolution. The flash architecture is commonly adopted by the ADC with the resolution of no more than 6 bits.

For the pipelined architecture, the inaccuracy is resulted in by the capacitor mismatch, the finite opamp gain, the opamp nonlinearity, the comparator offset, KT/C noise, and the opamp noise. Besides, the conversion rate is limited by the sum of the sampling time and the amplification time. The sampling time is a number of constant time of the sampling network, and the amplification time is determined by the bandwidth of the opamp.

For the SAR architecture, while it is digital and efficient, it suffers from issues if a high performance is required. First, the conversion speed is limited by the multiple clock cycles in one period. For a N -bit ADC with 1 bit per cycle, the conversion time is approximately $N(T_{COMP} + T_{DAC} + T_{logic})$. For a given CMOS process, the response time of each component is related to the power dissipation and its architecture, which cannot be neglected. The higher the resolution is, the longer the conversion period will be. Second, the resolution is limited by the property of the single stage. Since SAR topology imposes all the bits on the only one DAC, the area of the DAC limits the resolution of the SAR ADC. For example, in a differential 12 bit ADC, 8192 capacitor units are required. Considering that the capacitor unit is limited by the matching, the area occupied by the CDAC tends to be large and even can not be accepted. Third,

the accuracy is limited by the noise of the comparator. A low-noise comparator is desired, but its response time and power dissipation are usually unexpected.

2.2 Improved Pipelined ADC

Many efforts have been made to reduce the power dissipation of the pipelined ADC, which provides a good compromise between the high resolution and the high speed. The power-efficient SHA-less architecture, the multi-bit stage, and the redundancy technique are to be talked about in the section. All of them help to save the power dissipation and enhance the linearity of the ADC.

2.2.1 SHA-less Architecture

In a multistage ADC, the front-end SHA is the dominant noise, distortion and power contributor [7]. Removing the dedicated SHA and its noise, power, distortion, and area from the whole ADC budget is attractive and it has become the trend. In the SHA-less ADC, the sampling operation is distributed inside both the MDAC and flash ADC in the first stage. In other words, two sampling pathes track the input signal, instead of the unique sampling path provided by the SHA. Because of that, the aperture error is introduced and hence high-frequency input performance is challenged. The details on the aperture error and its solutions are to be discussed.

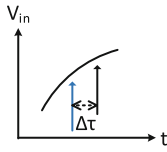
2.2.1.1 Aperture Error

Since the high-frequency input signal instead of the held signal is directly provided for the SHA-less architecture, the samples of the flash ADC and that of the MDAC may be slightly different, which is the aperture error.

Because of the aperture error, the residue falls outside the designed range. Take a 2-bit individual stage with 1-bit redundancy as an example. The ideal input/output characteristics is indicated by the black line in Fig. 2.7. The sampling instant of the flash ADC may be delayed or advanced, and the difference between the sampling instant of the flash ADC and that of the MDAC is labeled $\Delta\tau$. The difference between the flash ADC's sample and the MDAC's is labeled ΔV . Four possible combinations of the input's slope and over-range voltage's sign are identified. As is shown in Fig. 2.7, in the first and second cases, the sampled input of the flash ADC is smaller than that of the MDAC, the decision levels move right, and hence, the over-range voltage is positive. In the third and fourth cases, the sampled input of the flash ADC is bigger than that of the MDAC, the decision levels move left. And thereby, the over-range voltage is negative.

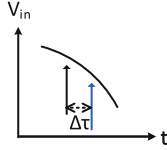
CASE 1: $OR > 0$

Slope > 0 , Flash ADC: advanced



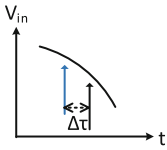
CASE 2: $OR > 0$

Slope < 0 , Flash ADC: delayed



CASE 3: $OR < 0$

Slope < 0 , Flash ADC: advanced



CASE 4: $OR < 0$

Slope > 0 , Flash ADC: delayed

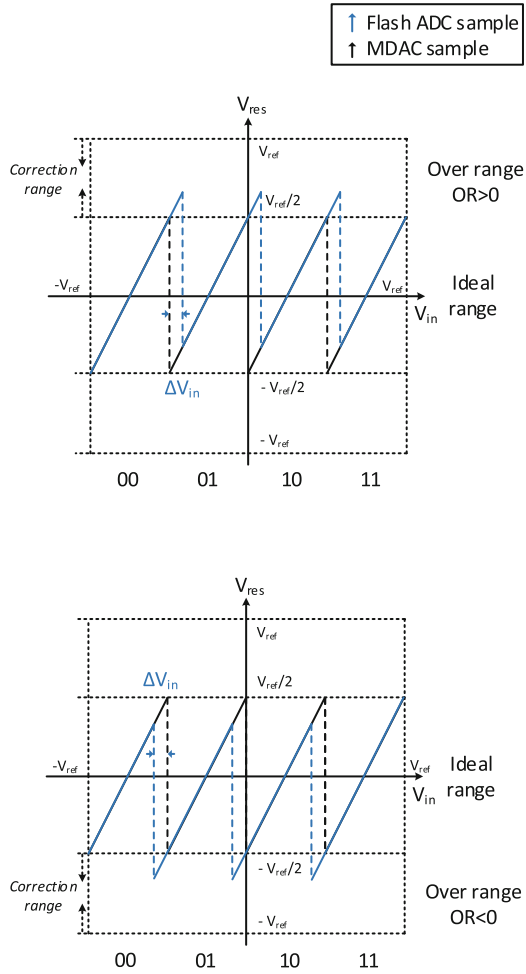
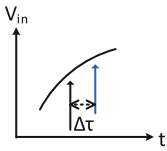


Fig. 2.7 The input/output characteristics of a 2-bit stage with the aperture error

Additionally, it should be noted that the over-range residue falls into the correction range. In other words, benefiting from the redundancy, the aperture error can be tolerated.

The aperture error limits the frequency of the analog input. Assuming the input voltage is a sinusoidal signal with the amplitude of A and the frequency of f_{in} , it can be written as

$$V_{in} = A \sin(2\pi f_{in} t) \quad (2.2)$$

The maximum sampling voltage error introduced by $\Delta\tau$ happens at the maximum slope of $2A\pi f_{in}$. Therefore,

$$V_{in,error} \leq 2A\pi f_{in} \Delta\tau \quad (2.3)$$

To realize the correct conversion, the residue voltage should not exceed the acceptable input range of the following stage. For the $(m+1)$ -bit individual stage with the redundancy of 1 bit, the tolerable input error is $\pm V_{FS}/2^{m+2}$, and thereby

$$2A\pi f_{in} \Delta\tau < \frac{V_{FS}}{2^{m+2}} \quad (2.4)$$

Assuming that the amplitude A is $V_{FS}/2$, the input frequency is limited by

$$f_{in} < \frac{1}{2^{m+2} \Delta\tau \pi} \quad (2.5)$$

Actually, $\Delta\tau$ is introduced for two reasons, the different time constant of the sampling network and different sampling instant.

In the sampling phase, both the input networks of MDAC and flash comparators track the input signal, as shown in Fig. 2.8. To provide the same time constant relative to the input, the sampling networks should satisfy [7]

$$\frac{R_{s1}}{R_{s1'}} = \frac{1/C_s}{1/C_{s'}} = \frac{R_{s2}}{R_{s2'}} = \frac{1/C_p}{1/C_{p'}} \quad (2.6)$$

where R_{s1} , $R_{s1'}$, R_{s2} , and $R_{s2'}$ are on-resistance of the sampling switches, C_s and $C_{s'}$ are the sampling capacitance, and C_p and $C_{p'}$ are the parasitic capacitance of the summing nodes. If the accurate matching cannot be realized, the aperture error appears. Besides, the sampling may happens at different instant due to the time skew between $\phi 1_p$ and $\phi 1_{p'}$. Although the unique sampling clock is provided to the networks, the parasitic resistance and capacitance in the two pathes results in slightly different RC delay. That also leads to the aperture error.

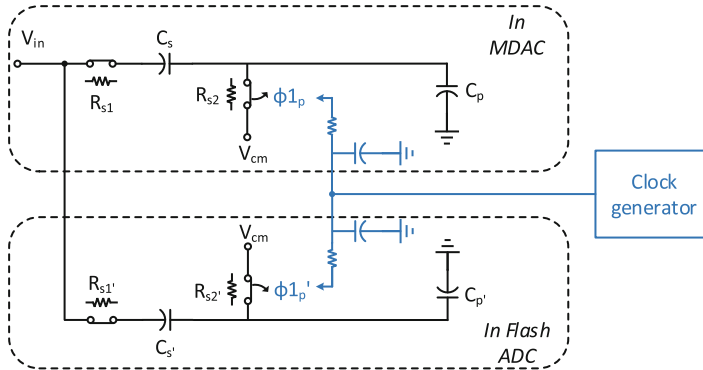


Fig. 2.8 Two input networks of MDAC and flash comparators in the sampling phase

2.2.1.2 Solutions to Aperture Error

Matching Sampling

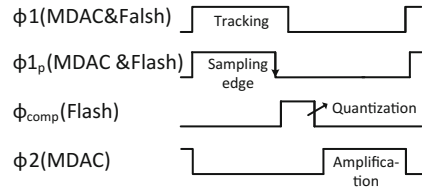
Since the aperture error is introduced by the mismatch between input networks, one of the solutions is to provide accurate matching to eliminate $\Delta\tau$ in Eq. 2.3. To realize that, the networks should be designed based on Eq. 2.6 and the high quality layout design is required.

However, one problem appears because that the sampling in the two networks is completed at the same time and there is no time left for the flash ADC to operate the normal conversion, providing the input of the MDAC in the following amplification phase. To solve that, a basic idea is to introduce an additional phase, ϕ_{comp} in Fig. 2.9, which can be adopted by the flash ADC to sample the reference voltage, redistribute the charge and make the decisions. ϕ_{comp} starts after ϕ_{1p} and ϕ_1 , which control both the MDAC and flash ADC to track and sample the input, and ends before ϕ_2 , which controls the MDAC to amplify the residue voltage. As the cost paid for eliminating the dedicated SHA, the additional phase slows down the conversion rate of the traditional two-phase pipelined ADC, which cannot be accepted by the high-speed ADC. Another approach is to add additional capacitors to sample the reference voltage in the flash ADC, and hence reduce the charge distribution time, like in [8]. The cost is the complicated circuit and timing design.

To cope with the problem in Fig. 2.9, adopting the comparator to sample the input is proposed in [9, 10]. The first stage and its timing are described in Fig. 2.10. For the flash ADC, sampling the reference voltage is accomplished in the amplification phase, ϕ_2 , which enables that the continuing subtraction between signal and threshold is done during the tracking phase, ϕ_1 . Both the MDAC and comparators sample the input at the falling edge of ϕ_{1p} . Thanks to the charge redistribution in ϕ_1 , comparators are able to make the decisions before the rising edge of ϕ_{2d} , leaving enough time for the MDAC. To track the analog input, the comparator's pre-amplifier and the input path of the flash ADC must provide large bandwidth to rapidly respond to the high-frequency input. To avoid exceeding the stage's correction range, the matching between the MDAC sampling network and the comparator is required, and hence the bandwidth of the pre-amplifier should satisfy

$$\tan^{-1} \frac{f_{in}}{f_{BWmax}} = 2\pi \frac{f_{in}}{\Delta\tau_{max}} \quad (2.7)$$

Fig. 2.9 Adjusted timing due to the aperture error



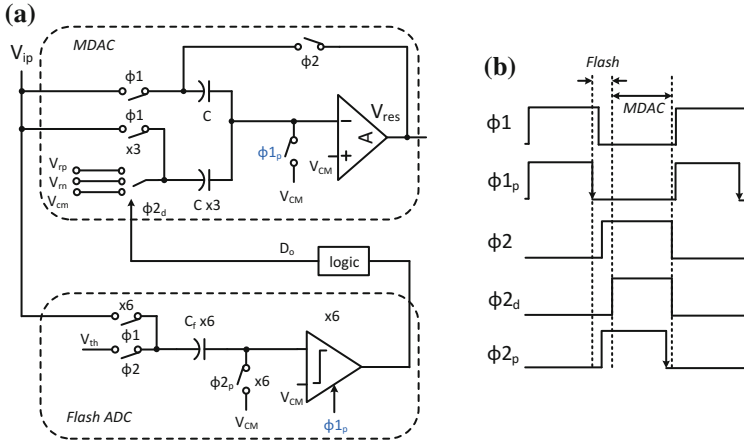


Fig. 2.10 The **a** first stage and **b** timing proposed in [9]

where $\Delta\tau_{max}$ can be obtained according to Eq. 2.4. The higher the input frequency is, the higher the bandwidth will be. This technique is verified in a 12-bit 270 MSps pipelined ADC and the measurement results are shown in Fig. 2.11. It reveals the dynamic performance for an input frequency sweep at 200 MSps and 270 MSps, (THD contains 2nd-10th harmonic). At 200 MSps, the ADC achieves the THD of 78.2 dB and the SNR of 69.5 dB for a 30.1 MHz input, and achieves the THD of 62.5 dB and the SNR of 58.9 dB for a high-frequency 195.1 MHz input. At 270 MSps, the ADC achieves the THD of 74.7 dB and the SNR of 64.4 dB for a 30.1 MHz input, and achieves the THD of 66.1 dB and the SNR of 57.3 dB for a high-frequency 195.1 MHz input. The cost of this technique is that more power is consumed in comparators. Besides, it should be noted that the total power dissipation increases at an exponential rate with the increased number of comparators in a multi-bit flash ADC, limiting the application of this technique in a multi-bit front end.

To save the power of the comparator without reducing the conversion rate, the modification of the timing is proposed in [11]. $\phi 1_a$ is introduced to enable the sampling instant to be advanced, as is shown in Fig. 2.12. The advantages are as follows.

1. The tracking time is compressed so that more time is left for comparators to make decisions. The operation time of the flash ADC is composed of the delay between the falling edge of $\phi 1_a$ and $\phi 1$ and the nonoverlapping time between $\phi 1$ and $\phi 2$.
2. From the point of view of the implementation, compared with the traditional sampling instant, $\phi 1_p$, in Fig. 2.10, the gate delay between the low-jitter clock input and $\phi 1_a$ is smaller, and thereby the jitter of $\phi 1_a$ is lower. Therefore, the proposed sampling instant is helpful to improve the sampling accuracy.

Besides, in Fig. 2.12, both input networks of the MDAC and the flash ADC accomplish the sampling at the same instant to eliminate the aperture error. Benefiting

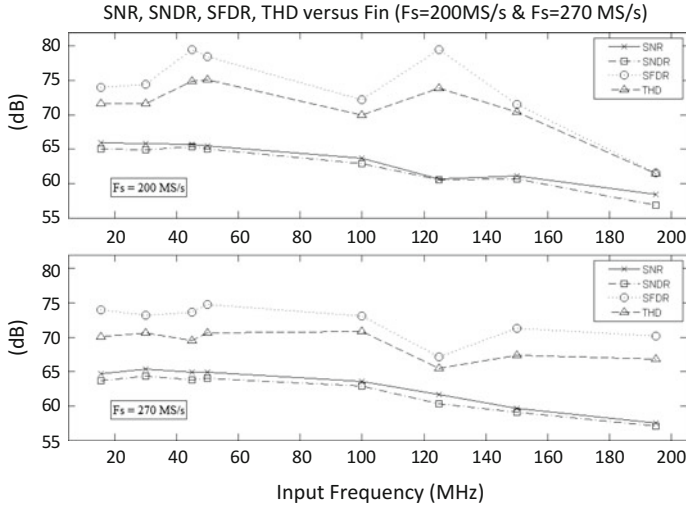


Fig. 2.11 Measured SNR, SNDR, SFDR, THD versus the input frequency

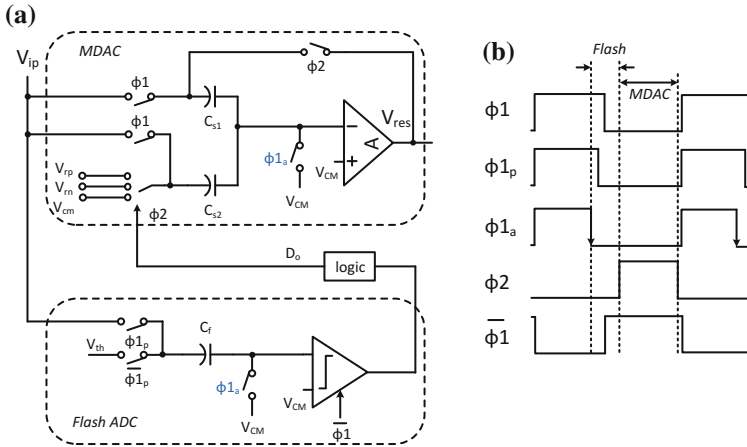


Fig. 2.12 The **a** first stage and **b** timing proposed in [11]

from the proposed timing, low-power dynamic comparator can be adopted in the flash ADC, saving the power dissipation effectively.

What's more, the requirement of the opamp's bandwidth is relaxed because of the enough time provided for the amplification. Since the opamp consumes most of power dissipation in a high-performance ADC, the power saved by it is considerable.

Calibrating Sampling

Besides matching the sampling between the MDAC and flash ADC, the calibration can be adopted by the SHA-less ADC to eliminate the aperture error. An over-range calibration is proposed in [12] and its basic idea is discussed here. It is used in a SHA-less ADC, comprising a 2.5-b MDAC, followed by a 8-b SAR ADC. With the aperture error, the residue voltage of the MDAC exceeds the ideal range, entering the correction range, and hence over range appears, as is shown in Fig. 2.13. As is discussed in Fig. 2.7, four possible combinations of the input's slope and over-range voltage's sign are identified, and the sampling instant of the flash ADC is delayed or advanced, correspondingly. The calibration works by adjusting the sampling instant of the flash ADC with respect to the MDAC's, based on the input's slope and the over-range voltage's sign. Benefit from the technique, multi-GHz input signal can be converted by the ADC. The cost of this technique is the additional power dissipation of the calibration block.

Sharing Sampling

Since the mismatch of two sampling pathes of the MDAC and flash ADC results in the aperture error, merging them into a unique sampling path can eliminate the error. An aperture error reduction technique of sharing the sampling networks is proposed and verified in a subranging SAR ADC [13]. By reusing capacitors of the flash ADC in the fine conversion phase, thermometer coarse capacitors belonging to the traditional CDAC are removed. This technique does not only minimize aperture error effectively but also reduces input capacitance. The details on the sharing sampling are to be discussed.

To illustrate the sharing sampling, the operation of the traditional and the proposed architecture are both depicted.

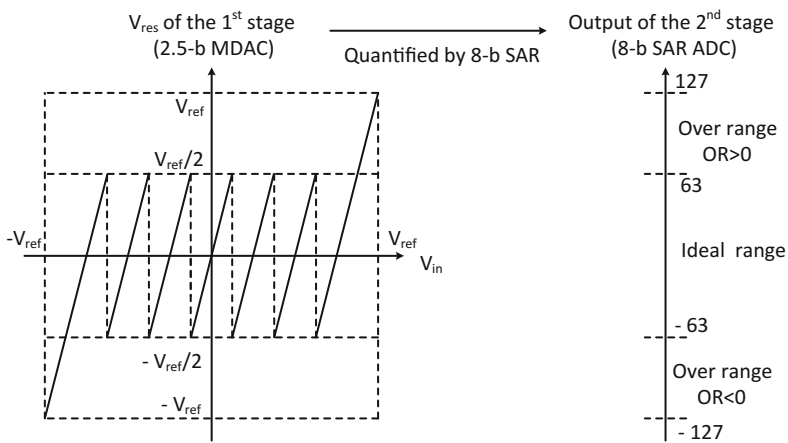


Fig. 2.13 The transfer curve of the 2.5-b MDAC in [12]

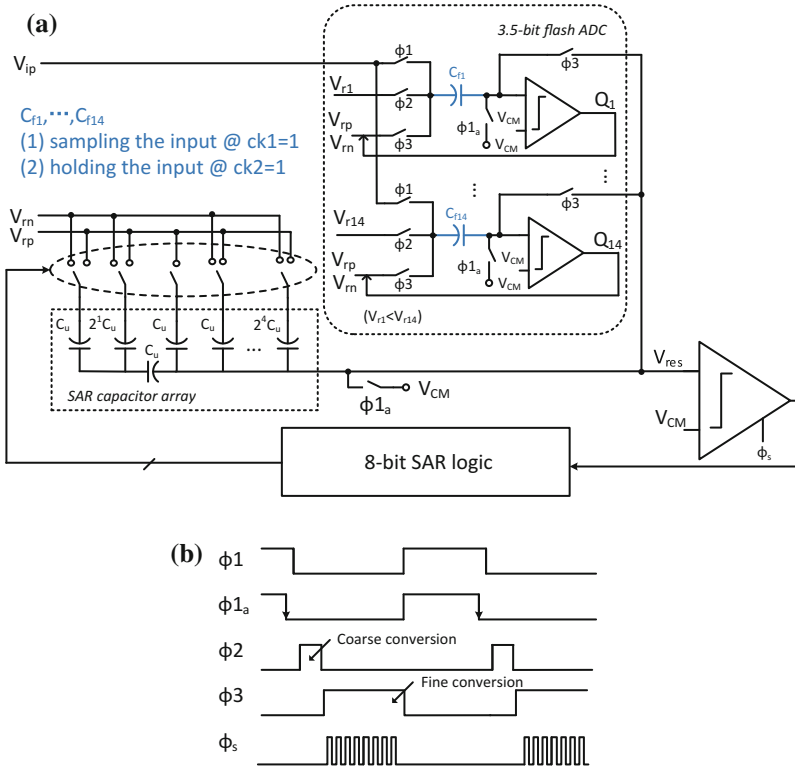
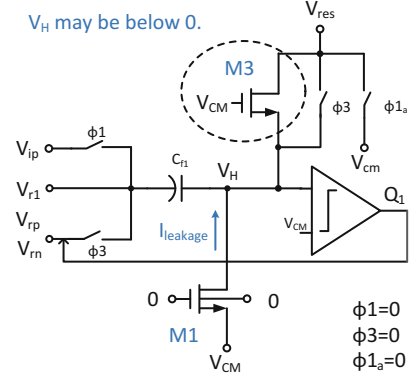


Fig. 2.14 The **a** subranging SAR ADC with aperture error reduction technique and **b** timing

1. A conventional 11-bit subranging SAR ADC without front-end T/H is depicted in Fig. 2.30a, comprising a 3.5-bit flash ADC for the coarse conversion, followed by an 8-bit SAR ADC for the fine conversion. The ADC employs two paths, capacitors C_i ($i = 1, \dots, 14$) in the CDAC and capacitors C_{fi} ($i = 1, \dots, 14$) in the flash ADC, to track the input in the sampling phase, $\phi_1 = 1$, as shown in Fig. 2.30b. And the sampling happens at the falling edge of ϕ_{1a} . When ϕ_2 is high, the flash ADC operates the coarse comparison and outputs the most significant bits (MSBs), Q_i , which control the capacitors C_i during the following fine conversion phase.
2. A SHA-less subranging SAR ADC with the sharing sampling is shown in Fig. 2.14. When ϕ_1 is high, only capacitors C_{fi} track the input and sample it at the falling edge of ϕ_{1a} . When ϕ_2 is high, the flash ADC operates the coarse conversion and outputs Q_i , just like the conventional one. Once the flash ADC conversion finishes, ϕ_3 goes high and capacitors C_{fi} and the SAR capacitor array are connected together. Q_i control the bottom plates of capacitors C_{fi} to attach to V_{rp} or V_{rn} , operating as the flash capacitor array in Fig. 2.30.

Fig. 2.15 The charge leakage error in the coarse conversion phase and the solution



Therefore, unlike the conventional SHA-less subbranging SAR ADC, the new architecture does not employ coarse capacitors C_i . The unique sampling capacitors, C_{fi} , sample the input, hold the charge, and provide the charge for the flash ADC in the coarse conversion phase and the CDAC in the fine conversion phase. Benefit from the unique sampling path, this technique does not only minimize the aperture error but also reduces the input capacitance.

Because that the principle of the technique is based on the switched-capacitor charge redistribution, any charge injection or leakage to C_{fi} is unacceptable. Actually, in the coarse conversion phase, the charge leakage may happen in the 1st or the last comparator. Take the 1st comparator in the flash ADC to illustrate that. It should be noted that V_{r1} is close to $V_{cm} - V_{ref}/2$. As is shown in Fig. 2.15, when $\phi2$ becomes high, the bottom plate of C_{f1} switches to the reference voltage V_{r1} . And the voltage at the capacitor's top plate, V_H , can be derived as

$$V_H = V_{cm} - V_{ip} + V_{r1} \quad (2.8)$$

where V_{cm} is the common-mode voltage, V_{ip} is the input signal. Considering that V_{ip} is the maximum, i.e., $V_{cm} + V_{ref}/2$, V_H can be rewritten as

$$V_H \approx V_{cm} - (V_{cm} + V_{ref}/2) + V_{cm} - V_{ref}/2 = V_{cm} - V_{ref} \quad (2.9)$$

where V_{ref} is the full scale of the single-ended input. Normally, in the SAR ADC, V_{cm} is $V_{DD}/2$, V_{ref} is V_{DD} , and hence V_H is

$$V_H \approx -V_{DD}/2 \quad (2.10)$$

In that situation, the substrate-to-drain leakage appears in switch transistor M1 and hence unexpected charge is added to C_{f1} . In the following fine conversion phase, the residue voltage, V_{res} , will deviate, decreasing the conversion accuracy of ADC. To solve the leakage, transistor M3 is introduced. If V_H drops and becomes small

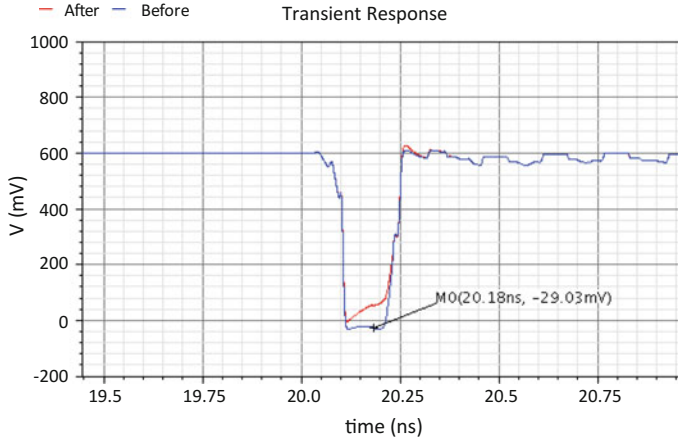


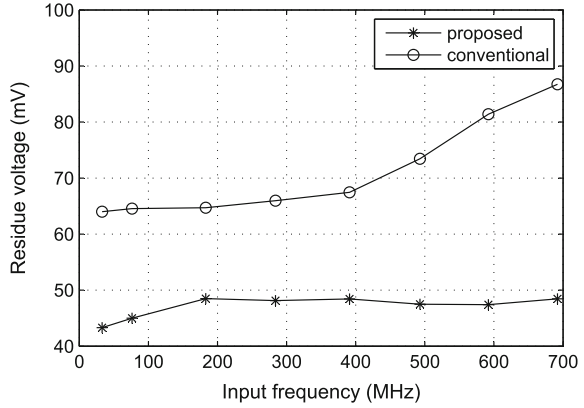
Fig. 2.16 The transient response of V_H before and after introducing M3 (simulated by Specter)

enough ($\leq -V_{th}$) to switch on M1, M3 will also switch on ($V_{gs,M3} = V_{cm} + V_{th}$) to charge the node V_H by connecting it with V_{res} in advance. V_{res} has been charged to V_{cm} in the sampling phase. The increased V_H prevents the leakage immediately. Besides, the injected charge to V_H by M3 does not affect the comparison result. That is because it is so small that the output does not switch. The simulated transient response of V_H is shown in Fig. 2.16. With the aid of M3, V_H rises immediately to prevent the leakage. Similarly, the preventing leakage transistor is adopted by the last comparator. Additionally, the charge leakage in the the 1st or the last comparator can be decreased by compressing V_{ref} or adopting the redundancy of 0.5 bit. The 11-bit 200 Msps subranging SAR ADC with the sharing sampling in Fig. 2.14 is designed in a 65 nm CMOS technology. For the comparison, the conventional subranging SAR ADC in Fig. 2.30 is also designed. Since the flash ADC and CDAC adopt the same clock, the sampling edge's mismatch is not considered in the simulation. Fig. 2.17 contrasts the maximum residue voltage after the coarse conversion phase, which shows the influence of aperture error directly. It is indicated that the aperture error can be reduced effectively with the proposed technique. Furthermore, the benefit of this technique will be more prominent in practice due to the layout parasitic.

2.2.2 Multi-bit Front End

Multi-bit front end can significantly reduce the power dissipation for the high-SNR noise-limited ADC [14–16]. It is to be discussed from the noise, the power dissipation, and the linearity.

Fig. 2.17 Maximum residue versus input frequency (simulated by Specter)



2.2.2.1 Noise

By adopting the multi-bit front end, the noise of the ADC can be optimized because the increased interstage gain of the first stage compresses the noise contribution of the back-end stages. If the resolution increases 1 bit, the interstage gain, G , scales up by a factor of 2 and the feedback factor, β , scales down by a factor of 2.

The noise sampled by the first stage in the tracking phase (referred to the input of the ADC) is

$$\sigma_1 \propto \sqrt{\frac{KT}{\beta G C_S}} \quad (2.11)$$

where C_S is the sampling capacitor. For extra bits, σ_1 maintains the same.

The noise sampled by the second stage is composed of two parts, the noise due to the sampling network in the second stage and the noise due to the amplifier in the first stage. When referred to the input of the ADC, they can be written as [16]

$$\sigma_{2,sw2} \propto \frac{1}{G} \sqrt{\frac{KT}{C_L}} \quad (2.12)$$

$$\sigma_{2,amp1} \propto \frac{1}{G} \sqrt{\frac{KT}{\beta C_L}} \quad (2.13)$$

where C_L is the total load, consisting of the sampling capacitor and the feedback capacitor, C_F , in the first stage, the sampling capacitor, C_{S2} in the second stage, and parasitic capacitors. For each additional bit in the first stage, $\sigma_{2,sw2}$ is reduced by $1/\sqrt{2}$, and $\sigma_{2,amp1}$ is also decreased by $1/\sqrt{2}$.

Therefore, for the fixed sampling capacitance, higher SNR can be achieved. From another point of view, for a given noise budget, the noise reduction enables the

lower power and the smaller sampling capacitance. The smaller sampling capacitance makes the ADC easy to drive, and the power saving will be talked about in detail.

2.2.2.2 Power Consumption

For a fixed noise budget, for each extra bit in the front end, C_L can be reduced to a quarter according to Eq. 2.12, and C_L can be reduced to a half according to Eq. 2.13. Based on the tradeoffs, C_L can be reduced to a value which is between 1/2 and 1/4.

Considering that the close-loop bandwidth of the amplifier is

$$BW = \beta \frac{g_m}{2\pi C_L} \quad (2.14)$$

in the best case, g_m can be reduced by half, maintaining the same bandwidth. And hence the current of the amplifier can be decreased by almost a half. Since amplifier consumes most of the power dissipation, the saved power is considerable.

2.2.2.3 Linearity

On one hand, multi-bit front end reduces the nonlinearity of the first stage. For a N -bit ADC including a M -bit first stage, the DNL error caused by the capacitor mismatch in the first stage can be derived as [17] (normalized to the LSB)

$$DNL = \frac{\gamma 2^{N-0.5M}}{\sqrt{C_{tot}}} \quad (2.15)$$

and

$$\gamma = \frac{\Delta C_i}{\sqrt{C}} \quad (2.16)$$

where ΔC_i is the error of each capacitance, C is the nominal value of each capacitor, and C_{tot} is the total capacitance. Therefore, the DNL error is compressed by $\sqrt{2}$ with every extra bit in the first stage, and it is also reduced by $\sqrt{2}$ with the doubled total capacitance.

On the other hand, the increased interstage gain associated with a high-resolution stage reduces the nonlinearity of the following stages(referred to the input of the ADC).

While the multi-bit front end enables the ADC to optimize the noise, reduce the power, and compress the nonlinearity, one problem is introduced. Since the tolerable input error is $\pm V_{FS}/2^{m+2}$ for the $(m+1)$ -bit individual stage with the redundancy of 1 bit, the tolerable comparator's offset (referred to the input of the flash ADC) is reduced. Therefore, multi-bit front end increases the comparator complexity.

2.2.3 Redundancy Technique

Besides precision analog design techniques and calibration techniques, introducing redundancy is another solution to mitigating the nonideal factors in the ADC. The fundamental difference from the calibration is that the errors are neither measured nor corrected, but simply tolerated and rejected by the redundancy [18]. From another point of view, the idea behind the technique is that the accurate value can be expressed in multiple and equivalent ways with the redundancy. The redundancy-aided conversion dates back to 1964 [19]. And after that, many variations are proposed to cope with the noise, as well as other nonidealities, such as the capacitor mismatch, finite sampling bandwidth, comparator's offset, DAC settling errors, and so on.

2.2.3.1 Redundant Decision Levels

Redundant decision levels is first proposed in [19], where four comparators instead of three ones are adopted to convert 2 bits, absorbing large conversion errors. Since then, the technique is widely adopted in the pipelined ADCs. In the redundancy-aided ADC, the sum of the stage's resolution is larger than the total resolution and then the redundancy is corrected to tolerate the nonlinearity.

The individual stage with 1-bit redundancy is described in [3] to tolerate the comparator's offset by scaling down the interstage gain by 2, as shown in Fig. 2.18. The 2-bit digital outputs are 00, 01, 10, and 11. The input-referred offset as large as $\pm V_{ref}/4$ in the comparator can be tolerated and the correction range of the residue is $\pm V_{ref}/2$. The redundancy is eliminated by a correction logic, which is illustrated by an ADC comprising five pipelined stages, as shown in Fig. 2.19. Since that the interstage gain is reduced by half, the output of the next stage moves left to compensate for that. The disadvantage of this algorithm is that an offset is introduced to the ADC. For example, if the input is $-V_{ref}$, the output is 001111 based on Figs. 2.18 and 2.19 but the expected code is 000000. That offset can be avoided by the individual stage with 0.5-bit redundancy proposed in [20].

The input/output characteristics of a 1.5-bit stage is illustrated in Fig. 2.20. Considering a 6-bit ADC consisting of 4 1.5-bit stages and a 2-bit stage, the input of $-V_{ref}$ is converted into 000000, eliminating the offset. Although the long tail of V_{res} exceeds $\pm V_{ref}/2$, the corrected comparator's offset is still $\pm V_{ref}/4$. Besides, the absence of code 11 avoids the overflow of the corrected output. And removing the decision level of 0 is helpful to improve the linearity of the small swing input's conversion. As to the name of 1.5 bit, it is because $2^n - 2$ (n is the number of digital output bits and here n is 2) comparators are needed in 1.5-bit stage and the resolution is $\log_2(2^n - 1) = 1.5$ bit.

Based on the discussion above, for a $(m+1)$ -bit or $(m+0.5)$ -bit individual stage with the unique error source of the comparator's offset, the offset of $\pm V_{FS}/2^{m+2}$ can be tolerated by the of 1-bit or 0.5-bit redundancy. And V_{FS} is the full scale of the input.

Fig. 2.18 Ideal residue versus input with the redundancy of 1 bit

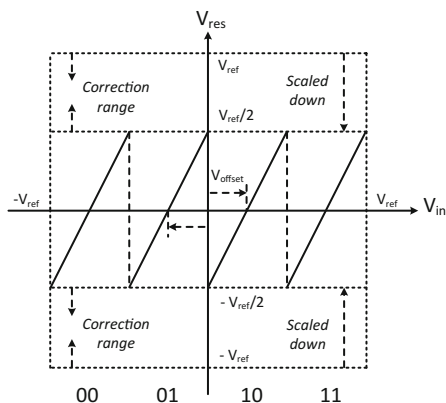


Fig. 2.19 A 6-bit output calculated by the correction algorithm

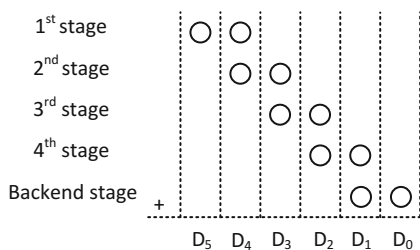
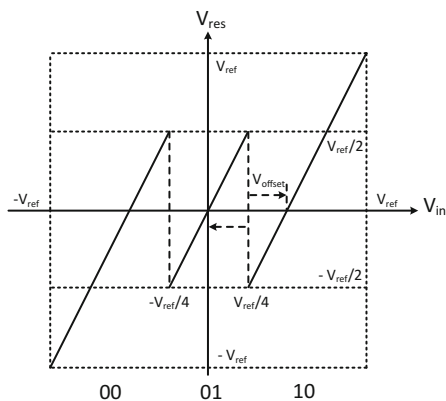


Fig. 2.20 Ideal residue versus input with the redundancy of 0.5 bit



2.2.3.2 Redundant Decision Steps

The technique of redundant decision steps is usually adopted in the SAR ADC to absorb conversion errors via increasing conversion cycles. Therefore, a unique N -bit code can be described by multiple $(N+R)$ -bit codes and R is the number of extra bits. Besides, the cost is the additional hardware of logics for redundant cycles.

For an ideal ADC with the radix of 2, the conversion result can be described by a binary expansion, which is

$$V' = \sum_{k=1}^N D_k 2^{-k} \quad (2.17)$$

where D_k is either 0 or 1 and $V' - V$ is the quantization error. The bit, D_k , is obtained by a binary search algorithm that uses the recursion of

$$V_k = V_{k-1} + S_k 2^{-k} \quad (2.18)$$

where

$$S_k = \begin{cases} 1 & V > V_k \\ -1 & V \leq V_k \end{cases} \quad (2.19)$$

and

$$b_k = (S_k + 1)/2 \quad (2.20)$$

Besides, the modification of Eq. 2.17 is

$$V' = \alpha \sum_{k=1}^N D_k \beta^{-k} \quad (2.21)$$

where $1 < \beta < 2$ and $\alpha = \beta - 1$ is a scale factor to set the full scale to unity. It is called beta-expansion [21].

From another point of view, Eq. 2.18 is realized by the DAC settling and Eq. 2.19 is realized via the comparator's operation. Those operations introduce two types of errors to the SAR ADC, the DAC settling error due to the finite speed of the DAC and the comparison error due to the finite accuracy of the comparator. Both of them can be tolerated by the redundancy.

Redundancy in Designs of Radix = 2

Incomplete settling can be tolerated by the redundancy and the associated calibration. Actually, the digital output of the ADC is obtained by comparing the analog input voltage with the reference voltage. For the traditional conversion in Fig. 2.21a, the equivalent reference voltage is reduced by half in each conversion cycle. For the conversion in Fig. 2.21b, the settling error is compensated for by shifting the equivalent reference voltage and using the extra bit to obtain the same code [22]. The operation in each cycle is illustrated in Fig. 2.21b in detail. The cost of this method is additional compensative capacitors and a error correction logic circuit.

Redundancy in Designs of Radix < 2

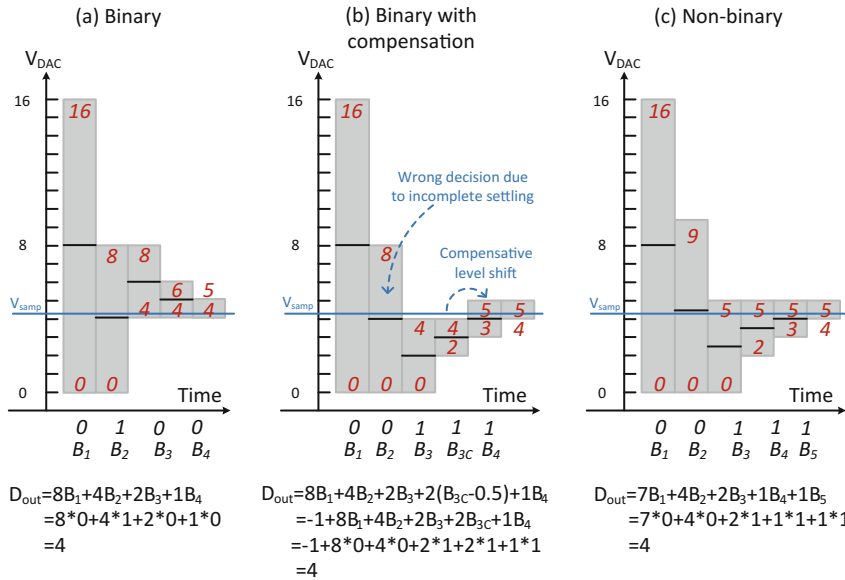


Fig. 2.21 Successive approximations using different methods

The output of a non-binary ADC is described by Eq. 2.21 and an example of the operation is illustrated in Fig. 2.21c, where the equivalent reference voltage is reduced by a factor of smaller than 2 after each DAC switching. Thanks to the redundancy, the settling error with a certain range can be tolerated. However, more conversion cycles and non-binary conversion lead to additional control logic and ROM to store the bit weights [23].

2.3 Improved SAR ADC

A lot of improvements have been achieved after 2000s, because the SAR ADC is digital and friendly to the CMOS technology. To raise the power efficiency, the set-and-down architecture is adopted. In the view of speed improvement, the asynchronous SAR conversion, the multi-bit/cycle SAR ADC, the conversion of redundancy and the time-interleaved SAR ADC are proposed. To effectively increase the resolution, the SAR ADC with a bridge capacitor is commonly used. The techniques are described here.

2.3.1 Power-Efficient Architecture

2.3.1.1 Set-and-Down Architecture

Switching the capacitive array consumes significant power. While the unit capacitance is limited by the KT/C noise, the switching sequence can be modified to improve the power efficiency. The set-and-down architecture is proposed in [24]. It saves time and power, compared with the classical SAR ADC in [25]. Examples of 3 bit switching operation are described in Figs. 2.22 and 2.23. In the sampling phase in

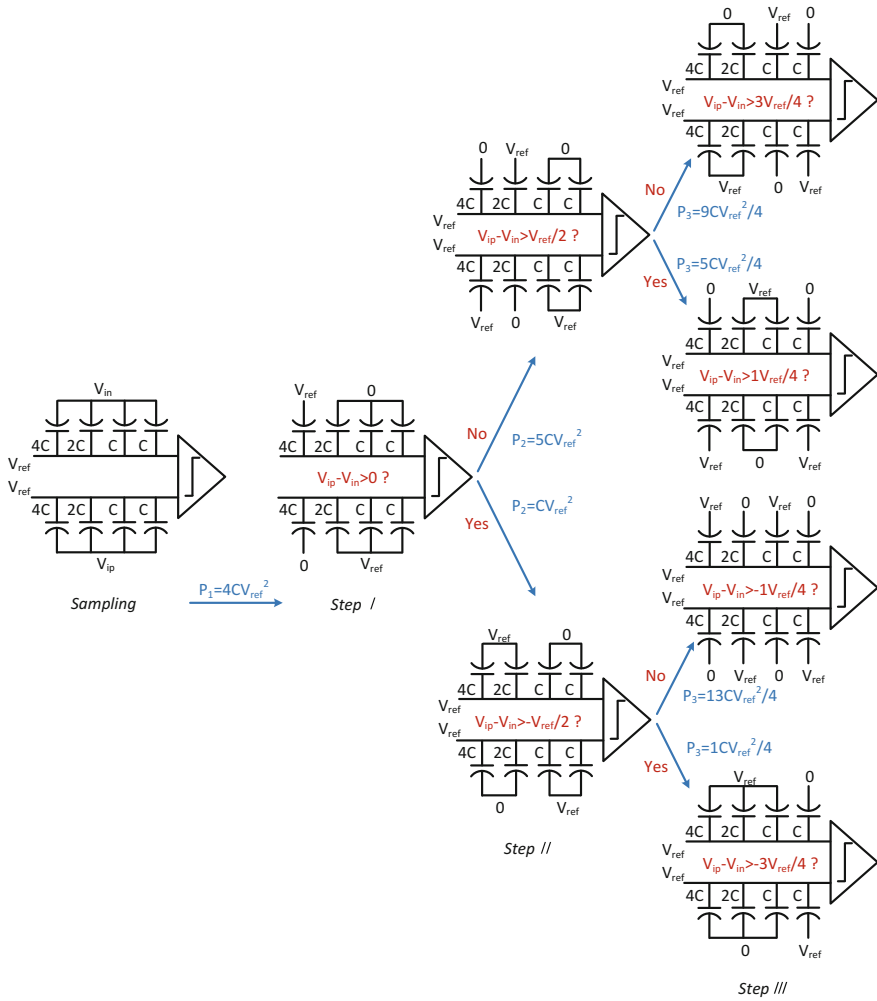


Fig. 2.22 Conventional switching sequence of 3 bit SAR ADC

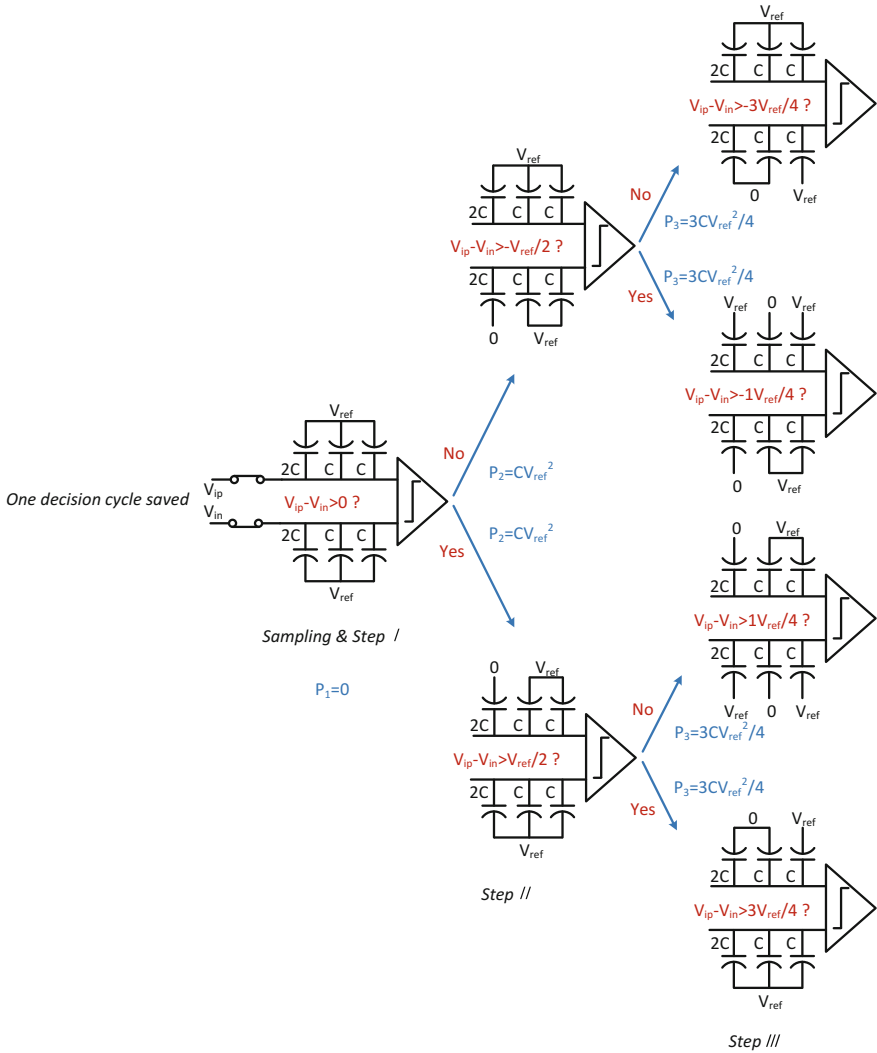


Fig. 2.23 Improved switching sequence of 3 bit SAR ADC in [24]

Fig. 2.23, the input voltage is directly connected to the input node of the comparator and the top plates of the capacitors. The bottom plates of the capacitors are set to V_{ref} at the same time. The comparator tracks the analog input and latched at the end of the sampling phase. Next, the input of the DAC is changed by connecting only one relevant capacitor to 0, resulting in the change of the input of the comparator. Then, a new output of the comparator resets the input of the DAC and starts another conversion cycle. For an n -bit SAR ADC with the conventional switching sequence in Fig. 2.22, the average switching energy can be derived as [25]

$$E_{total, n \text{ bit}} = \sum_{i=1}^n 2^{n+1-2i} (2^i - 1) C V_{ref}^2 \quad (2.22)$$

For an n -bit SAR ADC using the set-and-down switching sequence, the average switching energy can be derived as [24]

$$E_{total, n \text{ bit}} = \sum_{i=1}^{n-1} (2^{n-2-i}) C V_{ref}^2 \quad (2.23)$$

While a 10-bit SAR ADC using the conventional switching sequence consumes $1363.3 C V_{ref}^2$, the one using the set-and-down switching sequence only consumes $255.5 C V_{ref}^2$ and saves 81.3% power dissipation. Besides, one cycle is saved by the set-and-down switching method, which is competitive for the high-resolution and high-speed SAR ADC.

However, the conversion accuracy suffers from the architecture in Fig. 2.23. Sampling switches directly attach to differential inputs of the comparator, and hence the charge in the switches is injected to the comparator at the sampling instant. As a result, inputs of the comparator are disturbed, which may lead to the incorrect outputs and degrade the conversion accuracy. Therefore, the approach requires a comparator with good common-mode rejection.

2.3.1.2 Vcm-Based Architecture

Vcm-based switching approach is proposed in [26] to reduce the power further and avoid large common-mode jumps. Compared with the set-and-down switching, before bit decisions are obtained, bottoms of capacitors are connected to V_{cm} instead of V_{ref} or 0. However, the on-resistance in the switch connected to V_{cm} , like SW_3 in Fig. 2.24a, increases, because that V_{gs} of the switch transistors is reduced (V_{cm} is normally half of V_{ref}). As a result, the increased RC constant slows down the DAC settling. To respond to that, the split capacitor Vcm-based architecture is proposed. A capacitor from the DAC capacitor array is described in Fig. 2.24 to illustrate the modification. In the Vcm-based architecture, the capacitor bottom may be connected to 0, V_{ref} , or V_{cm} via switch SW_1 , SW_2 , or SW_3 in Fig. 2.24a. In the split Vcm-based architecture, the capacitor, SW_1 , and SW_2 split, and SW_3 is removed in Fig. 2.24b. And the operation of shorting $2C$ and V_{cm} is replaced by shorting C_1 and 0 and shorting C_2 and V_{ref} , as shown in Fig. 2.24c. Compared with [26], the modification not only increases the DAC settling, but also simplifies the SAR logic. But, for the minimum capacitor (which is normally the capacitor unit) in the capacitor array, the approach can not be adopted.

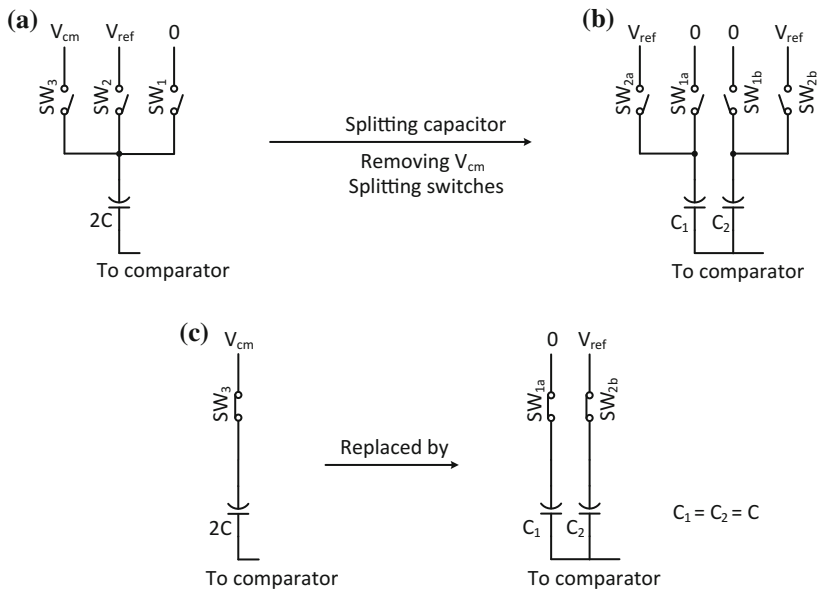


Fig. 2.24 A capacitor in **a** V_{cm}-based architecture and **b** split capacitor V_{cm}-based architecture, and **c** the operation of shorting the capacitor bottom and V_{cm}

2.3.2 High-Speed Architecture

2.3.2.1 Asynchronous Clocking Architecture

An asynchronous SAR ADC is proposed in [27] to exceed the power and speed limitations of a synchronous SAR ADC. For a synchronous N -bit SAR ADC with the conversion rate of F_S , an internal clock running at least $(N + 1)F_S$ is required, which is described in Fig. 2.25a. To implement a high-resolution and high-speed ADC, the clock generator and clock distribution network would consume more power than the ADC core itself, which is a significant overhead. Besides, every clock has to tolerate the worst conversion time and consider the margin for the clock jitter, which slows down the speed of the ADC. For an asynchronous SAR ADC, the high-speed internal clock is removed, shown in Fig. 2.25b. The comparison is triggered from the MSB to LSB like dominos. Once the current comparison is finished, a signal is generated to trigger the next comparison. The asynchronous clocking is commonly adopted by high-performance SAR ADC.

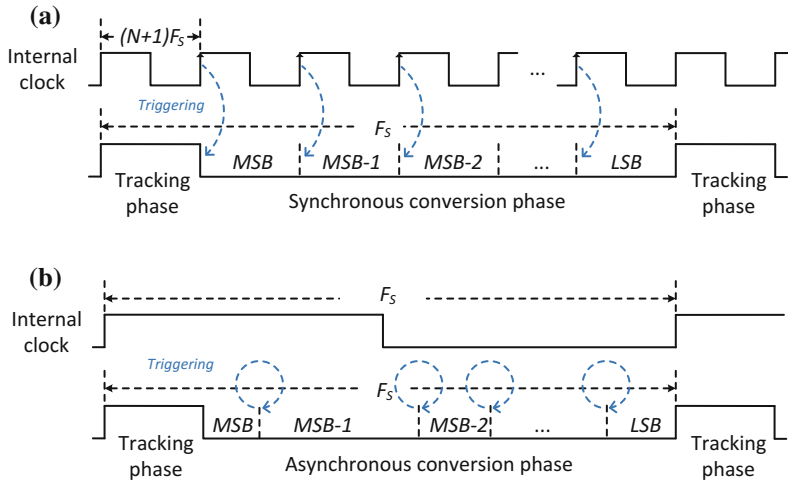


Fig. 2.25 Conversion of **a** synchronous and **b** asynchronous SAR ADC

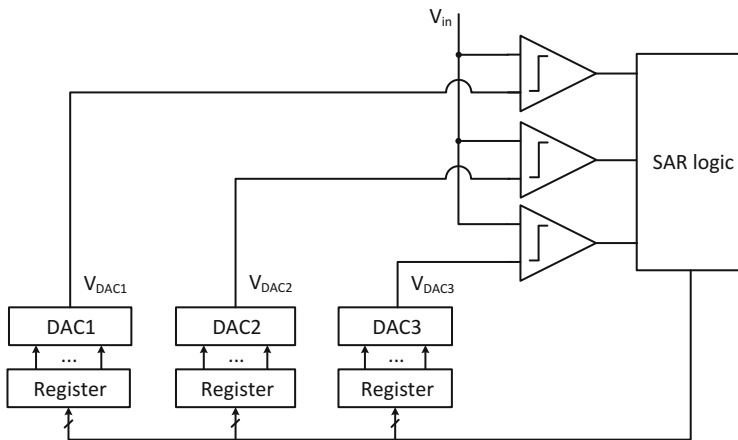


Fig. 2.26 SAR ADC with 2 bits per cycle

2.3.2.2 Multi-Bit-Cycle Architecture

To combine the high speed of a flash ADC and the low-power dissipation of a SAR ADC, converting more than one bit per cycle is proposed, like 2 bits per cycle in [6, 28, 29] and 3 bits per cycle in [30]. A simple 2-bit-cycle SAR ADC is illustrated in Fig. 2.26. In each cycle, 2 bits are provided to speed up the conversion rate. However, 3 comparators, 3 DACs and additional logics are required. The considerable growth in area, complexity and input capacitance (for capacitive DAC) lead to large hardware overhead, especially for the case of more than 2 bits per cycle. Besides, the random

offsets of the comparators limit the linearity of the conversion. To solve these issues, interpolation is adopted in [30] to decrease the number of comparators and DAC capacitors, and the offset calibration is used in [28–30] to improve the accuracy of the ADC.

2.3.2.3 Others

Interleaving channels of SAR ADC is a direct way to proportionally increase the speed. The generic issues of the time-interleaved architecture (to be discussed in Sects. 2.5 and 6.2.4) apply here as well, including increased area and input capacitance and interchannel mismatches. Besides, the channels couple with one other through the shared reference voltage, limiting the accuracy of the ADC [6].

2.3.3 Low-Area Architecture

To respond to the problem that the number of the unit capacitors exponentially increases with the raising resolutions, the capacitor array with a bridge capacitor is commonly adopted [6, 31]. A $(M + L + 1)$ -bit SAR ADC with a bridge capacitor, C_b , is described in Fig. 2.27a. There are M binary weighted capacitors and a C_{d1} in the MSB segment, and L binary weighted capacitors and a C_{d2} in the LSB segment. The contribution of the capacitors in LSB segment to the DAC output is scaled down due to C_b . Therefore, the unit capacitor in the LSB segment is scaled up, decreasing the capacitor mismatch and improving the linearity of the ADC. In order to calculate the capacitance, C_b , the response to bottom plates of its adjacent capacitors, $2^{L-1}C_u$ and kC_u , is illustrated in Fig. 2.27b. C_{Mt} and C_{Lt} are the total capacitance of the MSB segment and the LSB segment, respectively. They are given by

$$C_{Mt} = (2^M - 1)kC_u + C_{d1} \quad (2.24)$$

$$C_{Lt} = (2^L - 1)C_u + C_{d2} \quad (2.25)$$

At the DAC output, the step response of the two capacitors should satisfy

$$\Delta V_{o1} = 2\Delta V_{o2} \quad (2.26)$$

where

$$\Delta V_{o1} = \frac{kC_u(C_b + C_{Lt})}{X} \Delta V \quad (2.27)$$

$$\Delta V_{o2} = \frac{2^{L-1}C_bC_u}{X} \Delta V \quad (2.28)$$

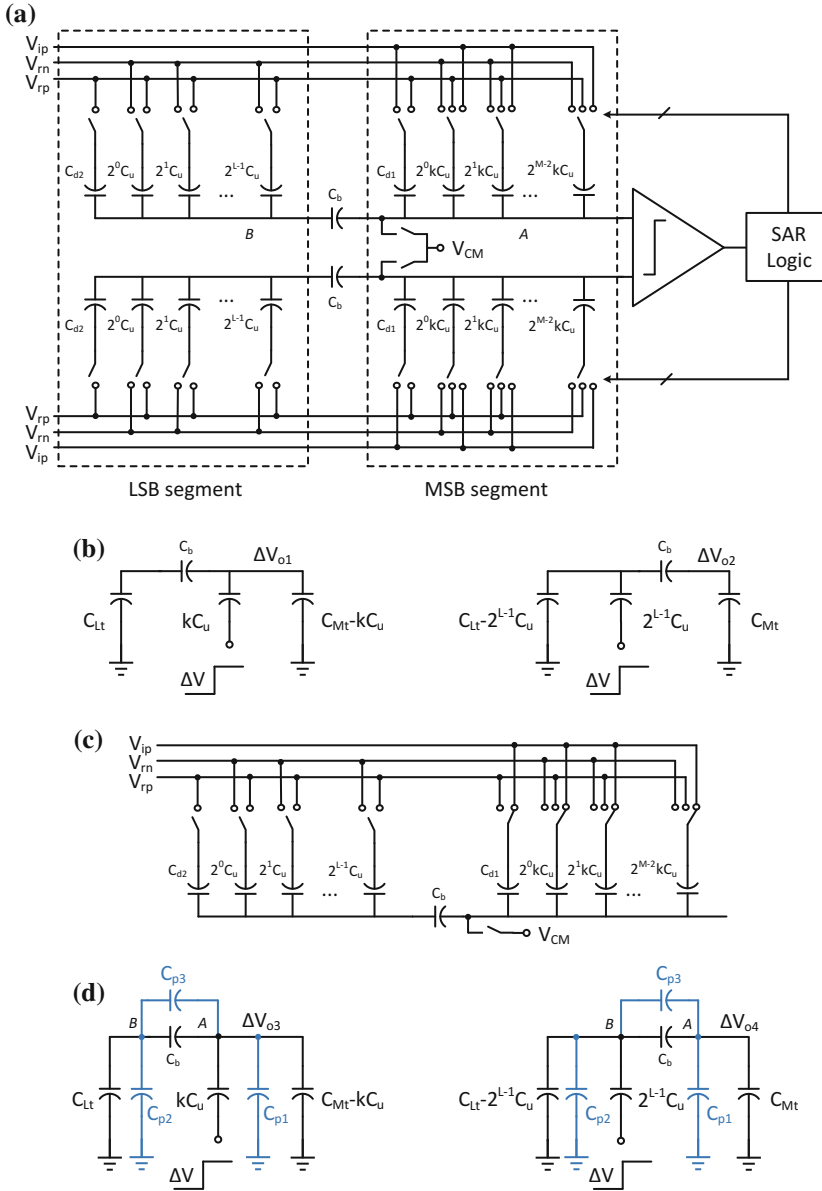


Fig. 2.27 **a** SAR ADC adopting a bridge capacitor, **b** the response to a bottom plate swing of ΔV , **c** operations in the sampling phase, and **d** the response to a bottom-plate swing of ΔV (single end is shown for simplicity in **b**, **c** and **d**)

And,

$$X = C_{Mt}(C_b + C_{Lt}) + C_b C_{Lt} \quad (2.29)$$

Therefore, the bridge capacitor can be derived as

$$\frac{C_b}{C_u} = \frac{k}{2^L - k} \frac{C_{Lt}}{C_u} = \frac{k}{2^L - k} \frac{(2^L - 1)C_u + C_{d2}}{C_u} \quad (2.30)$$

And,

$$\frac{C_{d2}}{C_u} \geq 0 \quad (2.31)$$

In Eqs. 2.30 and 2.31, C_b/C_u is the positive integer and C_{d2}/C_u is the nonnegative integer. For a given segmented capacitive DAC, M , L and k are fixed and C_b only depends on C_{d2} . C_b is usually calculated according to the minimum C_{d2} . Several examples of segmented DACs and the bridge capacitors are described in Table 2.1.

As to C_{d1} , it satisfies

$$C_{d1} = kC_u \quad (2.32)$$

Because C_{d1} samples the input, capacitors in the LSB segment do not sample the input voltage, as shown in Fig. 2.27c. Input capacitance is reduced and there is no gain error caused. Capacitor C_{d1} and its parasitics have no contribution to the gain error, which only depends on the ratio of total sampling capacitors to total DAC capacitors.

The bridge capacitor architecture suffers from the parasitic capacitors, including the grounded ones at A and B and the coupling one between A and B , which cause errors at the DAC output. To analyze the errors, the step response to the adjacent capacitors of C_b , $2^{L-1}C_u$ and kC_u , is described in Fig. 2.27d. ΔV_{o3} and ΔV_{o4} can be derived as

$$\Delta V_{o3} = \frac{kC_u(C_b + C_{p3} + C_{Lt} + C_{p2})}{Y} \Delta V \quad (2.33)$$

$$\Delta V_{o4} = \frac{2^{L-1}(C_b + C_{p3}C_u)}{Y} \Delta V \quad (2.34)$$

where

Table 2.1 Design of bridge capacitors

DACs	Given parameters	C_b (minimum C_{d2} adopted)
DAC1	$M = 4, L = 4, k = 1$	$C_b = C_u$ ($C_{d2} = 0$)
DAC2	$M = 2, L = 6, k = 2^4$	$C_b = 21C_u$ ($C_{d2} = 0$)
DAC2	$M = 4, L = 6, k = 2^2$	$C_b = 5C_u$ ($C_{d2} = 12C_u$)
DAC2	$M = 4, L = 8, k = 2^4$	$C_b = 17C_u$ ($C_{d2} = 0$)

$$Y = (C_{Mt} + C_{p1})(C_b + C_{p3} + C_{Lt} + C_{p2}) + (C_b + C_{p3})(C_{Lt} + C_{p2}) \quad (2.35)$$

Ideally, the binary bit weights require

$$\Delta V_{o3} = 2\Delta V_{o4} \quad (2.36)$$

The nonideal bit weights caused by the bridge capacitor's parasitics can be described as

$$\epsilon = \frac{\Delta V_{o3} - 2\Delta V_{o4}}{2\Delta V_{o4}} \approx \frac{C_{p2}}{C_{Lt}} - \frac{C_{p3}}{C_b} \quad (2.37)$$

Therefore, the bit weights suffer from C_{p2} and C_{p3} , resulting in the nonlinearity of the ADC. C_{p1} only leads to the gain error at the DAC output.

2.3.4 Summing up

Techniques discussed above and their cost are as follows.

To save the power dissipation, different switching approaches are proposed. While set-and-down architecture with top-plate sampling saves the power and time, it requires a comparator with good common-mode rejection, since large common-mode jumps occur during charge redistribution. Vcm-based architecture saves the power further and reduces common-mode jumps, but it suffers from the slow DAC settling. To respond to that, split capacitor Vcm-based switching is proposed. However, for the minimum capacitor (which is normally the capacitor unit) in the capacitor array, the approach can not be adopted.

The asynchronous clocking and multi-bit-cycle architecture are commonly adopted by high-speed single-channel SAR ADC. However, for the case of more than 2 bits per cycle, the considerable growth in area, complexity and input capacitance (for capacitive DAC) lead to large hardware overhead. Besides, the random offsets of the comparators limit the linearity of the conversion. For the time-interleaved SAR ADC, the cost of the increased speed includes increased area and input capacitance, interchannel mismatches, and so on.

To respond to the problem that the number of the unit capacitors exponentially increases with the raising resolutions, the capacitor array with a bridge capacitor is commonly adopted. Parasitic capacitors of the bridge capacitor degrade the linearity.

2.4 Hybrid ADC

As shown in Fig. 2.28, the hybrid ADC combines the high speed of the flash ADC, the low power of the SAR ADC, and the effective compromise of high speed and high resolution in the pipelined ADC, improving the performance and saving the power

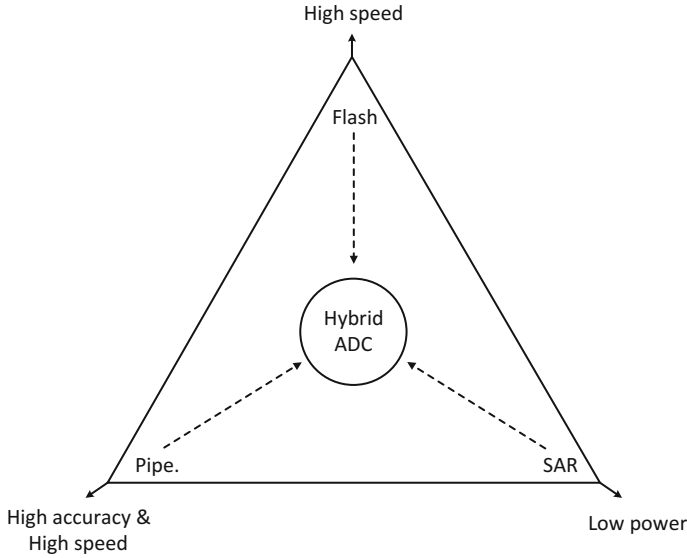


Fig. 2.28 The hybrid ADC based on traditional architectures

dissipation. In this section, we discuss the subranging SAR ADC and the pipelined SAR ADC.

2.4.1 Subranging SAR ADC

The subranging SAR has the potential to realize the fast and power-efficient conversion. A common subranging architecture is depicted in Fig. 2.29. It consists of a coarse ADC, a DAC, a fine ADC and a correction block, operating the sampling, the coarse, and the fine conversion in one period. For the subranging SAR ADC, the coarse conversion is accomplished by the flash ADC and the fine conversion is done by the SAR ADC. The first N_1 MSBs are output in parallel, speeding up the conversion. The comparators' accuracy of the flash ADC is relaxed due to the redundancy. Furthermore, the power-hungry opamp is removed in the architecture, reducing the power dissipation.

Here is an 11-bit subranging SAR as an example, as shown in Fig. 2.30. It includes a 3.5-bit flash ADC for the coarse conversion, followed by an 8-bit SAR ADC for the fine conversion. When ϕ_1 is high, the capacitor array and the flash ADC track the input and sample it at the falling edge of ϕ_{1a} . When ϕ_2 is high, the flash ADC operates the coarse comparison and outputs the MSBs, Q_i , which control the capacitors C_i during the following fine conversion phase. From a point of view of the capacitive DAC, the 3.5-bit MSB settleings are overlapped, and hence there is only one critical

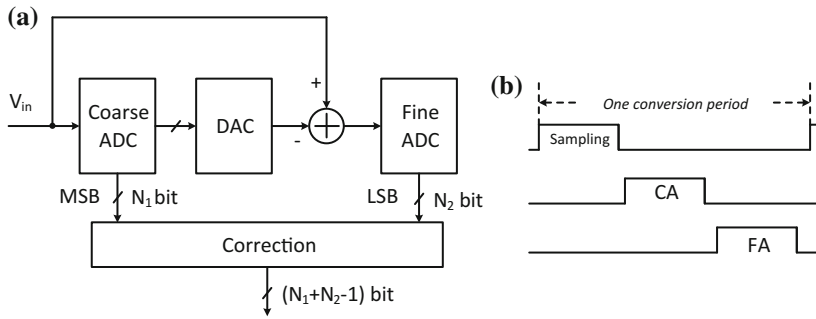


Fig. 2.29 **a** The concept of a sub-ranging ADC and **b** the timing

DAC settling. The 8-bit LSB settlings are based on the SAR principle. As a two-stage architecture, its input/output characteristics of the coarse stage is similar to that of a individual stage in a pipelined ADC and the slope is 1 due to the absence of the residue amplifier, as is show in Fig. 2.30c.

2.4.2 Pipelined SAR ADC

The pipelined SAR ADC adopts the SAR architecture as the sub-ADC in the pipelined stages, avoiding requirements of high-accuracy comparators and the extra front-end sample-and-hold. It combines the high resolution of the pipelined architecture and the low-power dissipation of the SAR ADC.

The topology of a pipelined SAR ADC is shown in Fig. 2.31. The ADC is composed of two stages, the SAR-assisted first-stage and the second-stage SAR. In the first stage, both the sampling networks of the sub-ADC and the MDAC are merged in the capacitive DAC. Besides, the DAC, the comparator and the SAR logic generate N_1 -bit code and the residue voltage to be amplified. The interstage gain of 2^{M1} is provided by the closed-loop opamp. The second stage is implemented by a N_2 -bit SAR ADC.

2.5 Time-Interleaved ADC

The time-interleaved ADC speeds up the conversion rate using n parallel identical ADCs, which operate in time multiplexing way. As is shown in Fig. 2.32, although every ADC converts data at the low rate of F_s/n (here n is 4 as an example), the time-interleaved ADC achieves the high speed of F_s . Besides, time-interleaved architecture can be adopted by any ADCs, such as the pipelined ADC, the SAR ADC, the flash ADC, and so on.

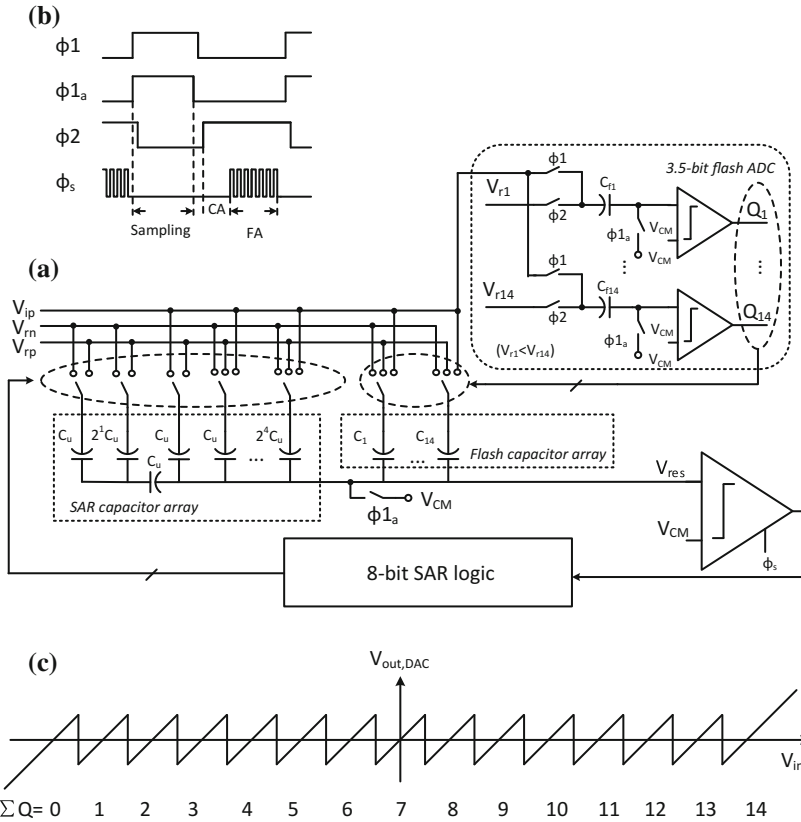


Fig. 2.30 a An 11-bit subranging SAR ADC, b the timing, and c the input/output characteristics of the coarse stage

2.6 Summing up

In this chapter, different ADC architectures are discussed. First, three traditional ADCs are presented. Although lots of Nyquist-rate ADCs are proposed to resolve resolutions at different speeds throughout the years, there are three types of architectures most widely used and they are the pipelined ADC, the SAR ADC, and the flash ADC. Second, the improvement of them are analyzed, because they all have the potential to achieve the high performance and the high-power efficiency, via the adjustment in the architecture level or with the aid of useful techniques. Then, we talk about the hybrid ADC, which combines the high speed of the flash ADC, the low power of the SAR ADC, and the effective compromise of high speed and high resolution in the pipelined ADC. In addition, the time-interleaved technique is discussed. It effectively assists the low-power single-channel ADC in improving the conversion rate.

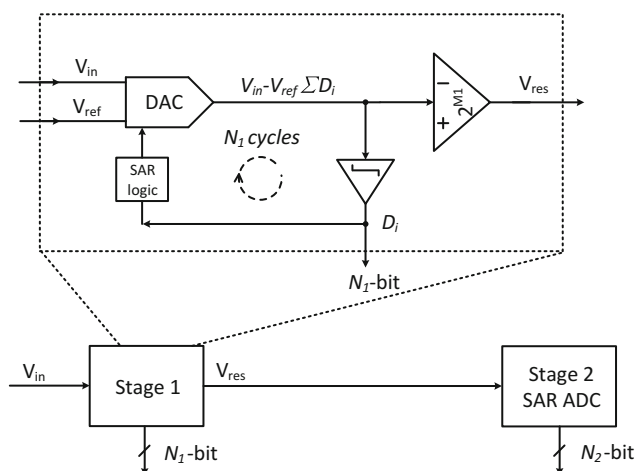


Fig. 2.31 The pipelined SAR ADC

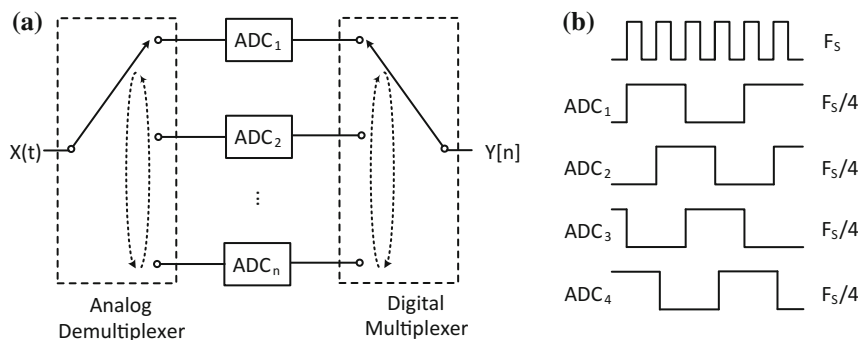


Fig. 2.32 The **a** time-interleaved ADC and **b** timing

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