

Preface

Low-power (LP) design, power-aware (PA) verification, and Unified Power Format (UPF) or IEEE-1801 power standards are no longer special features. These technologies and methodologies are now part of standard design, verification, and implementation flows (DVIFs). Almost every chip design today incorporates some kind of low-power technique through power management on chip—by dividing the design into different voltage areas and controlling the voltages, through UPF and testbench. Then, the PA dynamic and PA static verification or their combination comes into the play.

The entire LP design and PA verification process involves thousands of techniques, tools, and methodologies, employed from the register transfer level (RTL) of design abstraction down to the synthesis or place-and-route levels of physical design. These techniques, tools, and methodologies are evolving everyday through the progression of design-verification complexity and more intelligent ways of handling that complexity by engineers, researchers, and corporate engineering policy makers.

However, the industry is missing a complete knowledge base to fully comprehend LP design and PA verification techniques and methodologies. And deploy them all together in a real design verification and implementation projects. This book, “The Concepts and Fundamentals of Power Aware Verification”, is the first approach to establishing a comprehensive PA knowledge base.

Writing an engineering reference book is never an easy task, especially when the perspective is wide, encompassing academic thought and the pragmatic objective of making a reference engineering handbook. The entire effort seeks to bring the complex LP design and PA verification process to a complete and one-stop platform – one where engineers will find real examples and results, corporate engineering policy makers will discover ideas for appropriate methodologies to adopt for their next design-verification project, researchers will find topics for new and innovative ideas, and EDA verification experts will be able to enhance and fine tune their tools for the best industry practices.

This book is written in a ground up manner with the objective to appeal to a wide range of readers – from beginners to experts in the low power design and power

aware verification world. However, it is highly recommended that the reader have a solid grasp of HDL (Verilog, SystemVerilog, and VHDL etc.) fundamentals before jumping into this book. This is because UPF directly inherit ports, nets, elements, instances, modules, interfaces, boundaries, hierarchical constructs, scopes, and more from HDL. And obviously, the PA verification artifacts – tools and techniques are founded on the combination of UPF and HDL constructs.

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