

Chapter 2

Three-Dimensional Macroporous Nanoelectronics Network

2.1 Introduction

Seamlessly merging functional electronic circuits as embedded systems in a minimally-invasive manner with host materials in 3D could serve as a pathway for creating “very smart” systems because those embedded systems would transform conventional inactive materials into active systems. The embedded electronic sensor circuitry could monitor chemical and physical changes throughout a host material, thus providing detailed information about the host material’s response to external environments as well as desired feedback to the host and external environment [1, 2]. To achieve this goal, the addressable electronics should be firstly macroporous, not planar, to enable 3D interpenetrations with the host materials. Second, to minimize invasiveness of the macroporous electronic network it must have (1) microscale to nanoscale feature sizes, (2) a small filling fraction with respect to the host (e.g., $\leq 1\%$), (3) comparable or softer mechanical properties than the host, and (4) an inert chemical response within the host material.

The constraints outlined above require the utilization of 3D nanoelectronic networks that are macroporous and have active elements (nanodevices). Previously, two basic methods have been used to fabricate 3D integrated electronic circuits. The first involves bonding 2D substrates, each containing 2D devices/circuits network, together in a 3D stack [3, 4]. The second exploits bottom-up assembly of nanoelectronic elements in a layer-by-layer manner [5, 6]. However, both methods yield solid or nonporous 3D structures that only allow the top-most layer of electronic elements to be interfaced directly with a second material/object and thus precluding integration of all of the electronic elements seamlessly with a host material in 3D. Here, we introduce a general mechanics-driven strategy for patterning macroporous nanoelectronic networks that contains regular arrays of addressable nanowire nanoelectronic elements in 3D structure.

2.2 Experimental

2.2.1 3D Macroporous Nanowire Nanoelectronic Network Fabrication

Uniform 30 nm p-type single-crystalline silicon nanowires were synthesized as report [7, 8]. The 3D macroporous nanowire nanoelectronic networks were initially fabricated on the oxide or nitride surfaces of silicon substrates prior to relief from the substrate. A mechanics-driven fabrication process was (Fig. 2.1) used in the fabrication of the 3D macroporous nanowire nanoelectronic networks that were reported in ref 2 and 7 briefly: (1) lithography and thermal deposition were used to pattern nickel metal relief layer for the 2D free-standing macroporous nanowire

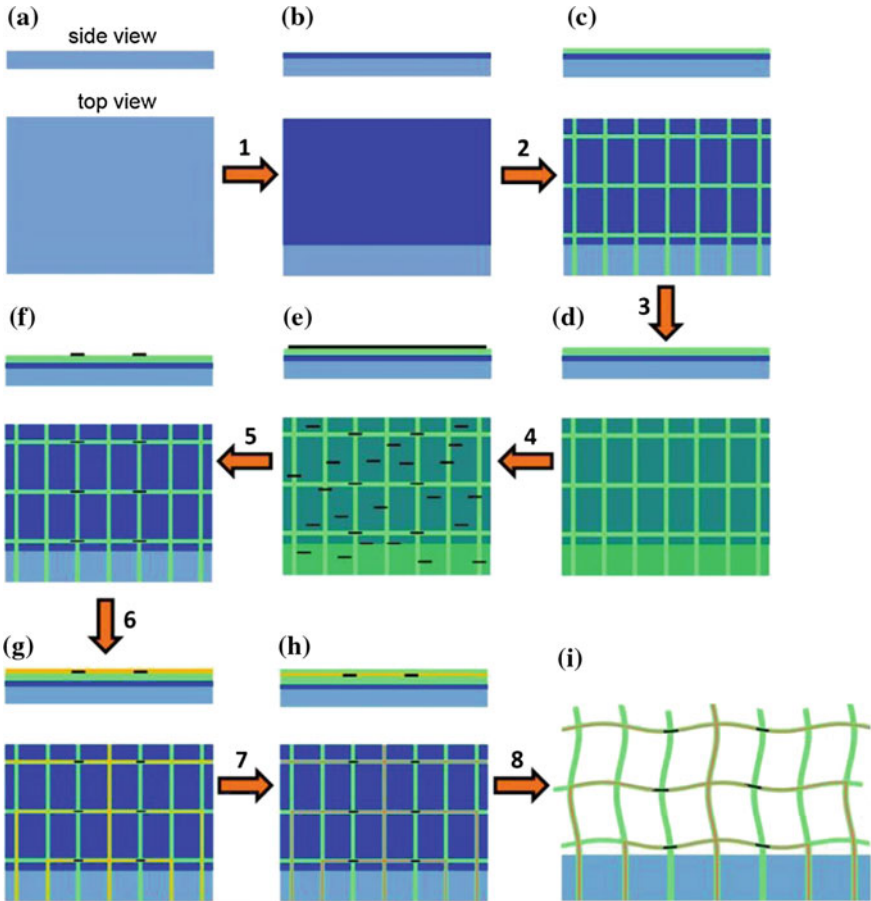


Fig. 2.1 Schematic of macroporous nanoelectronics fabrication. Components include silicon wafer (cyan), nickel sacrificial layer (blue), polymer (green), metal interconnects (gold) and silicon nanowires (black)

nanoelectronic networks. (2) A 300–500 nm layer of SU-8 photoresist was deposited over the entire chip, then (3) the synthesized nanowires were directly printed from growth wafer over the SU-8 layer by the contact printing methods reported previously [6]. (4) Lithography (photolithography or electron beam lithography) was used to define regular patterns on the SU-8. Those nanowires on the non-exposed area will be removed by washing away in SU-8 developer and isopropanol solution for leaving those selected nanowires on the regular pattern SU-8 structure. (5) A second 300–500 nm layer of SU-8 photoresist was deposited over the entire chip. Then lithography was used to pattern the bottom SU-8 layer for passivating and supporting the whole device structure. (6) Lithography and thermal deposition were used to define and deposit the metal contact to address each nanowire device and form interconnections to the input/output pads for the array. (7) A third 300–500 nm layer of SU-8 photoresist was deposited over the entire chip. Then lithography was used to pattern the top SU-8 layer for passivating the whole device structure. (8) The 2D macroporous nanowire nanoelectronic networks were released from the substrate by etching of the nickel layer. (9) The 3D macroporous nanowire nanoelectronic networks were dried by a critical point dryer and stored in the dry state prior to use.

2.2.2 Three-Layer Interconnect Ribbon for Mechanical Simulation

SU-8/metal/SU-8 ribbons with 100 μm long and 5 μm wide segments over the Ni-layer and wider segments directly on substrate were defined by EBL using the same approach described above. A schematic and an optical image of the resulting sample element are shown in Fig. 2.2a, b, respectively. An atomic force microscope was used to measure force versus displacement curves for the ribbon (Fig. 2.2c). The spring constant of the AFM cantilever/tip assemblies used in the measurements were calibrated by measuring the thermal vibration spectrum [9].

The self-organization of the macroporous structure due to residual stress was simulated by the commercial finite element software ABAQUS. Ribbons were modeled as beam elements. The equivalent bending moment on SU-8/metal ribbons was calculated using the residual stress measured by MET-1 FLX-2320-S thin film stress measurement system, which were 1.35 and 0.12 Gpa for Cr (50 nm) and Pd (75 nm), respectively.

2.2.3 Characterization and Measurement of Macroporous Nanoelectronics

Scanning electron microscopy (SEM), Bright-field and dark-field optical microscopy, and confocal fluorescence microscopy were used to characterize the

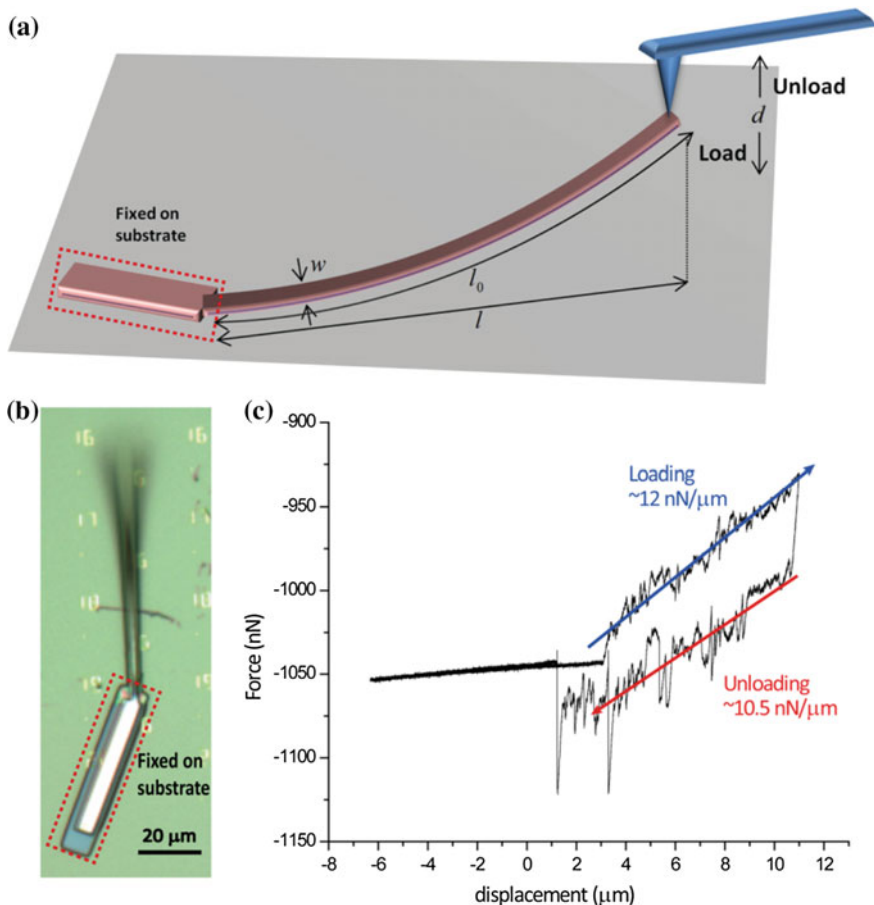


Fig. 2.2 Bending stiffness measurements. **a** Schematic illustrating the measurement of the bending stiffness of a representative SU-8/metal/SU-8 ribbon in the macroporous nanoelectronic networks. The tip of the AFM is placed at the free end of the ribbon, and then translated vertically downward (loading) and upward (unloading) to yield the force-displacement curves. In the scheme, w : the width of the ribbon, l_0 : the length of the ribbon, l : the projected length of the ribbon and d : the displacement of the AFM tip. **b** Optical micrograph of the fabricated structural element, where the substrate fixed portion is highlighted by the red dashed rectangle and the free beam is in the upper portion of the image with a width of 5 μm and a length of 100 μm . **c** A typical force—displacement curve with F/d for loading and unloading of 12 and 10.5 $\text{nN}/\mu\text{m}$, respectively

macroporous nanoelectronic networks. *ImageJ* (ver. 1.45i) was used for 3D reconstruction and analysis of the confocal and epi-fluorescence images.

Silicon nanowire device in the 3D macroporous nanoelectronic network recording was carried out with a 100 mV DC source voltage. The current was amplified by a home-built multi-channel current/voltage preamplifier with a typical gain of 10^6 A/V . The amplified signals were filtered through a home-built conditioner with band-pass of 0–3 kHz, digitized at a sampling rate of 20 kHz and

recorded using Clampex 10 software. The nanowire FET conductance and transconductance (sensitivity) were measured and calculated in $1 \times \text{PBS}$ as described previously [10].

2.3 Results and Discussion

2.3.1 3D Macroporous Nanoelectronic Network

We combine both “bottom-up” and mechanics-driven approaches to realize 3D macroporous nanoelectronic networks (Fig. 2.3). In this approach, we utilize functional nanowires as nanoelectronic elements (Fig. 2.3a). The variations of nanowires in composition, morphology and doping encoded during synthesis [11–19] define diverse functionality including devices for logic and memory [20, 21], sensors [18, 23], light-emitting diodes [17], and energy production and storage [24, 25]. Through a combination of nanowire assembly and conventional 2D lithography carried out on a sacrificial substrate (see below), we can first realize 2D mesh nanoelectronic networks with multiple functions. Then, we remove the sacrificial layer to yield a free-standing and flexible 2D mesh nanoelectronic network as precursor for 3D macroporous electronics (Fig. 2.3b). Third, we implemented internal stress into the metal interconnects of 2D mesh electronic network during fabrication. This stress, due to its designed distribution, creates forces to organize the freestanding 2D mesh nanoelectronic precursor into a regular 3D macroporous structure.

The key steps for this “bottom-up” fabrication process are outlined in Fig. 2.4. First, nanowires were uniaxially-aligned by contact printing [14] on the surface of a layer of SU-8 negative resist (Fig. 2.4a, I). Second, the SU-8 layer with aligned nanowires was patterned to define a periodic array by lithography, and the excess nanowires on unexposed regions of the SU-8 were removed when the pattern was developed (Fig. 2.4a, II). The nanowire density and feature size in periodic arrays

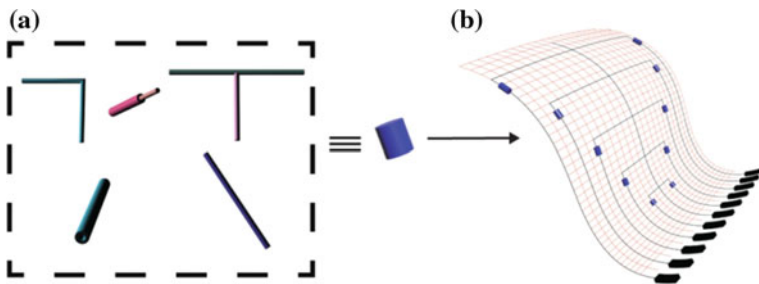
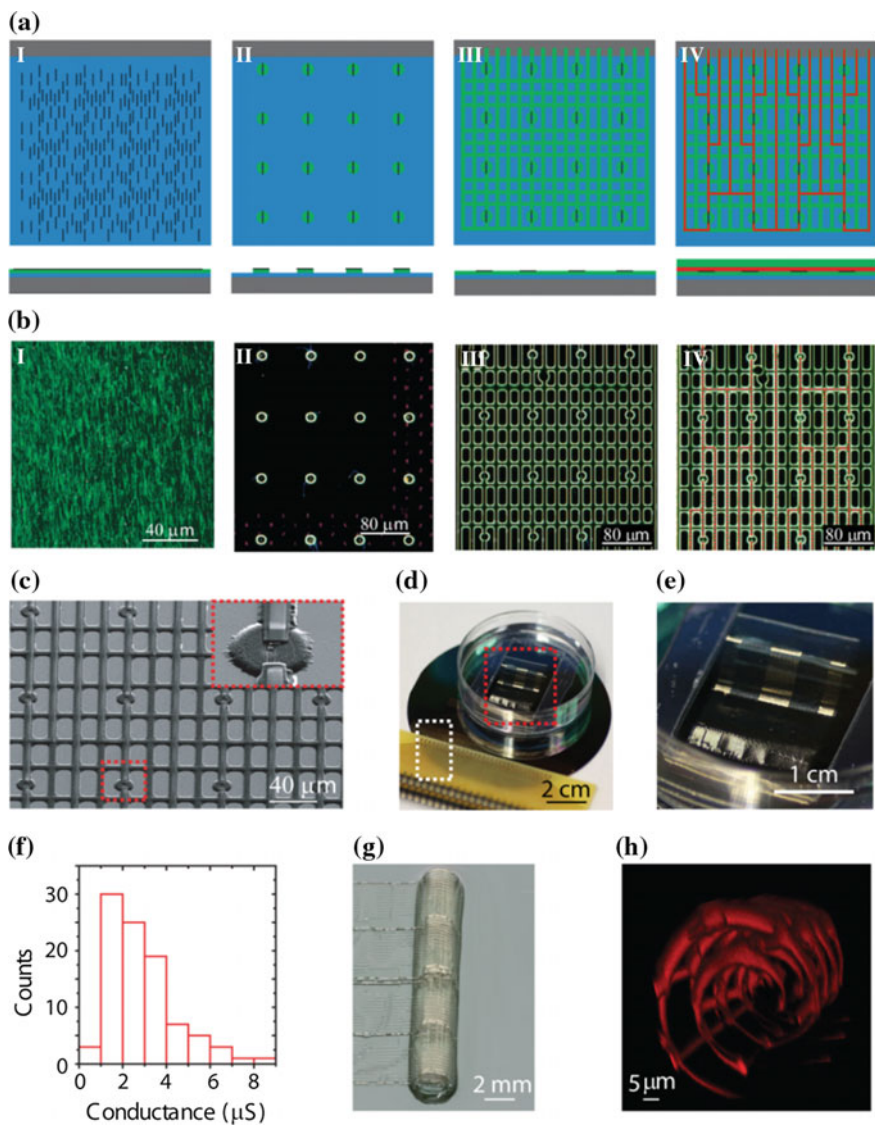


Fig. 2.3 Strategy for preparing 3D macroporous nanoelectronic networks. **a** Different nanowire nanoelectronic elements such as kinked nanowire, nanotube, core-shell, straight and branched nanowire. **b** Freestanding 2D macroporous nanowire nanoelectronic “precursor”. Blue: nanoelectronic element, orange: passivation polymer, black: metal contact and input/output (I/O)



◀**Fig. 2.4** Organized 2D and 3D macroporous nanoelectronic networks. **a** Schematics of nanowire registration by contact printing and SU-8 patterning. Gray: Silicon wafer, blue: Ni sacrificial layer, black ribbon: nanowire, green: SU-8, red: metal contact. (Top) shows top view and (bottom) shows side view. **(I)** Contact printing nanowire on SU-8. **(II)** Regular SU-8 structure was patterned by lithography to immobilize nanowires. Extra nanowires were washed away during the develop process of SU-8. **(III)** Regular bottom SU-8 structure was patterned by spin-coating and lithography. **(IV)** Regular metal contact was patterned by lithography and thermal evaporation, followed by top SU-8 passivation. **b** Dark field optical images corresponding to each step of schematics in **(a)**. **c** SEM image of a 2D macroporous nanoelectronic network prior to release from the substrate. Inset, corresponds to zoom-in of the region enclosed by the red dashed box containing a single nanowire device. **d** Photograph of wire-bonded free-standing 2D macroporous nanoelectronic network in petri-dish chamber for aqueous solution measurements. The red dashed box highlights the free-standing portion of the nanoelectronic network and the white-dashed box encloses the wire-bonded interface between the input/output (I/O) and PCB connector board. **e** Zoom-in of the region enclosed by the red-dashed box in **(d)**. **f** Histogram nanowire device conductance in the free-standing 2D macroporous nanoelectronic networks. **g** Photograph of a manually scrolled-up 3D macroporous nanoelectronic network. **h** 3D reconstructed confocal fluorescence images of a representative self-organized 3D macroporous nanoelectronic network viewed along the x-axis

were chosen such that each element contained on average 1–2 nanowires. Third, a second SU-8 layer was deposited and patterned in a mesh structure by lithography (Fig. 2.4a, III). This SU-8 mesh serves to interconnect the nanowire/SU-8 periodic features and provides an adjustable support structure to tune the mechanical properties. Fourth, metal interconnects were defined by standard lithography and metal deposition on top of the appropriate regions of the SU-8 mesh, such that the end of nanowires were contacted and the nanowire elements were independently addressable (Fig. 2.4a, IV). Last, a third SU-8 layer was lithographically patterned to cover and passivate the metal interconnects.

Dark-field optical microscopy images obtained from a typical nanoelectronic network fabrication corresponding to the steps described above (Fig. 2.4b) highlight several important features. First, the images recorded after contact printing (Fig. 2.4b, I) confirm that nanowires are well-aligned over areas where nanowire devices are fabricated. We can achieve good nanowire alignment on length scales up to at least several centimeters as reported elsewhere [6, 7, 14]. Second, a representative dark-field image of the patterned periodic nanowire regions (Fig. 2.4b, II) shows that this process removes nearly all of the nanowires outside of the desired features. Nanowires can be observed to extend outside of the periodic circular feature (i.e., an end is fixed at the feature) at some points; however, these are infrequent and do not affect subsequent steps defining the nanodevice interconnections. Third, images of the underlying SU-8 mesh (Fig. 2.4b, III) and final device network with SU-8 passivated metal contacts and interconnects (Fig. 2.4b, IV) highlight the regular array of addressable nanowire devices realized in our fabrication process. Last, scanning electron microscopy (SEM) images (Fig. 2.4c) show that these device elements have on average 1–2 nanowires in parallel.

The 2D macroporous nanoelectronic structures were converted to free-standing macroporous networks by dissolution of the sacrificial Ni layers over a period of 1–

2 h (ref 7). Representative images of a free-standing nanoelectronic network (Fig. 2.4d, e) highlight the 3D and flexible characteristics of the structure and show how input/output (I/O) to the free-standing network can be fixed at one end outside of a solution measurement petri-dish chamber. Electrical characterization of individually-addressable nanowire device elements in a free-standing mesh demonstrates that the device-yield is typically $\sim 90\%$ (from 128 device design) for the free-standing nanoelectronic mesh structures fabricated in this way. The average conductance of the devices from a representative free-standing mesh (Fig. 2.4f), $2.85 \pm 1.6 \mu\text{S}$, is consistent with 1–2 nanowires/device based on measurements of similar (30 nm diameter, 2 μm channel length) *p*-type Si single nanowire devices [26], and thus also agrees with the structural data discussed above. In addition, by varying the printed nanowire density and S/D metal contact widths, it is possible to tune further the average number of nanowires per device element.

These 2D freestanding macroporous nanoelectronic networks can be transformed into 3D structures by manually rolled-up into 3D arrays (Fig. 2.4g). To better control the microstructure of the 3D macroporous structure, a mechanics-driven approach was demonstrated through introducing built-in stress in metal interconnects with a tri-layer metal stack, which self-organize the 2D macroporous network into a scrolled structure [13, 27]. Importantly, the reconstructed 3D confocal fluorescent image of a 3D macroporous nanoelectronic network produced in this manner (Fig. 2.4h) shows a clearly scrolled 3D structure that separate each layer of nanowire devices and distribute the nanowire devices evenly in 3D space with a $>99\%$ free volume. More generally, these mechanics-driven 3D macroporous nanoelectronic structures could be readily diversified to meet goals for different hybrid materials using established mechanical design and bifurcation strategies [28].

2.3.2 Mechanics Analysis

The 3D macroporous nanoelectronic networks consist of single-layer polymer (SU-8) structural and three-layer ribbon (SU-8/metal/SU-8) interconnect elements. The effective bending stiffness per unit width of the 3D macroporous nanoelectronic networks can be estimated [29] by Eq. (2.1)

$$\overline{D} = \alpha_s D_s + \alpha_m D_m \quad (2.1)$$

where α_s and α_m are the area fraction of the single-layer polymer and three-layer interconnect ribbons in the networks. $D_s = E_s h^3/12$ is the bending stiffness per unit width of the single-layer polymer, where $E_s = 2 \text{ GPa}$ and h are the modulus and thickness of the SU-8. For a SU-8 ribbon with 500 nm thickness, D_s is 0.02 nN m. D_m is the bending stiffness per unit width of a three-layer structure, which includes 500 nm lower and upper SU-8 layers and 100–130 nm metal layer, and was measured experimentally as described below and shown in Fig. 2.2.

Qualitatively, the facile manipulation of the macroporous nanoelectronic networks to form 3D structures suggests a very low effective bending stiffness. We have evaluated the effective bending stiffness, $\overline{D}$, using a combination of calculations and experimental measurements. Due to the residual stress, the SU-8/metal/SU-8 elements bend upward from the substrate (due to internal stress of the asymmetric metal layers) with a constant curvature, K_0 , and projected length, l , where l_0 is the free length defined by fabrication. We use the curvilinear coordinate, s , to describe the distance along the curved ribbon from the fixed end, and the coordinate, χ , to describe the projection position of each material point of the ribbon (Fig. 2.5a). For a specific material point with distance s , the projection position χ can be calculated as $x = \int \cos \psi ds$, where $\psi = K_0 s$ is the angle between the tangential direction of the curvilinear coordinate s and the horizontal direction (Fig. 2.5b). Integration yields $x = \sin(K_0 s)/K_0$ and when $\chi = l$ and $s = l_0$, $K_0 = 0.0128 \mu\text{m}^{-1}$ for typical experimental parameters $l_0 = 100 \mu\text{m}$ and $l = 75 \mu\text{m}$.

As the element is deflected a distance, d , by the AFM tip with a force, F , each material point is rotated by an angle, φ , (Fig. 2.5b), where the anti-clockwise direction is defined as positive. Assuming a linear constitutive relation between the moment M and curvature change $d\varphi/ds$ [30] yields

$$\frac{d\varphi}{ds} = \frac{M}{wD_m} \quad (2.2)$$

where M is the moment as a function of position, x (Fig. 2.5), and w is the width.

$$M(x) = -F(l - x) \quad (2.3)$$

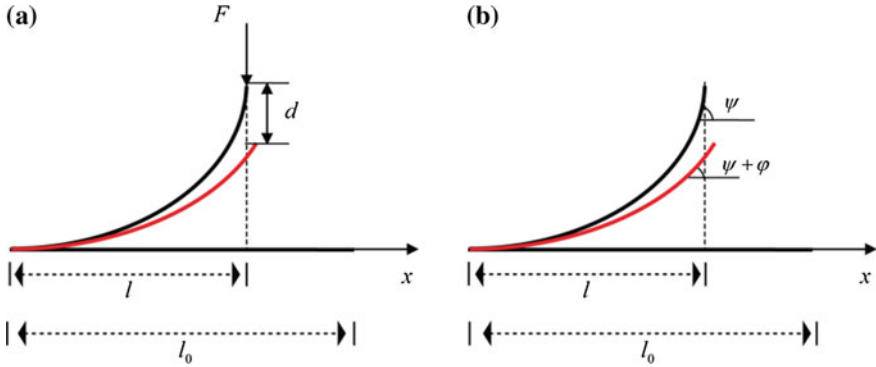


Fig. 2.5 Schematics for bending stiffness calculation. **a** A schematic of the position of the substrate free beam before (black) and after (red) applying a calibrated force, F , and vertical displacement, d , at the end of the beam with the AFM. **b** The angle between the tangential direction of a material point on the beam and the horizontal direction, ψ , of the ribbon before (black) and after displacement, $\psi + \varphi$, (red). l_0 : the total length of the ribbon. l : projection of the ribbon

Solving for the bending stiffness, D_m , with the assumption that φ is small so that $\sin \varphi \approx \varphi$ yields:

$$D_m = \frac{F}{wd} \left(\frac{ll_0 \sin(K_0 l_0)}{K_0} + \frac{1}{K_0^2} \left(l \cos(K_0 l_0) - l + \frac{l_0}{2} \right) + \frac{1}{K_0^3} \left(\frac{\sin(2K_0 l_0)}{4} - \sin(K_0 l_0) \right) \right) \quad (2.4)$$

The slope of a representative loading force-deflection curve, yields $F/d = 12 \text{ nN}/\mu\text{m}$ (Fig. 2.2c), and using Eq. (2.4) the calculated bending stiffness per width ($w = 5 \mu\text{m}$) is $D_m = 0.358 \text{ nN m}$. For typical 3D macroporous nanoelectronic networks the area fraction for both types of elements (i.e., SU-8 and SU-8/metal/SU-8) can range from 1 to 10%, yielding values of the effective bending stiffness from 0.0038 to 0.0378 nN m.

2.4 Conclusions

We have demonstrated a general strategy combining bottom-up and mechanics-driven approaches for preparing regular 3D interconnected and addressable macroporous nanoelectronic networks from 2D nanoelectronic “pre-cursors” that are fabricated by conventional lithography. The 3D networks have porosities larger than 99%, contain 100’s of addressable nanowire devices, and have feature sizes from the 10 micron scale for electrical and structural interconnections to the 10 nm scale for the functional nanowire device elements. The network is extremely flexible with the bending stiffness from 0.0038 to 0.0378, which is the most flexible electronics reported.

Bibliography

1. Reuss RH, Hopper DG, Park JG (2006) Macroelectronics. *MRS Bull* 31:447
2. Tian B et al (2012) Macroporous nanowire nanoelectronic scaffolds for synthetic tissues. *Nat Mater* 11:986
3. Al-sarawi SF, Abbott D, Franzon PD (1998) A review of 3-D packaging technology. *IEEE Trans Compon Packag Manuf Technol* 21:2
4. Benkart P et al (2005) 3D chip stack technology using through-chip interconnects. *IEEE Des Test Comput* 22:512
5. Ahn JH et al (2006) Heterogeneous three-dimensional electronics by use of printed semiconductor nanomaterials. *Science* 314:1754
6. Javey A, Nam S, Friedman RS, Yan H, Lieber CM (2007) Layer-by-layer assembly of nanowires for three-dimensional, multifunctional electronics. *Nano Lett* 7:773
7. Liu J et al (2013) Multifunctional three-dimensional macroporous nanoelectronic networks for smart materials. *Proc Natl Acad Sci USA* 110:6694–6699
8. Wu Y et al (2004) Controlled growth and structures of molecular-scale silicon nanowires. *Nano Lett* 4:433

9. Butt HJ, Jaschke M (1995) Calculation of thermal noise in atomic force microscopy. *Nanotechnology* 6:1
10. Tian B et al (2010) Three-dimensional, flexible nanoscale field-effect transistors as localized bioprobes. *Science* 329:831
11. Yang C, Zhong ZH, Lieber CM (2005) Encoding electronic properties by synthesis of axial modulation-doped silicon nanowires. *Science* 310:1304
12. Tian BZ, Xie P, Kempa TJ, Bell DC, Lieber CM (2009) Single-crystalline kinked semiconductor nanowire superstructures. *Nat Nanotechnol* 4:824
13. Fan Z et al (2008) Wafer-scale assembly of highly ordered semiconductor nanowire arrays by contact printing. *Nano Lett* 8:20
14. Lu W, Lieber CM (2007) Nanoelectronics from the bottom up. *Nat Mater* 6:841
15. Lieber CM, Wang ZL (2007) Functional nanowires. *MRS Bull* 32:99
16. Qian F, Gradecak S, Li Y, Wen Y, Lieber CM (2005) Core/multishell nanowire heterostructures as multicolor, high-efficiency light-emitting diodes. *Nano Lett* 5:2287
17. Tian B et al (2007) Coaxial silicon nanowires as solar cells and nanoelectronic power sources. *Nature* 449:885
18. Gao R et al (2012) Outside looking in: nanotube transistor intracellular sensors. *Nano Lett* 12:3329
19. Jiang X et al (2011) Rational growth of branched nanowire heterostructures with synthetically encoded properties and function. *Proc Natl Acad Sci USA* 108:12212
20. Yan H et al (2011) Programmable nanowire circuits for nanoprocessors. *Nature* 470:240
21. Xiang J et al (2006) High performance field effect transistors based on Ge/Si nanowire heterostructures. *Nature* 441:489
22. Cui Y, Wei Q, Park H, Lieber CM (2001) Nanowire nanosensors for highly sensitive and selective detection of biological and chemical species. *Science* 293:1289
23. Qin Y, Wang XD, Wang ZL (2008) Microfibre-nanowire hybrid structure for energy scavenging. *Nature* 451:809
24. Chan CK et al (2008) High-performance lithium battery anodes using silicon nanowires. *Nat Nanotechnol* 3:31
25. Zheng GF, Patolsky F, Cui Y, Wang WU, Lieber CM (2005) Multiplexed electrical detection of cancer markers with nanowire sensor arrays. *Nat Biotechnol* 23:1294
26. Leong TG et al (2009) Tetherless thermobiochemically actuated microgrippers. *Proc Natl Acad Sci USA* 106:703
27. Freund LB (2000) Substrate curvature due to thin film mismatch strain in the nonlinear deformation range. *J Mech Phys Solids* 48:1159
28. Kim DH et al (2011) Epidermal electronics. *Science* 333:838
29. Landau LD, Lifshitz EM (1986) *Theory of elasticity*, 3rd edn, Elsevier, pp 67–73

Biomimetics Through Nanoelectronics
Development of Three Dimensional Macroporous
Nanoelectronics for Building Smart Materials, Cyborg
Tissues and Injectable Biomedical Electronics
Liu, J.
2018, XX, 98 p. 48 illus. in color., Hardcover
ISBN: 978-3-319-68608-0