Chapter 2
Low-Noise CMOS Image Sensors

CMOS image sensors (CIS) as known today are the fruit of several decades of research and development culmination starting from the discovery of the photodetecting effect of pn junctions and the implementation of charge coupled devices (CCDs) as image sensors to the development of pinned photo-diodes (PPDs) in CMOS technology. Today, CIS is a mature technology, PPDs became standard devices and the optimal readout circuit schemes for each application are becoming well known. This Chapter recalls the historical background of CIS, presents a simplified physical model of the PPD and reviews the readout chain architectures implemented in the low-noise context.

2.1 Pinned Photodiodes

The pinned photo diode (PPD) is a photosensitive structure at the heart of almost all CMOS image sensors and even CCDs. PPDs became the first choice device in solid state image sensors due to their CMOS compatibility, high quantum efficiency and low dark current in addition to a readout process based on correlated double sampling which is prone to a low noise readout by canceling the reset noise and mitigating low frequency noise.

2.1.1 Brief Historical Review

The idea of using silicon devices as photodetectors goes back to 1965 when the photosensing effect of pn junctions has been revealed for the first time by G.P. Weckler [1, 2]. These early works showed that a reverse biased pn junction behaves as a capacitor charged by a photocurrent proportional to the incident light intensity.

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This device became the key element in the first MOS passive pixel sensors (PPS) designed by P.J.W. Noble [3] in 1968. These pn junctions were also introduced in the CCDs in a device called Inter Line Transfer (ILT) [4] in order to avoid using the CCD structure for both the light integration and the charge transfer. A transfer gate was introduced, in each pixel, between the pn junction and the CCD structure transferring the integrated photoelectrons through the whole column to the sense node located at the output of the chip for the readout. But the pn junction photodiodes performance was mainly limited by the sampled noise after reset, commonly referred to as the *kTC* noise and the incomplete charge transfer during the readout [5]. To address these issues, N. Teranishi invented the buried pn junction that was first presented in 1982 [6]. This buried structure consisted in adding a heavily doped p+ thin layer on the top of the n layer of the pn junction making it a vertical p+np structure. This device had also another virtue consisting in an extremely lower dark current compared to pn junctions [6]. The name of PPD has first been given to this structure in a 1984 publication [7] presenting an enhancement of the buried photo diode quantum efficiency through the reduction of the p+ layer thickness.

Thanks to the miniaturization of CMOS devices, the integration of in-pixel amplification became possible. E.R. Fossum was the first to take advantage of this aspect. He proposed the in-pixel integration of charge transfer and source follower buffering in 1993 [8, 9] and gave it the name of active pixel sensor (APS). This CMOS structure used a photogate as a detection device. The implementation of PPDs in CMOS pixels required further technological improvements to allow the charge transfer from the PPD to the sense node with low voltages compatible with CMOS processes. Such improvements emerged in the late 90 [10, 11] and early 2000 [12, 13]. The name of 4 T pixels is commonly given to the pixel structure combining the APS topology with a PPD phototdetector. In other words, an APS where the photogate is replaced by a PPD. The name of 4 T pixels was given by contrast to the 3 T pixel structure designating a pixel with a photodiode directly connected to a source follower with a reset and selection switches. The 4 T pixel has the additional transfer gate separating the PPD from the sense node. The fabrication of APS with PPDs in CMOS processes was a major turning point in the image sensor industry. From this point, the CMOS image sensors started challenging and advancing CCDs even at the sensitivity level. The sensitivity of CIS based on PPD was further optimized in terms of quantum efficiency by introducing back-side-illumination (BSI). BSI was first introduced for CCDs to enhance their quantum efficiency by exposing the back side of the chip to the incident light instead of the front side which is partially covered by the gates and metal wires [14, 15]. BSI was adapted to the CIS industry and became a standard in the late 2000 included even in the mass produced consumer applications [5]. The color filter and micro lenses layers are stacked in the back side of the chip and the front side metal layers act as light reflector further increasing the quantum efficiency.

2.1.2 Device Physics

As mentioned in the historical review, the PPDs have been first developed in CCD technology for their low spill back and lag, low dark current and good quantum efficiency. These devices have been implemented after in CIS. The PPD structure consists in a np junction buried under a shallow highly doped p+ thin layer. A few physical models of the PPD have been proposed in the literature [16–18]. In this section, we give a basic physical model of the PPD leading to a simple derivation of the potential shape and pin voltage value and position. The PPD is nothing else than two pn junctions sharing the same n doped area as depicted in Fig. 2.1. The junctions give rise to depletions in both sides of each junction. When the concentration of free carriers is mainly given by the doping concentration, the full depletion approximation can be used. The latter assumes that the depletion length in each side of the junctions have a clear edge and the transition between the depleted (charged) and non-depleted (neutral) regions is abrupt [19]. These assumptions are justified by the exponential dependence of the carrier concentration on the gap between the Fermi level and band edges.

Consider the case when the depletion regions of the p+n and np junctions merge in the n layer. The n layer of the PPD becomes fully depleted as depicted in Fig. 2.1. x_n marks the edge between the p+ and n layers while x_p marks the border between the latter and the epitaxial p bulk. x_{p_1} is the depletion edge abscissa of the p+n junction and x_{p_2} corresponds the depletion edge for the p junction. The charge distribution, under the full-depletion approximation, corresponding to the structure described in Fig. 2.1 is shown in Fig. 2.2a. For the sake of simplification, we do not consider the case of linear doping concentration in the n layer.

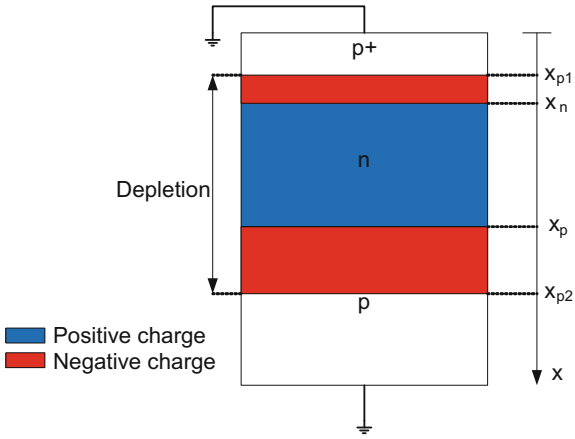

Fig. 2.1 Structure of the stacked p+np layers in the PPD

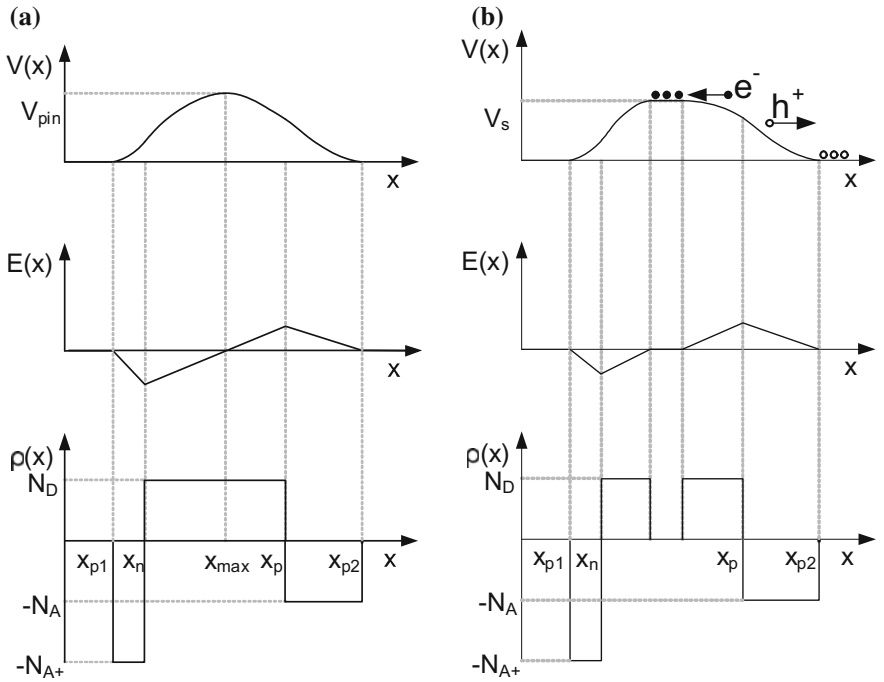

Fig. 2.2 Charge density, electric field and potential under the full depletion approximation for a fully depleted PPD (**a**) and after integration (**b**)

The key equation relating the electric field and potential to the charge distribution is the Poisson equation which is expressed as:

$$\frac{d^2V(x)}{dx^2} = -\frac{dE(x)}{dx} = -\frac{\rho(x)}{\varepsilon_s}, \tag{2.1}$$

where $V(x)$ is the potential, $E(x)$ is the electric field, $\rho(x)$ is the charge density and ε_s is the semiconductor dielectric constant. We add to these differential equations the global boundary conditions which are field free and zero potential at the level of the surface and the p substrate. Based on Fig. 2.2a, five different regions can be distinguished based on the distribution of $\rho(x)$. The continuity of the electric field and potential across the different regions of the PPD is also a constraint to take into consideration.

2.1.2.1 Neutral p+ and p Regions

The neutral p+ region is delimited by $0 \leq x < x_{p_1}$. For the p epitaxial substrate it corresponds to $x_{p2} \leq x$. These areas of the semiconductor are not depleted, hence the

charge density is nul ($\rho(x) = 0$). Consequently, these two areas are field free with a zero potential.

2.1.2.2 Depleted p+ Region

The depleted region of the p+ layer is located within $x_{p_1} \leq x < x_n$. The charge density in this area is determined by the hole impurities density as

$$\rho(x) = -qN_{A^+}. \tag{2.2}$$

N_{A^+} is of the order of 10^{18} to $10^{19}\,\mathrm{cm}^{-3}$ which is one to two orders of magnitude higher than the concentration of donors in the n layer and a few orders of magnitude higher that the p substrate concentration ranging between 10^{15} and 10^{16}.

The electric field is then derived by solving (2.1) for the boundary condition of $E(x_{p_1}) = 0$ verifying the continuity of the electric field at x_{p_1}. $E(x)$ simplifies to

$$E(x) = -\frac{qN_{A^+}}{\varepsilon_s}(x - x_{p_1}) \text{ for } x_{p_1} \leq x < x_n. \tag{2.3}$$

Consequently, the potential over x in this region can be expressed, in the way that verifies its continuity at x_{p_1}, as

$$V(x) = \frac{qN_{A^+}}{2\varepsilon_s}(x - x_{p_1})^2 \text{ for } x_{p_1} \leq x < x_n. \tag{2.4}$$

2.1.2.3 Depleted n Region

This region corresponds to $x_n \leq x < x_p$. The depleted n region is in a certain way the result of the merging between the depletions of the p+n and np junctions. The charge density under full depletion is given by the density of donor impurities N_D. The density of donors in this area is considered to decrease linearly with x. Here we suppose N_D constant for simplification since this linear dependence over x does not have a fundamental impact on the potential shape. The charge density is hence expressed as

$$\rho(x) = qN_D. \tag{2.5}$$

The electric field is then expressed using the Poisson equation (2.1) and the continuity condition at $x = x_n$ using (2.3). This yields to

$$E(x) = \frac{qN_D}{\varepsilon_s}(x - x_n) - \frac{qN_{A^+}}{\varepsilon_s}(x_n - x_{p_1}) \text{ for } x_n \leq x < x_p. \tag{2.6}$$

Consequently, the potential verifying the Poisson equation and the continuity at x_n can be expressed as

$$V(x) = -\frac{qN_D}{2\varepsilon_s}(x - x_n)^2 + \frac{qN_{A^+}}{\varepsilon_s}(x_n - x_{p_1})x - q\frac{qN_{A^+}}{\varepsilon_s}(x_n - x_{p_1})(x_n + x_{p_1}) \text{ for } x_n \leq x < x_p. \tag{2.7}$$

2.1.2.4 Depleted p Region

The depleted region of p substrate corresponds to $x_p \leq x < x_{p_2}$. The charge density in this area is determined by the hole impurities density in the epitaxial substrate as

$$\rho(x) = -qN_A. \tag{2.8}$$

The electric field is then derived by solving (2.1) for the boundary condition of $E(x_{p_2}) = 0$ verifying the continuity of the electric field at x_{p_2}. $E(x)$ simplifies to

$$E(x) = -\frac{qN_A}{\varepsilon_s}(x - x_{p_2}) \text{ for } x_p \leq x < x_{p_2}. \tag{2.9}$$

Consequently, the potential over x in this region can be expressed, in the way that verifies is continuity at x_{p_2}, as

$$V(x) = \frac{qN_{A^+}}{2\varepsilon_s}(x - x_{p_2})^2 \text{ for } x_p \leq x < x_{p_2}. \tag{2.10}$$

Note that the continuity must also be verified between the depleted p and n regions. This condition leads to the following equation

$$N_A x_{p_2} - N_{A^+} x_{p_1} = (N_A + N_D)x_p - (N_{A^+} + N_D)x_n. \tag{2.11}$$

This equation sets the relationship between the doping concentrations and the depletion width of the PPD.

2.1.2.5 Pin Voltage

Based on the Eqs. (2.4), (2.7) and (2.10), the potential takes its maximum in the depleted n region. The position x_{max} corresponding to this maximum corresponds to the abscissa where the electric field is nul. Hence x_{max} is obtained by solving the equation $E(x) = 0$ in the depleted n region as

$$x_{max} = x_n + \frac{N_{A^+}}{N_D}(x_n - x_{p_1}). \tag{2.12}$$

Let us first verify that x_{max} is comprised between x_n and x_p. It is clear from (2.13) that x_{max} is higher than x_n. The continuity condition (2.11) can be used to express x_{max} as a function of x_p. Based on this equation x_{max} can also be expressed as

$$x_{max} = x_p - \frac{N_A}{N_D}(x_{p_2} - x_p). \tag{2.13}$$

Hence x_{max} is comprised between x_n and x_p.

The pin voltage can be expressed by substituting x_{max} in (2.7) as

$$V_{pin} = \frac{qN_{A^+}}{2\varepsilon_s} \cdot \frac{N_{A^+} + N_D}{N_D}(x_n - x_{p_1})^2. \tag{2.14}$$

The pin voltage expression obtained in (2.14) is exactly the built-in voltage of the p+n junction. Indeed this result shows that the pin voltage of the p+np structure of the PPD can be determined by analyzing the Fermi level gaps between the layers. The Fermi level gap between the p+ and n layers is given by

$$V_{bi1} = \frac{kT}{q} ln\left(\frac{N_{A^+}N_D}{n_i^2}\right), \tag{2.15}$$

where V_{bi1} is the built-in potential of the p+n junction. The Fermi level gap between the n layer and the epitaxial p is given by

$$qV_{bi2} = \frac{kT}{q} ln\left(\frac{N_A N_D}{n_i^2}\right), \tag{2.16}$$

where V_{bi2} is the built-in potential of the pn junction. As mentioned previously, the doping concentration in the p+ layer is a few orders of magnitude higher than the one in the epitaxial p layer. Hence

$$V_{bi1} > V_{bi2} \tag{2.17}$$

Consequently, the built-in potential in the p+np structure when the Fermi levels of the different layers become equal is given by the highest energy gap which corresponds to the p+n junction. Finally the pin voltage can be expressed as

$$V_{pin} = \frac{kT}{q} ln\left(\frac{N_{A^+}N_D}{n_i^2}\right). \tag{2.18}$$

For instance, for a doping concentration in the p+ layer N_{A^+} of $10^{18}\,cm^{-3}$ and a donors concentration in the n layer of $10^{16}\,cm^{-3}$, the pin voltage at 300 K would be 0.8 V.

Note that in the simplified analysis presented above, the linear doping concentration over the PPD n well [5] is not considered and replaced by a flat concentration

over the n well. This analysis does not include the horizontal border effects on the PPD and the impact of the PPD width and length on the pin voltage [20].

2.1.2.6 Charge Photo-Generation and Integration

The band gap energy of the silicon is about 1.1 eV. A visible photon has an energy ranging between 3.5 and 1.5 eV. For front side illumination, the thin p+ layer on the top of the PPD is transparent and the photon gets absorbed by silicon atoms located in the depleted region. Since the photon energy is higher than the silicon band gap, an electron-hole pair is generated. Due to the electric field in the depleted region (Fig. 2.2a), the electron is attracted by the position corresponding to the maximum potential and the hole sinks in the ground through the substrate. Each photoelectron located at the depleted n well compensates the positive charge of a donor hole. Hence, with cumulated photoelectrons, a neutral region starts to grow in both sides of the maximum voltage position (x_{max}) as depicted by Fig. 2.2b. The PPD is saturated when the depleted region in the n well disappears due to the cumulated electrons. Consider a PPD section of area A. The total positive charge in the PPD volume corresponding to the section A in the n well between x and x_{max} is given by $q \cdot N_D \cdot A \cdot (x_{max} - x_n)$. Hence, a number of $N_D \cdot A \cdot (x_{max} - x_n)$ photoelectrons is enough to saturate this section of a PPD, since there will be no maximum voltage, which gives an estimation of the PPD full well capacity FWC. For a doping concentration of $10^{16}\,cm^{-3}$ and an n layer depth of 0.25 µm the rough estimation of the maximum storage charge is about $2.5\,ke^{-}/\mu m^2$.

2.1.3 Device Operation

Figure 2.3 shows the conventional schematic of a pixel based on a PPD. The cross section of a PPD allows to see stacked n and p+ layers as well as the shallow trench insulator (STI) used to isolate the PPD. A heavily doped p+ area separates the STI oxide from the PPD n well and p epitaxial layer in order to reduce the impact of interface imperfections as will be shown in the next Chapter. The transfer gate (TG) is used to control the potential barrier at the edge of the PPD. When the TG voltage is low enough, the potential under the transfer gate is lower enough than the pin voltage of the PPD in order to keep the integrated charge in the PPD n well. Typical values of the TG low voltage range between 0 V and slightly negative values for dark current issues as will be discussed in the next Chapter. The sense node is simply an n+p junction capacitance. The voltage at the surface of the n + layer is set to a high voltage in the 2.5–3.3 V range creating a depletion at the n+p interface. The sense node voltage is read by an adequate electronic circuit that will be detailed in the next Section. After sensing the reset level, the TG voltage is increased creating a depletion

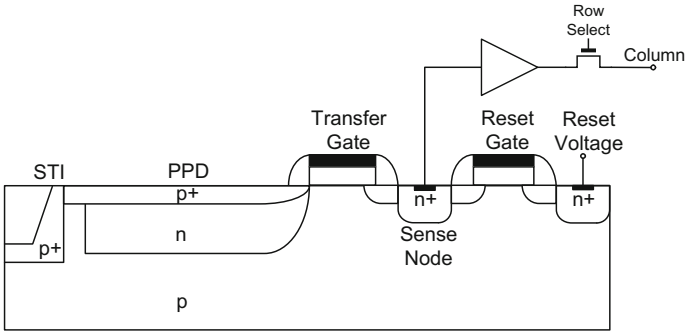

Fig. 2.3 Global architecture of a pixel based on a PPD

under the transfer gate where the potential is higher that the PPD pin voltage and in the mean time lower than the sense node maximum voltage. During this time, the depletion regions under the sense node, the transfer gate and in the PPD n well merge and the electrons cumulated in the PPD during the integration phase diffuse towards the higher potential area under the transfer gate and then to the sense node where the potential is even higher. The charge diffusion to the sense node causes its voltage level to drop from the reset level with a step proportional to the transferred charge. This voltage is sensed and the reset level voltage is then subtracted to obtain the signal level only assuming the reset level has remaind constant. This operation is called correlated double sampling (CDS). It not only subtracts the constant reset level but also reduces the noise that is correlated between the reset time and the transfer time such as the flicker noise [21].

The charge storage and transfer discussed above can be described by the hydraulic model of Fig. 2.5 that shows the different readout steps according to the operation timing diagram of Fig. 2.4 showing also the reset and transfer samples of the CDS.

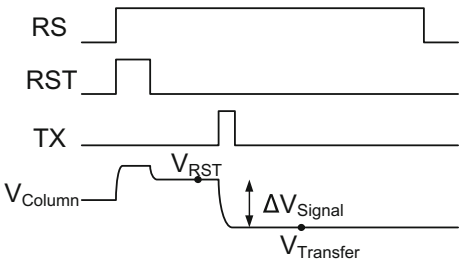

Fig. 2.4 Readout timing diagram of a conventual pixel based on a PPD

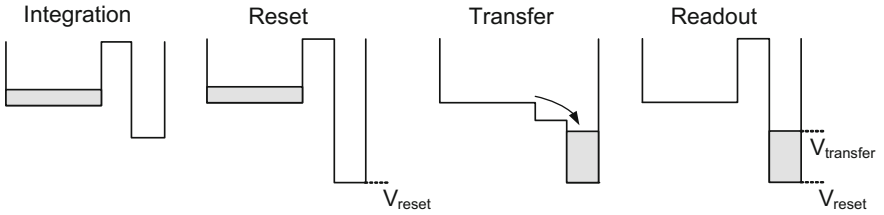

Fig. 2.5 Hydraulic model of a PPD with the transfer gate and sense node regions showing the different readout steps

2.2 CIS Global Architecture

Figure 2.6 shows the overall block diagram of a conventional low noise CIS. The pixels array is at the center of the imager. It occupies most of the chip silicon area. Each pixel comprises a pinned photodiode with at least one amplifying transistor and three MOS switches for reset, transfer and row selection. In order to achieve high frame rates, a column parallel readout scheme is generally performed. The pixels array is read line by line and all the pixels of the same line are read in parallel. Hence, at the top of the lines, a mixed signal control block made of shift registers and level shifters is generally implemented in order to drive the pixel lines by generating the row selection, reset and transfer commands. At the bottom of the columns, analog amplification is generally implemented before the correlated sampling and analog-to-digital conversion. Figure 2.7 shows the timing diagram of a conventional CIS readout chain. It shows the main line control signals as well as the timing of the column level signal processing. Each pixel line is generally addressed with the same frequency as the frame rate. Hence the PPDs remain exposed to the light between two consecutive readouts. In order to control the exposure time of the pixels, an intermediate reset and transfer operation can be performed in order to empty the PPDs between two consecutive readouts. The integration time is then set by the time interval between that charge transfer resetting the PPD and the one performed during the readout. At the column level, the correlated sampling and the analog-to-digital-conversion (ADC) are performed after the column-level amplification. The digital data is then stored in static random access memories SRAMs. These SRAMs are then shifted horizontally to the digital output of the chip. For a higher frame rate, the horizontal shift of each frame is performed at the beginning of the next frame as shown in the timing diagram of Fig. 2.7.

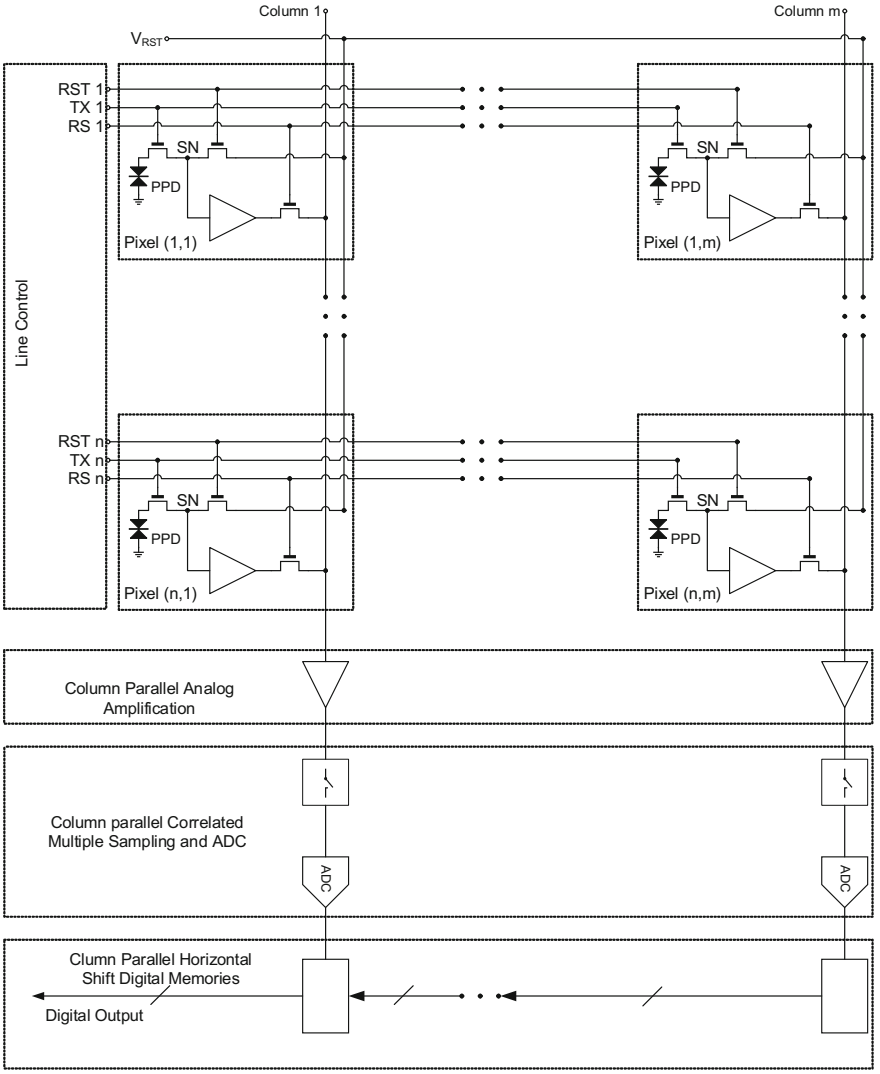

Fig. 2.6 Block diagram of a low noise CIS

2.3 Pixel Architectures

In any sensor readout chain, the low noise amplification must be applied at the earliest stage of the readout chain. In the case of CCDs, the amplification was applied at the output level of the chip since the CCDs do not offer the possibility of integrating any electronics at the pixel level [22]. Indeed the charge was transferred from pixel to pixel vertically then horizontally until the sense node located at the chip output. The

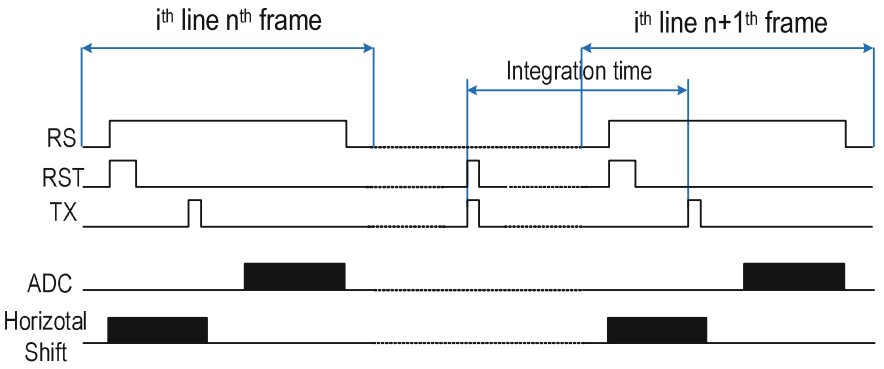

Fig. 2.7 Timing diagram of a conventional low noise CIS

idea of integrating electronic amplification at the pixel level goes back to the early beginnings of CMOS image sensors [23, 24] with 3 T pixels. The main advantage of this in-pixel amplification is the separation between the sense node of the pixel and the column level parasitic capacitance. Indeed, without in-pixel amplification, the photodiode would be directly connected to the column through the pixel (row) selection switch MOS transistor [2]. In this configuration, the sense node capacitance would be of the order of several pF. Hence, each photoelectron integrated in the photodiode would only result in a few 160 nV which is a very weak signal to be detected by CMOS uncooled electronics.

In order to optimize the quantum efficiency and fill factor of the pixel, the in-pixel amplification is introduced with the minimum number of MOS transistors. When operated in saturation, a single MOS transistor can operate as a voltage amplifier in three possible topologies, namely, the source follower (common drain), the common source and common gate configurations [25]. In the common gate configuration, the bias current of the amplifying transistor flows through the input voltage source which is not practical in active image sensors since the sense node is either connected to the photodiode or to a sense node junction. Hence, the source follower and common source topologies are the most popular in-pixel amplifying schemes used in CMOS image sensors.

2.3.1 Source Follower Based Pixel

The in-pixel source follower (SF) topology is the most common configuration in CIS. Figure 2.8a shows the schematic of the source follower stage. The sense node is connected to the gate of the amplifying transistor and the output voltage is produced at its source. In this configuration, the transistor is used as a voltage buffer. The output voltage as a function of the sense node voltage is depicted in Fig. 2.8b. This DC characteristic shows two important advantages of the source follower scheme.

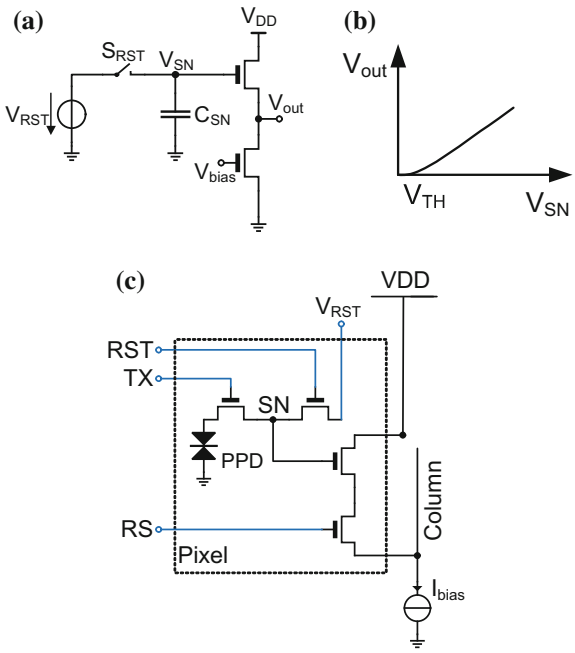

Fig. 2.8 Circuit topology of a source follower stage (**a**), the DC characteristic (**b**) and a schematic of a pixel based on in-pixel source follower buffer (**c**)

The first consists in a large voltage swing. For the 3.3 V transistors usually used in CIS pixels, the voltage swing of the pixel ranges between 1 and 2 V. The second advantage of the source follower scheme is the easy reset. Indeed, the sense node can be reset without much constraints about the exact reset voltage value at the sense node. Hence, this readout scheme is robust against the reset switch imperfections [21]. Figure 2.8(c) shows the schematic of a source follower based 4 T pixel. The current bias of the source follower stage is connected to the column. Hence, the current bias is connected to the in-pixel SF transistor only when the row selection switch connects the pixel to the column during the readout.

2.3.2 Common Source Based Pixel

Figure 2.9a shows the schematic of the common source stage with a PMOS load. In this readout scheme, the sense node is connected to the gate of the amplifying transistor and the output voltage is produced at its drain. The output voltage as a function of the sense node voltage is depicted in Fig. 2.9b. This DC characteristic exhibits two main differences compared to the source follower stage. The first consists in the in-pixel voltage gain at the cost of a proportionally lower voltage swing. The second difference consists in the necessity of a precise feedback reset. Indeed, this reset scheme is necessary to make sure that the sense node voltage is at the linear

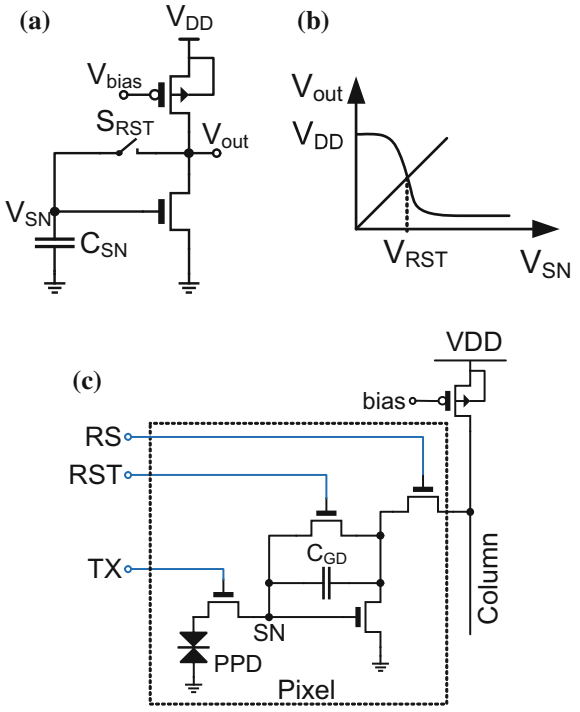

Fig. 2.9 Circuit topology of a common source stage (**a**) the DC characteristic (**b**) and schematic of the pixel based on a common source in-pixel amplification (**c**)

part of the DC characteristic. Note that the common source stage is very sensitive to the reset switch non-ideality. In fact a charge injection induced by this switch can set the sense node voltage in a saturation point.

Figure 2.9(c) shows the schematic of a pixel based on a common source amplification. The in-pixel row selection switch connects the common source transistor the load located at the column level. The load can be implemented by a PMOS, NMOS or a passive resistive element. The common source configuration can be implemented as an open loop gain amplifier [26, 27] or as a capacitive transimpedence amplifier (CTIA) [28, 29] by introducing a capacitive feedback between the common source drain and gate. Note that the open loop gain configuration is a particular case of the CTIA for which the feedback capacitance is simply given by the gate to drain total parasitic capacitance of the in-pixel amplifying transistor.

2.4 Column-Level Amplification

The column-level amplifier is an important block in the readout chain. It is located between the pixel and the next processing stages, namely, the analog buffers, the track-and-holds and analog-to-digital converters. Hence, by introducing the gain

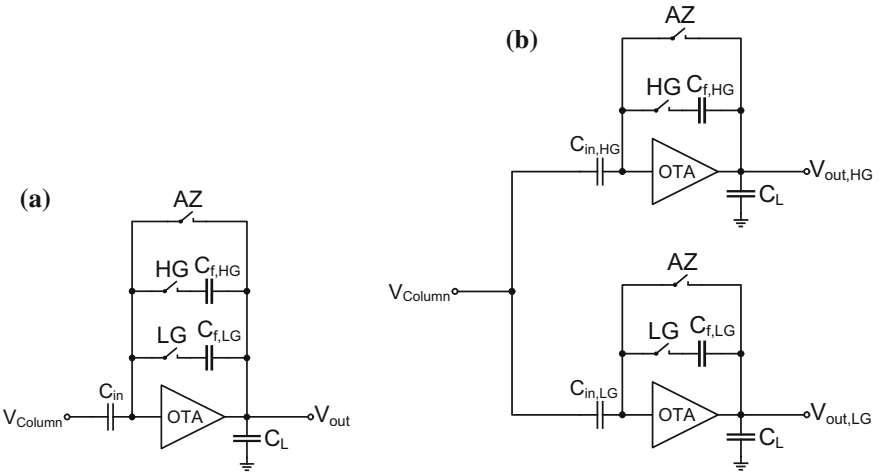

Fig. 2.10 Schematic of the column level switched capacitor amplifier with variable gain (**a**) and dual gain column level amplification

right after the pixel, the noise originating from these stages is minimized. One other important role of the column-level amplifier, especially with a source follower based pixel, is the bandwidth control reducing the thermal noise. The first implementation of column-level amplification leading to a low noise performance was published in [30] reporting a performance of $2\,e^-_{rms}$.

The column-level amplification is generally implemented with switched capacitor amplifiers as shown in Fig. 2.10a. The gain is set by the ratio between the input and feedback capacitors. The amplifier is reset after each readout thanks to an autozero that also dramatically reduces its offset and low frequency noise [21].

In low noise CIS readout chain, the column-level amplifier is especially necessary with the source follower based readout chain. For the best dynamic range, low column level gain is required to exploit as much as possible the full well capacity of the PPD and high column level gain is required for a low noise floor. Hence the column-level amplifier must perform low gain for images under good lighting conditions and high gain in the case of low light imaging. Hence, adaptative column-level gain [31] is required. Figure 2.10b shows the schematic of a parallel dual gain column-level amplifier. In this readout scheme, each pixel is read with both high and low gain levels. In this way, each frame of the imager corresponds to two images, one adequate for dark pixels and the other for highly illuminated pixels. Image post processing can be applied to combine both resulting in a higher dynamic range performance but at the cost of higher power consumption and larger silicon area.

2.5 Correlated Sampling and Analog-to-Digital Conversion

2.5.1 Correlated Double Sampling

Correlated double sampling (CDS) is similar to autozeroing except that the signal is sampled twice and then the difference is taken between these two samples. It has been introduced initially for image processing in CCDs [32, 33] then introduced to CIS. The CDS in the case of CIS is operated by differentiating two samples at the output of the sensor, one after resetting the sense node and the other one after the charge transfer.

The most common implementation of CDS is shown in Fig. 2.11a. In this configuration, two sample-and-hold circuits, connected in parallel to the output of the column level amplifier, are used. Figure 2.11(c) shows the timing diagram of the different control phases operating the readout chain depicted in Fig. 2.11a. First, the in-pixel reset (RST) transistor is switched on in order to reset the sense node. The column level amplifier auto-zero (AZ) switch is closed in order to clear the feedback capacitor C_f, reset the input voltage of the amplifier and store the offset of the amplifier in the input capacitor C_{in}. Once the AZ switch is opened, this offset is canceled. Note that this AZ also reduces the low frequency noise originating from the column level amplifier [21]. The first sample-and-hold circuit switch S_{SH1} is opened after the settling of the voltage corresponding to the reset level. The latter is then held in capacitor C_{SH1}. The TG is then pulsed to its higher level in order to transfer the charge from the PPD to the sense node. The voltage corresponding to the transfer level is then sampled after the signal settles in the second sample-and-hold circuit by opening the second switch S_{SH2}.

Another implementation of the CDS consists in performing the latter at the input of a single slope analog-to-digital converter (ADC). An example of such implementation is shown in Fig. 2.11b. The timing diagram of the control signal of this readout chain is shown in Fig. 2.11(d). During reset of the pixel and the column level amplifier auto-zeroing, the auto-zero switch of the comparator at the input of the ADC stage is closed. When the reset level voltage has settled at the output of the column level amplifier, this switch is opened in order to sample the reset level voltage in the capacitor C_{comp}. Instantaneously, the voltage at the positive input of the comparator becomes equal to the difference between the voltage at the output of the column level amplifier and the reset level voltage sampled in C_{comp}. Now the voltage sampled at the input of the comparator corresponds to the difference between the reset and transfer levels. The ramp then is activated synchronously with the counter and once the rampe voltage is equal to the voltage held at the positive input of the comparator, the latter switches to its high voltage level in order to store the counter value in the SRAM. The CDS time corresponds to the time between the comparator auto-zero and the switching of the comparator output. Note that, in this configuration, the CDS time depends on the signal level.

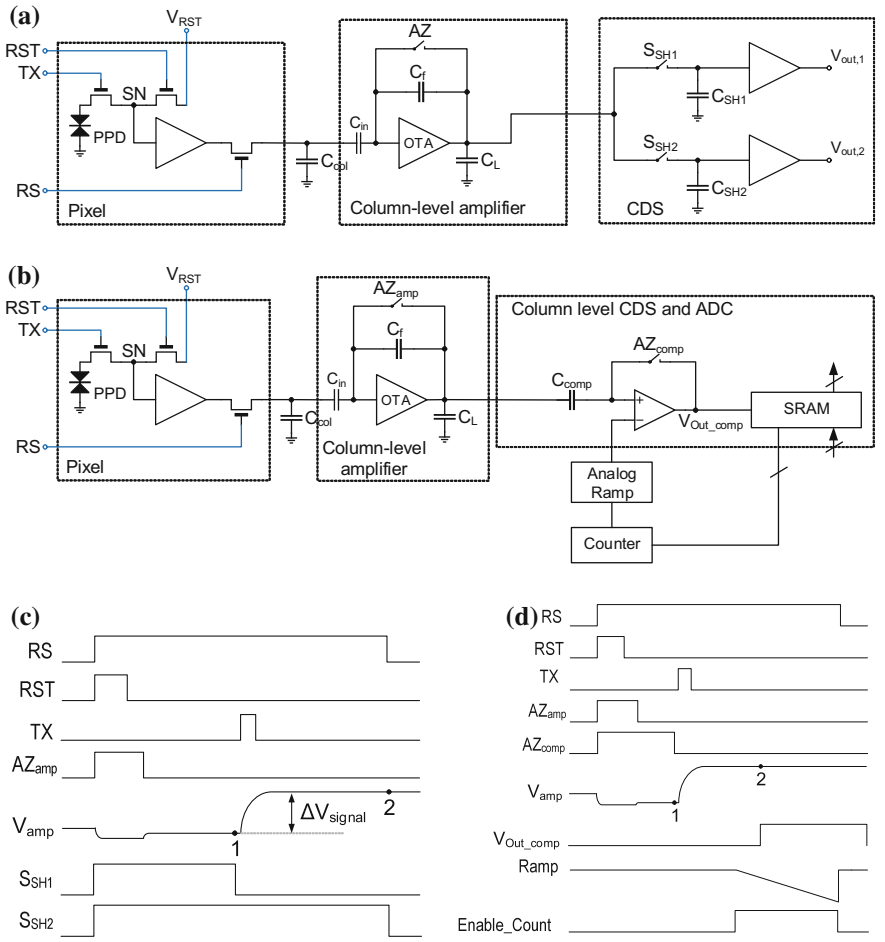

Fig. 2.11 Column level readout chain of a CIS with analog CDS implemented by two track-and-holds (**a**) and the corresponding timing diagram (**c**). Column level readout chain of a CIS with analog CDS implemented at the input of the ADC comparator (**b**) and the corresponding timing diagram (**d**)

2.5.2 Correlated Multiple Sampling

Correlated multiple sampling (CMS) was introduced for CIS in [34–36]. It combines CDS with averaging. CMS of order M corresponds to averaging M samples at the reset level and M samples after charge transfer and then differentiating the two averages. Figure 2.12 shows the timing diagram of CMS in case for a CIS readout chain. A CMS of order M corresponds to averaging M samples in of the reset level voltage and M other samples after transferring the charge from the PPD to the sense

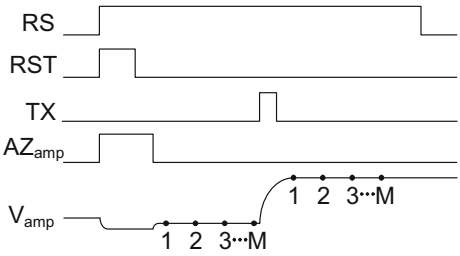

Fig. 2.12 Timing diagram of the an M-order CMS showing the M samples at the first and second voltage levels

node and settling of the signal. For the timing diagram of Fig. 2.12 the voltage at the output of an ideal CMS is expressed as:

$$V_{CMS} = \frac{1}{M}\sum_{i=1}^{M} V_{\text{transfer},i} - \frac{1}{M}\sum_{i=1}^{M} V_{\text{reset},i}. \tag{2.19}$$

Practically, CMS CIS readout chains can be performed with analog circuits or in the digital domain after ADC.

2.5.2.1 Analog CMS

An implementation of CMS with analog circuitry consists in using a column level integrator. The schematic of a CIS readout chain implementing this technique is shown in Fig. 2.13a. Figure 2.13b shows the corresponding timing diagram. In this configuration, after the reset of the sense node and auto-zeroing of the column-level amplifier, the column level voltage is sampled at the capacitor C_{in} and transferred to the amplifier feedback capacitor C_{f} using the switches S_{sample} and S_{transfer} as shown by the schematic and timing diagram. This operation is iterated M times in order to cumulate the charge corresponding to M consecutive samples in the feedback capacitor. This results in the voltage at the output of the integrator being equal to the sum of the M consecutive reset level voltage samples. The switch S_{SH1} is then opened in order to hold this reset level cumulated voltage in the capacitor C_{SH1}. The charge transfer from the PPD to the sense node is then performed and the same operation is iterated after settling of the transfer voltage level. The switch S_{SH2} is then opened to hold the transfer level voltage.

The integrator results hence in cumulating the reset level and transfer level samples instead of averaging. Thus, this configuration results in a dynamic range decrease by a factor M. An alternative to this implementation [36] consists in using folding integration by introducing a digitally assisted feedback that prevents the integrator from saturating. This implementation is obtained at the cost of additional active mixed signal circuitry.

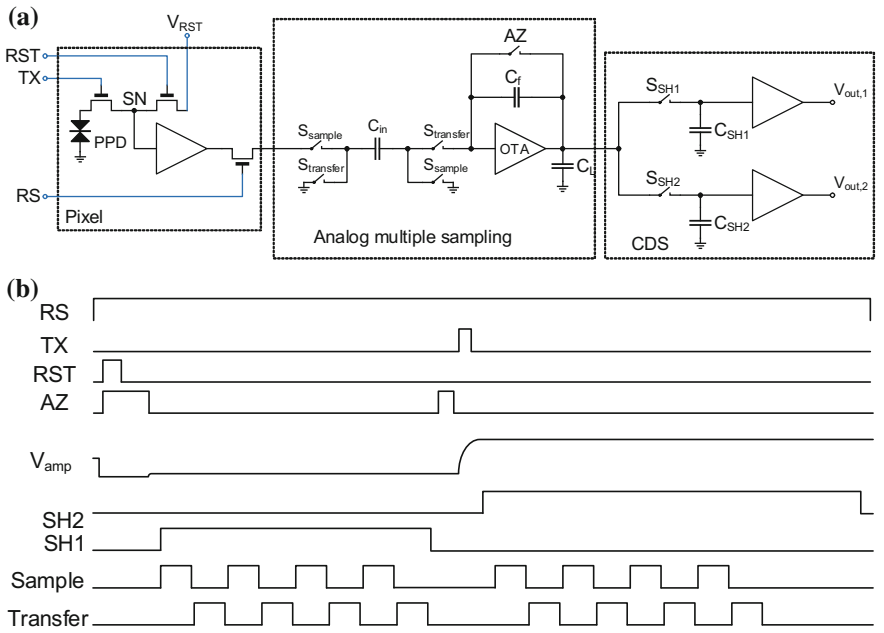

Fig. 2.13 Analog implementation of CMS using column-level integrator (**a**) and the corresponding timing diagram (**b**)

2.5.2.2 Digital CMS

CMS can also be performed in the digital domain [37, 38]. Figure 2.14b shows a readout chain based on a 4 T pixel, column-level amplification and multiple rampe ADC used to perform CMS by multiple analog-to-digital conversions using multiple ramping. The corresponding timing diagram is shown in Fig. 2.14a. After the sense node reset, the column level amplifier auto-zeroing and settling of the reset level voltage at the input node of the ADC comparator. Multiple ramps are iterated synchronously with a bitwise counter. The counts corresponding to M conversions are cumulated. Then the charge is transferred from the PPD to the sense node and the bitwise inversion is activated in order to set the counter in the count down mode. Similarly to the reset level voltage. The multiple ramping is activated in the same way after settling the transfer voltage level at the output of the column-level amplifier. But in this case the counter counts down subtracting in this way the cumulated transfer level voltage samples from the reset level ones.

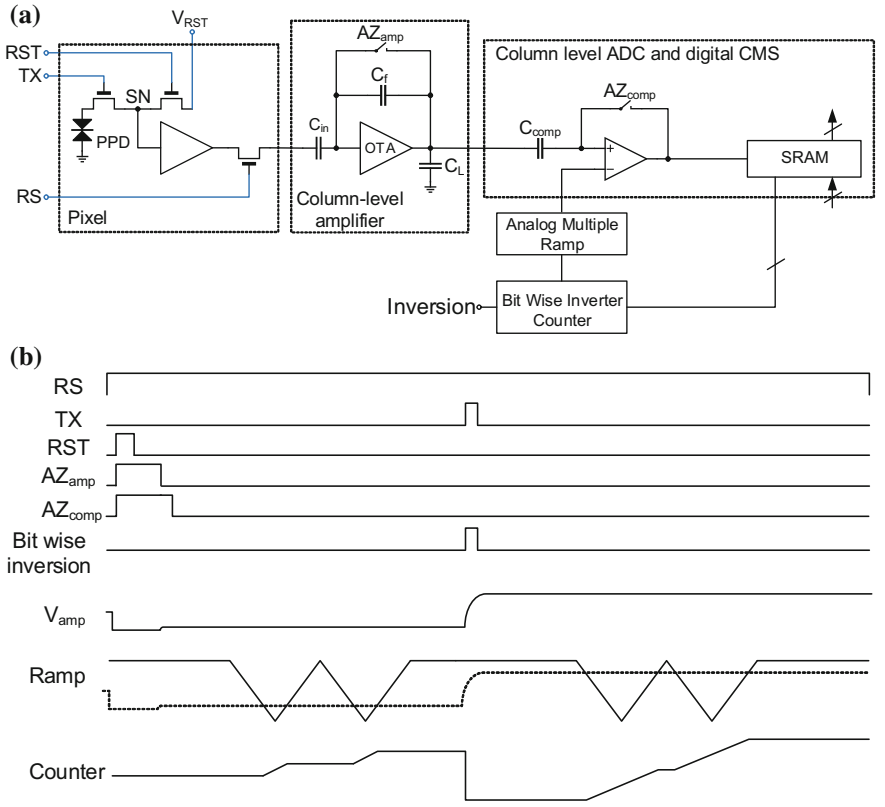

Fig. 2.14 Digital implementation of CMS using column-level multiple ramp ADC (**a**) and the corresponding timing diagram (**b**)

2.6 Summary

PPDs are the key element in low noise CIS. PPDs present a buried potential well in a depleted area that collects the photoelectrons. Low noise CIS pixels comprise, in addition to the PPD, at least four transistors to control the selection, reset and transfer. The fourth transistor is generally operated in the source follower configuration to buffer the voltage level of the sense node. The latter can also be used in the common source configuration for a higher pixel-level voltage gain. The pixel readout is performed in a double sampling scheme and the signal corresponds to the difference between the sense node voltage right after the reset and its level after the charge transfer from the PPD. This readout scheme cancels the reset sampled noise and reduces the low frequency noise originating from the readout chain electronics. CIS chips are generally built in a column parallel structure. The pixels of each line are simultaneously selected and read. The column level circuits include the bias current or load of the in-pixel amplification stage, the column-level amplifiers are used to

introduce a gain minimizing the noise contribution of the next stages and controlling the bandwidth for optimal thermal noise. The CDS and ADC take place after column amplification and can be implemented in different schemes. Signal multiple sampling and averaging can also be implemented for further noise reduction. In the low noise CIS context, the combination of averaging and double sampling is called CMS. It can be implemented with analog or digital circuitry.

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