

Chapter 2

Introduction: From Phase-Locked Loop to Costas Loop

The Costas loop can be considered an extended version of the phase-locked loop (PLL). The PLL has been invented in 1932 by French engineer Henri de Belleszice [1]. In his first application, de Belleszice used the PLL as a synchronous demodulator for double sideband amplitude modulated signals with carrier. The block diagram of a PLL is shown in Fig. 2.1. It is built from three blocks, a phase detector (PD), a loop filter (LF), and a voltage-controlled oscillator (VCO). In the first PLL applications, an analog multiplier was used for the phase detector [2]. Assuming for the first moment that both signals U_1 and U_2 are sinusoidal, we can write

$$\begin{aligned}u_1(t) &= U_{10} \sin(\omega_1 t + \theta_1) \\u_2(t) &= U_{20} \cos(\omega_1 t + \theta_2)\end{aligned}$$

where U_{10} , U_{20} are the amplitudes of U_1 and U_2 , respectively, ω_1 is the radian frequency of the input signal U_1 , and θ_1 and θ_2 are the zero phases of U_1 and U_2 , respectively. Assume further that the system is already locked, i.e., both signals have the same frequency, but can have different phases. In this case, the signals u_1 and U_2 differ by 90° in the locked state; hence, it is reasonable to define U_1 as a sine wave and U_2 as a cosine wave. It can be shown that the output signal of the phase detector is proportional to $\sin(\theta_1 - \theta_2) = \sin(\theta_e)$, where θ_e is called phase error. But the output signal of that type of phase detector also contains a high-frequency term, i.e., a sine term having radian frequency $2\omega_1$. This term is removed by the loop filter, which is mostly realized either as a lag-lead filter or as a PI filter (proportional

Electronic supplementary material The online version of this chapter (doi:[10.1007/978-3-319-72008-1_2](https://doi.org/10.1007/978-3-319-72008-1_2)) contains supplementary material, which is available to authorized users.

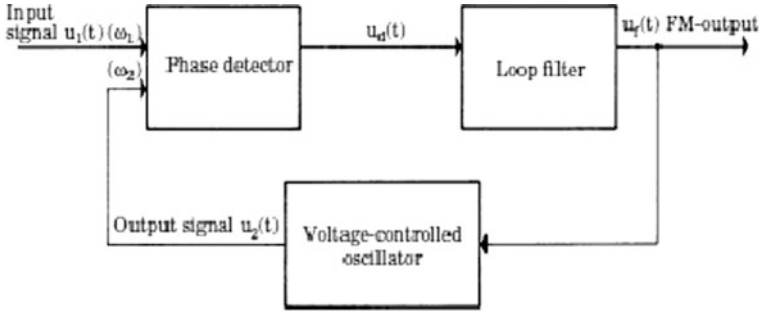


Fig. 2.1 Block diagram of a phase-locked loop

and integral filter). More about loop filters later in this text. The output signal u_f of the loop filter is applied to the input of the VCO. When there exists a phase error, the frequency of the VCO is adjusted such that finally the phase error becomes either 0 or is at least very small.

Next we consider a PLL circuit used for synchronous demodulation of AM signals.

Figure 2.2 shows the relevant signals. The upper trace is the modulating signal. It is scaled such that it is within the range from -1 to 1 . The middle trace is the carrier signal $c(t)$. The modulated signal U_1 is given by

$$u_1 = c(t)(1 + m u_m(t))$$

with m = modulation index. m must be chosen $m < 1$, a commonly used value is $m = 0.3$. In this case, the modulated signal u_1 (lower trace) is always in-phase with the carrier $c(t)$. If m were chosen larger than 1, U_1 could be in antiphase with the carrier when the modulating signal has large negative values. When the modulated signal u_1 is now applied to the input of a PLL, the output signal U_2 of the VCO would correctly lock onto that signal, i.e., there would always be a phase difference of 90° between u_1 and u_2 . Figure 2.3 shows the block diagram of a PLL designed for synchronous demodulation of the amplitude modulated signal.

Four blocks have been added to the basic circuit of Fig. 2.1, a 90° phase shifter, a multiplier (MUL), a lowpass filter (LPF), and a highpass filter (HPF). As we have seen, there is a phase difference of 90° between U_1 and U_2 when the PLL has locked. When U_2 is shifted by 90° , the shifted signal $U_{2,\text{shift}}$ is exactly in-phase with the modulated carrier U_1 . With the definitions

$$\begin{aligned} u_1 &= U_{10} \sin(\omega_1 + \theta_1)(1 + m u_m) \\ u_{2,\text{shift}} &= U_{20} \sin(\omega_1 + \theta_1) \end{aligned}$$

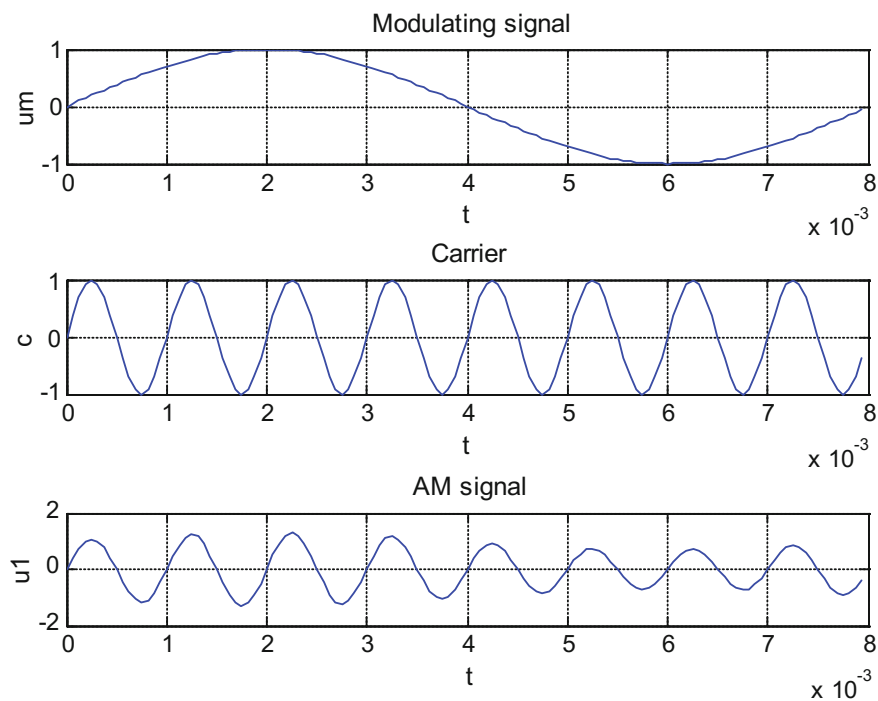


Fig. 2.2 Double sideband AM with carrier. Upper trace: modulating signal U_m , middle trace: carrier c , lower trace: modulated signal U_1

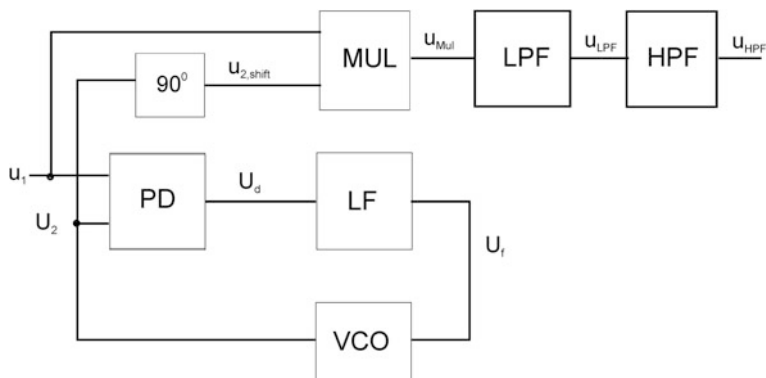


Fig. 2.3 PLL used for synchronous demodulation of AM signal

the output signal of the multiplier U_{Mul} becomes

$$\begin{aligned} u_{Mul} &= U_{10}U_{20}(1 + m u_m) \sin^2(\omega_1 t + \theta_1) \\ &= U_{10}U_{20}(1 + m u_m) \left[\frac{1}{2} - \frac{1}{2} \cos(2\omega_1 t + 2\theta_1) \right] \end{aligned}$$

We recognize that U_{Mul} contains a high-frequency term centered at twice the center radian frequency ω_1 . This term is removed from the lowpass filter; hence, its output signal is given by

$$u_{LPF} = \frac{U_{10}U_{20}}{2} (1 + m u_m)$$

This signal contains a dc term $U_{10}U_{20}/2$. This can be removed if required by a highpass filter. The output of the highpass filter is then

$$u_{HPF} = \frac{U_{10}U_{20}m}{2} u_m$$

which is identical with the modulating signal scaled by a factor $U_{10}U_{20} m/2$.

Whereas the PLL can be successfully used for the synchronous demodulation of double sideband AM signals with carrier, it fails when it comes to demodulated AM signals with suppressed carriers. The waveforms of such an AM signal are shown in Fig. 2.4.

First trace: modulating signal U_m . Second trace: carrier $c(t)$. Third trace: modulated signal U_1 . Fourth trace: reconstructed carrier $U_{2,shift}$.

The modulated signal U_1 is given here by

$$u_1 = u_m \sin(\omega_1 t)$$

When U_m is positive (cf. time interval from 0...4 ms), U_1 is in-phase with the carrier. When U_m becomes negative, however, the U_1 is in antiphase with the carrier (cf. time interval from 4...8 ms). When U_1 is applied now to the input of a PLL, this circuit would track the phase of the VCO output signal U_2 to the phase of U_1 . The shifted signal $U_{2,shifted}$ would be in-phase with U_1 when U_m is positive, but after a transient in the interval 4...5 ms, it would lock in antiphase with the carrier $c(t)$. If the circuit in Fig. 2.3 were used to demodulate the AM signal, the output signal U_{Mul} would have wrong polarity during the intervals where U_m is negative.

There is another application where the PLL fails for the same reason: Binary Phase Shift Keying (BPSK). The signals are similar to those in the previous example, as shown in Fig. 2.5.

The same happens as in the previous example. Because the polarity of the BPSK signal is reversed when the binary signal becomes negative, the reconstructed carrier $U_{2,shift}$ is in antiphase with the carrier $c(t)$, when the modulating signal U_m is negative.

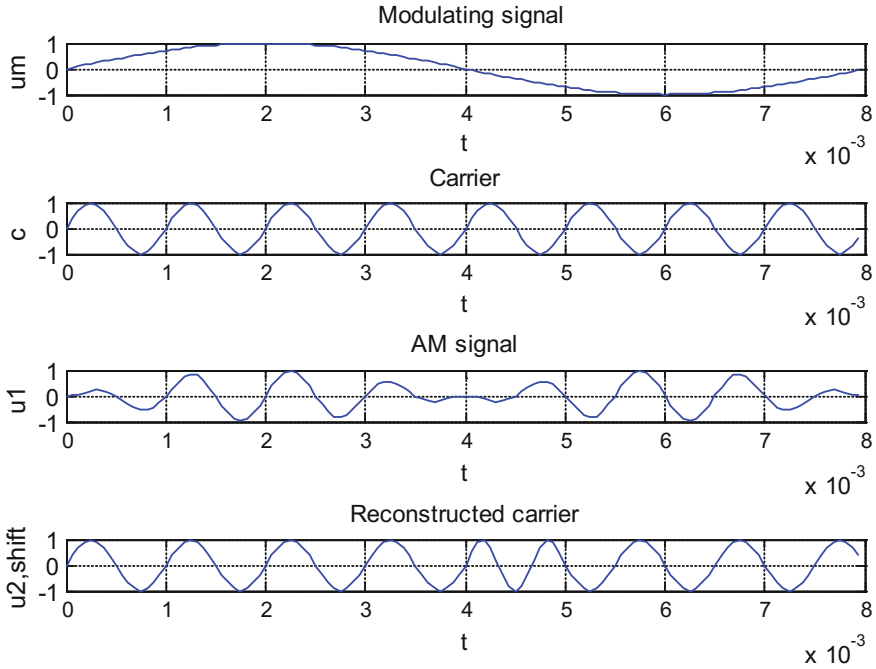


Fig. 2.4 Waveforms of a double sideband AM signal with suppressed carrier

Here the Costas loop comes into play [3]. Figure 2.6 shows the block diagram of the conventional Costas loop for BPSK. Compared with the PLL, this novel circuit consists of two branches, the I branch and the Q branch, whereas the PLL has only one. The input signal is given by $U_1 = m(t) \sin(\omega_1 t + \theta_1)$, where m is the data signal and can take two values, $+c$ or $-c$, where c is a constant. In many cases, $c = 1$ is chosen. When the currently transmitted bit is a logical one, $m = +c$, and when the currently transmitted bit is a logical zero, $m = -c$. The voltage-controlled oscillator in this circuit has two outputs that differ by 90° in-phase, i.e., a sine output and a cosine output. The input signal is multiplied by the sine wave in the I branch, and it is multiplied by the cosine wave in the Q branch. Consequently, the output of the multiplier in the I branch becomes $m(t) \sin(\omega_1 t + \theta_1) 2 \sin(\omega_1 t + \theta_2)$. This signal contains a high-frequency term whose frequency is centered around $2\omega_1$. This term is removed by lowpass filter LPF1, and the output signal of this filter becomes $m(t) \cos(\theta_1 - \theta_2) = m(t) \cos \theta_e$, where θ_e is the phase error. In analogy, the output signal of lowpass filter LPF2 becomes $m(t) \sin \theta_e$. Now the output signals of both lowpass filters are multiplied; hence, the output signal of multiplier MUL is

$$u_d = \frac{m^2}{2} \sin(2\theta_e)$$

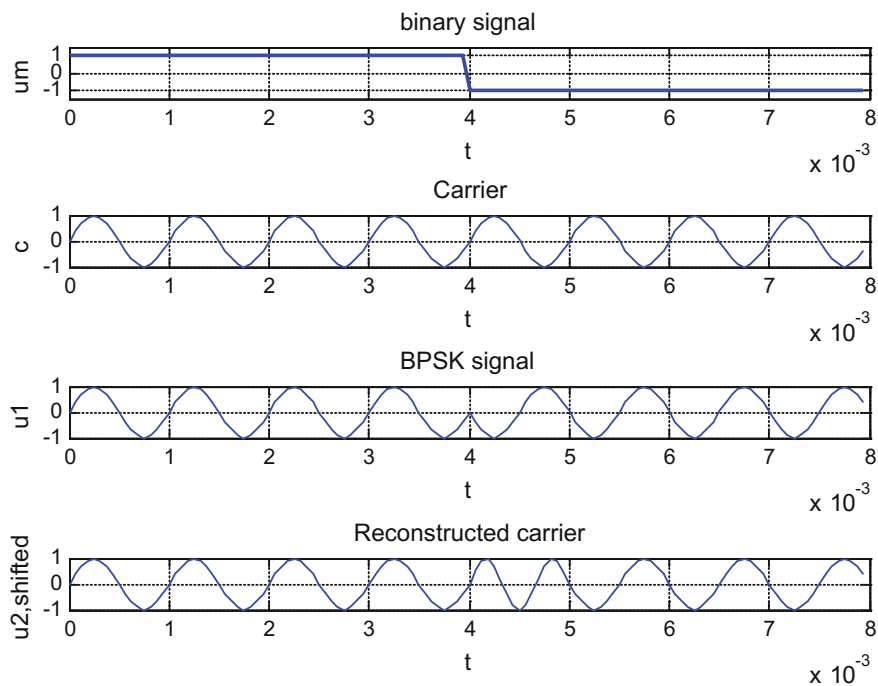


Fig. 2.5 Waveforms for BPSK. First trace: binary signal u_m . Second trace: carrier $c(t)$. Third trace: BPSK signal u_1 . Fourth trace: reconstructed carrier $U_{2,\text{shift}}$, shifted by 90°

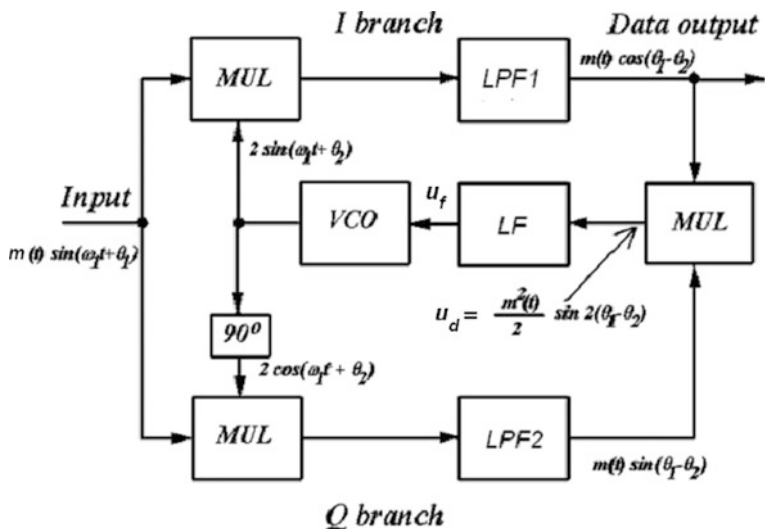


Fig. 2.6 Block diagram of Costas loop for BPSK

When the phase error is small, this can be written

$$u_d = m^2 \theta_e$$

i.e., the multiplier represents a phase detector having detector gain

$$K_d = m^2$$

We recognize that the output signal u_d of the phase detector does not depend on the polarity of signal m , due to the factor m^2 . Thus, the phase detector output signal does not change polarity when m changes from positive to negative values and vice versa. The output signal u_d of the multiplier (phase detector) is applied to the input of the loop filter LF. This filter is always realized as a lowpass filter. Two kinds of loop filters are in use, the lag-lead filter and the PI filter (proportional and integral filter) [2, 4]. When there is a phase error θ_e , the output signal of the loop filter controls the frequency of the VCO such that the phase error is reduced to zero or to a very small value. When the phase error has been reduced to zero or near zero, the output signal of lowpass filter LPF1 is identical with the data signal $m(t)$.

We have seen that the Costas loop can adjust the frequency and phase of the VCO such loop locks with a phase difference $\theta_1 - \theta_2$ near zero. It should be noted that the Costas loop can also lock with a phase difference $\theta_1 - \theta_2$ of π . Assume for the moment that $\theta_1 - \theta_2$ has not yet attained the value π , but is near π . We then can set

$$\theta_1 - \theta_2 = \pi + \theta_e$$

Under this condition, the output signal of LPF1 becomes $m(t) \cos(\theta_1 - \theta_2) = -m(t) \cos \theta_e$, and the output signal of LPF2 becomes $-m(t) \sin \theta_e$. The output signal of the multiplier then becomes again

$$u_d = m^2 \theta_e$$

Here again, when there exists a phase error, the frequency of the VCO will be adjusted such that the loop stably locks with a phase difference $\theta_1 - \theta_2 = \pi$. We can conclude therefore that the Costas loop can lock at two different points of equilibrium, i.e., with $\theta_1 - \theta_2 = 0$ or with $\theta_1 - \theta_2 = \pi$. When the loop locks with a phase difference of π , the output signal of lowpass filter LPF1 becomes $-m$, i.e., its polarity gets inverted.

This is not necessarily a problem, because in many cases differential encoding is used with BPSK [5]. With standard—i.e., not differential—encoding the value of the currently transmitted bit depends only on the polarity of signal $m(t)$. The Costas loop can decide that a transmitted bit is a logical 1 when m is positive or a logical 0 when m is negative. When differential encoding is applied, the value of the currently transmitted bit depends from two values, i.e., from the polarity of the current bit and the polarity of the previously transmitted bit. We define, for example, that

the currently transmitted bit is a logical 1 when current and previous bit have opposite polarity, and that the value of that bit is a logical 0 when these two samples have the same polarity. Under this condition, the Costas loop can lock onto any of the two equilibrium states.

Non-differential encoding can be used when the Costas loop can be brought to lock a priori with the “correct” phase difference of 0. Assume that a transmitter starts to send a series of binary data, e.g., a series of 256 bits. To obtain correct locking, a preamble is preceding the data block, e.g., a series of 16 logical 1’s. The Costas loop must now be equipped with an initialization circuit that becomes active at start of data transmission. Because the Costas loop “knows” the correct value of the first received bits, the initialization circuit can control the VCO such that false locking (i.e., locking with a phase difference of π is prevented). In Sect. 5.6, an example of a Costas loop using such a preamble is presented.

References

1. De Belleszice H., La Reception Synchrone, L’onde électrique, **11**, 225–240 (1932)
2. E. Roland, *Best, phase-locked loops, design, simulation, and applications*, 6th edn. (McGraw-Hill, New York, 2007)
3. J.P. Costas, Synchronous communications. Proc. IRE. 1713–1718 (1956)
4. U. Rohde, J. Whitacker, *Communications receivers* (Software Radios, and Design, McGraw-Hill, DSP, 2001)
5. B. Sklar, *Digital communications, fundamentals and applications* (Prentice Hall, USA, 1988)

Costas Loops

Theory, Design, and Simulation

Best, R.

2018, XI, 155 p. 85 illus., 4 illus. in color., Hardcover

ISBN: 978-3-319-72007-4