

# Preface

Real-time modelling and processing is an active research field in both academia and industrial domains. Communication systems operating in various application domains from automotive industry to telecommunications, health, e-commerce, surveillance, etc., are dependent on the communication of various integrated components. For the desired results, these integrated components and devices must work in bounded time to deliver guaranteed quality in a cost-effective and computational efficient way. Therefore, the development of such system must follow an adaptive, reflexive, intelligent, and fast reconfigurable modelling design. In addition, these systems form a heterogeneous ecosystem of systems in which the implementation and realization of real-time practices become a challenging task and raise numerous scientific and technological issues. Going beyond the existing conventional real-time systems, major efforts are required to propose accurate and computational efficient real-time modelling algorithms and design automation tools that covers technological progress in advanced high-speed and ultra-low-power transceiver communication architectures based on nanoscale devices challenges along with practical implementation and validation scenarios of the real-world design application. These real-time models consider the system nonlinear dynamics going through the characterization, formulation, extraction, and implementation in order to evaluate performance parameters and deliver the expected quality based on deterministic and statistical (variability) analysis.

Understanding the importance of modelling and processing in various research fields, this book presents contents and significant results that provide the essential models, methodologies, and algorithms for designing and implementing such practices. The contents of the book are very consistent, starting from the overview of basic concepts to the more technical aspects of modelling and processing. One of the distinctive aspects of this book is the presentation of work considering the real-time modelling and processing in various domains. This book can contribute to enhance the knowledge of readers especially researchers, engineers, and students working in this field. The gradual and interlinked organization of the chapters will enable readers to rapidly grasp the concepts and enhance their knowledge related to modelling and processing for communication systems. Therefore, in this book, we

cover the most recent real-time modelling and processing research in the design and development of communication systems active in various application domains.

A concise overview of each chapter can be presented as follows. Chapter “[Real Time Modelling and Processing](#)” presents the introduction, motivation, and application of the real-time modelling and processing requirements by exploring the fundamental and perspectives concepts of the real-time processing challenges. The workflow of a computationally efficient and accurate real-time modelling algorithm is presented and analyzed for both computer large scale electronic device, real-time simulations and when the algorithm is embedded in a hardware platform where the CPU and memory resources need to be carefully considered. The advantages and real-time processing applications of the future neurocomputation or processing in memory, enabled by the recent research on memristive nanoscale devices that eliminate the gap between the memory and processing unit, are presented. Moreover, the requirements and the challenges for generating a high-level abstraction modelling algorithms that balance the trade-offs between computational complexity and predictive accuracy are described and discussed for electronic device, real-time computer simulation, control, and automation.

Chapter “[IBIS and Mpilog Modelling Frameworks for Signal Integrity Simulation](#)” presents the structure of the modern integrated circuits (IC) and the necessity of the I/O buffers circuit for ensuring reliable chip-to-chip communication in high-speed digital communication I/O links. Nonlinear circuit simulation based on dc and transient analysis is discussed in order to properly figure out the importance of these algorithms by addressing their convergence issue and computational cost for signal integrity simulation. Moreover, the nonlinear dynamic intrinsic and extrinsic characteristics of the I/O buffers circuit are identified and analyzed. Moreover, this chapter describes IBIS and Mpilog modelling algorithms at circuit level and explains the reason behind the adoption of these modelling tools at different computer-aided design (CAD) tools and design houses as opposed to the SPICE transistor level models in the simulation of printed circuit board (PCB) performance for signal and power integrity simulation. The different design steps of the system identification framework are detailed in the context of accurately capturing the nonlinear dynamic behavior of the I/O buffers electrical circuit. With the aim of analyzing the origins of behavioral modelling developed for output buffer/driver to capture its nonlinear and memory effects and in a way to establish a link with their modelling approaches through large-signal equivalent circuit model and parametric curve fitting techniques, a comprehensive overview of the mathematical modelling framework based on system identification theory is presented in this chapter. For sake of simplicity, the methodology is firstly described for one-port active devices. Then, it is extended to two ports covering the black-box and the gray-box formulations and identification for modelling the driver’s nonlinear dynamic behaviors where the state-of-the-art input/output buffer information specification (IBIS) and parametric modelling are analyzed and discussed.

Chapter “[Improved and Reduced-Order I/O Devices Behavioral Modeling Solutions for SI Simulation](#)” presents the parametric and equivalent circuit solutions for improving the I/O buffer behavioral modelling. The previously neglected

driver's nonlinear dynamic effects are efficiently captured to significantly reduce the state-of-the-art black-box parametric modelling complexities and enhance the input/output buffers information specifications (IBIS). This is achieved by following the gray-box approach that merges the features of the black-box model's formulation and the analysis of the observed I/O electrical signals and the analysis of the buffer's physical structure properties under practical operation conditions. This approach leads to physically inspired behavioral model's construction procedure that overcomes the issues of the previous modelling approaches by optimizing the resources used at different model's generation steps (i.e., characterization, formulation, extraction, and implementation) to mimic the driver's nonlinear dynamic behavior. In the conceived parametric solution, the output current relationship with the output voltage is expressed as a summation of a static nonlinearity plus linear dynamics. This separation in the model format is supported by both measurements and the physical structure of a general driver circuit. This approach merges the features of equivalent circuit and the parametric approaches to build a reduced-order parametric behavioral model which, compared to other published models, is more adequate to describe the device's electrical behavior from transient input–output data. Furthermore, an efficient and accurate table-based behavioral model extraction for high-speed input/output buffer behavior is presented in this work. The nonlinear voltage–current ( $I$ – $V$ ) and voltage–charge ( $Q$ – $V$ ) functions describing the gray-box model structure are extracted via the bias-dependent  $S$ -parameters frequency domain measurements or the least squares methods using identification signals recorded from large-signal transient simulation. Finally, the development of a new two-port analog behavioral model for over-clocking simulation that copes with the recent trends in I/O memory interfaces characterized by higher data rate transmission is proposed. The effectiveness and the accuracy of the developed and implemented parametric and equivalent circuit behavioral models are qualitatively and quantitatively assessed by comparing the numerical results of their functions extraction and transient simulation to the ones simulated and extracted with transistor level models and the state-of-the-art IBIS in order to validate their predictive and the generalization capabilities.

Chapter “[Neuro-Fuzzy Nonlinear Dynamic Modelling for Signal Integrity Simulation](#)” presents a multiport empirical model for I/O memory interface (e.g., inverter) designed based on fully depleted silicon on isolator (FDSOI) CMOS 28 nm process for signal and power integrity assessments. The analog mixed-signal identification signals that carry the information about I/O interface are recorded from large-signal simulation setup. The model's functions are extracted based on a nonlinear optimization algorithm and then implemented in Simulink software. The performance of the resulted model is validated in typical power and ground switching noise scenario. The developed empirical model accurately predicts the timing signal waveforms at the power, ground, and at the output port. Moreover, a comparative analysis between the artificial neural networks (ANNs) and adaptive neuro-fuzzy inference (ANFIS) models by exploring their modelling capabilities regarding the mathematical structures and identification algorithms in providing an accurate and computational effective behavioral model for the I/O buffers nonlinear

dynamic behavior is investigated. The proposed model of the two-port I/O buffer is extracted from observable large-signal I/O current and voltages transient data. The training and computational performances along with the prediction accuracy of both modelling approaches are evaluated. The ANFIS model has better prediction accuracy by improving the normalized mean squared error (NMES) by  $-13.5$  dB while reducing by 11.66% the parameters' number in cross-validation signal integrity scenario.

Chapter “[Fuzzy Sliding Mode Controller Design Based on Euclidean Particle Swarm Optimization](#)” presents a new design of fuzzy sliding mode control based on parallel distributed compensator and using Euclidean particle swarm optimization in order to overcome the problem caused by an inappropriate selection of sliding surface parameters. The proposed method employs the parallel distributed compensator scheme to design the state feedback-based control law. The controller gains are determined in offline mode via a linear quadratic regular. The Euclidean particle swarm optimization is incorporated into the linear quadratic regular technique for determining the optimal weight matrices. Consequently, an optimal sliding surface is obtained. This latter is used to design the proposed control law. Finally, several tests have been done to examine the performance and applicability of the proposed method in real world.

The development of electrothermal models of power semiconductor devices is of great importance in the design of power systems, operating under extreme temperature conditions like applications dedicated to the exploitation of petroleum or geothermal resources. Thereby, the electrothermal behavior of power devices which risks altering their electrical characteristics especially for high operating temperatures should be thus studied. Therefore, in Chapter “[An Electrothermal Behavior Study of the Power PiN Diode](#)”, an electrothermal study of the Power PiN diode is performed. Indeed, the self-heating effects inside the PiN diode structure as well as the influence of the variation of the internal temperature on their electrical characteristics are highlighted. It is also demonstrated that the temperature distribution inside the PiN diode structure, operating under self-heating conditions, is not uniform. This fact should be mandatory considered for the development of electrothermal analytical models of power devices. The effects of the increase of the PiN diode operating temperature on their transient characteristics during their turnoff phase are studied, and finally, the electrothermal losses dissipated by these devices during their turnoff transient are analyzed as a function of the operating temperature.

In Chapter “[A Detailed Extraction Procedure of Thyristor Design Parameters](#)”, through a study considering an experimental circuit of a switching cell including a Thyristor under test controlled by a MOSFET transistor, it is checked that a simple wiring inductance as the circuit wiring representation is insufficient to obtain accurate simulation results. Therefore, a suitable wiring model of the switching cell circuit is developed taking into account the wiring parasitic inductances of the layout and the mutual effects between them. Then, using the accurate model of the switching cell circuit, a detailed extraction procedure of the Thyristor design parameters is developed. This extraction procedure is based on a comparative study

between experimental and simulated results, considering the physics of component. Finally, a good agreement is obtained between experimental and simulated results confirming the validity of the developed extraction procedure as well as the suitable wiring model of the switching cell circuit.

Chapter “[Modeling of Memristive Devices for Neuromorphic Application](#)” presents the physical mechanism analysis and the compact behavioral modelling of the titanium oxide, ferroelectric tunnel junctions, and phase change materials memristive devices. The memristive devices mathematical theoretical model’s derivation and physics-based model structure representations along with their resistive switching mechanisms are analyzed, implemented, and validated. The accuracy of the implemented Verilog-A models of the considered memristive devices is assessed in a synaptic transmission through spike-timing-dependent plasticity. Moreover, the key properties and performances of these three memristors technologies are discussed in order to classify them and study their adequacy for their adoption to artificially imitate synaptic functionality in neuromorphic applications.

Chapter “[Modeling, Designing and Analyzing Resource Reservations in Distributed Embedded Systems](#)” comprehensively presents a study about the resource reservation modelling for distributed embedded systems. Distributed embedded systems in many domains are becoming highly complex, mostly due to ever-increasing demand for advanced computer controlled functionality. These systems are realized by several embedded systems communicating through network channels. These systems are often required to be predictable, i.e., their responses to internal or external stimuli should be delivered within the constraints that are specified on them. Compositional development methods have been proposed by the research community to lower the software complexity, ensure predictability, and allow flexibility during the development and execution of these systems. According to these methods, the computation and communication resources are allocated to each part (or sub-system) of the system, which in turn brings isolation among the parts and eases the system integration. This chapter presents a new end-to-end resource reservation model for distributed embedded systems that covers not only the computational nodes but also the communication channels. Moreover, timing analysis is presented to verify the predictability of the systems. This chapter also describes guidelines to distribute resources efficiently among different parts of the system. As a proof of concept, the end-to-end resource reservation model is implemented in the Rubus Component Model. This component model is already used for the development of control functionalities in vehicular embedded systems by several international companies. In order to show the usability of the proposed model, reservation design method, end-to-end timing analysis, and extended component model, a vehicular application case study is conducted and several experiments are performed.

Chapter “[Real-Time Implementation of Light-Independent Traffic Sign Recognition Approach](#)” presents the real-time implementation of light-independent traffic sign recognition modelling. Computer vision for driving assistance offered significant progress in road sign detection, but still needs great improvements because

of difficulties associated with extreme variations in lighting conditions. When poor lighting conditions are met, the driver must be alerted when a road sign is encountered. This is feasible through an automatic system equipped with a camera on the dashboard of the vehicle, capable of detecting the road sign and alarming the driver. This chapter's main objective is the development of an adequate and robust Traffic Signs Recognition system functioning independently of lighting situations. A three-task approach is proposed; it is mainly composed of object detection, shape classification, and content classification. The detection phase is based on the RGB-color space segmentation with an empirically determined threshold. It extracts the relevant red and blue regions in the image with limit values of Bounding Boxes (BB). After object extraction, the sign's shape is classified by an artificial neural network (ANN). The classified circular and triangular shapes are passed on to the second ANN in the third phase. These identify the pictogram of the road sign. The output of the second ANN allows the full recognition of the traffic sign. The proposed algorithm and its performance was tested in real driving scenarios under realistic weather conditions. Moreover, a design of a novel embedded ADAS system is presented. The system can detect and recognize road signs even in critical weather conditions and at different luminosity situations. The proposed system allows real-time detection in high-resolution images. Probable sign candidates are extracted by means of the maximally stable external regions (MSER) technique. Each candidate is examined by the recognizing process in order to accept or to reject the sign and can be executed according to a local database.

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