Chapter 2
Fundamentals of Electromigration

Having shown in Chap. 1 that the future development of microelectronics will lead to more and more electromigration problems, let us now investigate in detail the actual low-level migration processes. A solid grounding in the physics of electromigration (EM) and its specific effects on the interconnect will give us the knowledge to establish effective mitigation methods during the design of integrated circuits (ICs).

We first explain the physical causes of EM (Sect. 2.1) and then present options to quantify the EM process (Sect. 2.2), which enable us to effectively characterize key aspects of the process and its effects. In Sect. 2.3, we introduce EM-influencing factors arising from the specific circuit technology, the environment, and the design. We then investigate detailed EM mechanisms with regard to circuit materials, frequencies, and mechanical stresses (Sect. 2.4).

Since EM is closely related to other migration processes, such as thermal and stress migration that also occur in the conductors of electronic circuits, we examine their interdependencies (Sect. 2.5). IC designers must be especially aware of thermal and stress migration; both are introduced and described in their interaction with EM.

Finally, Sect. 2.6 outlines the principles of a migration analysis through simulation. This honors the importance of finite element modeling (using the finite element method, FEM) in electromigration analysis and enables the reader to develop and apply similar modeling and simulation techniques.

2.1 Introduction

The reliability of electronic systems is a central concern for developers, which is addressed by a variety of design measures that include, among others, the choice of materials to best suit an intended use. As the structural dimensions of electronic interconnects are downscaled (Chap. 1), new factors that reduce reliability and that

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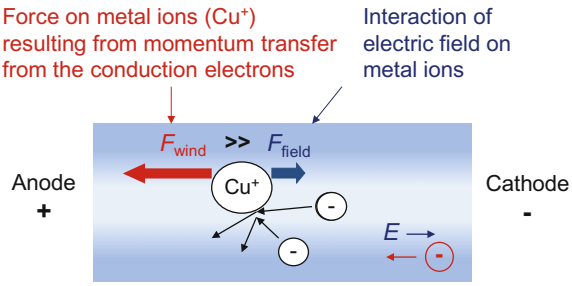

Fig. 2.1 Two forces act on metal ions (Cu) that make up the lattice of the interconnect material. Electromigration is the result of the dominant force, that is, the momentum transfer from the electrons that move in the applied electric field E

previously could be ignored now come to bear. In particular, material migration processes that occur in electrical interconnects during IC operation can no longer be ignored during IC design and development.

Material migration is a general term that describes various forced material transport processes in solid bodies. These include (1) chemical diffusion due to concentration gradients, (2) material migration caused by temperature gradients, (3) material migration caused by mechanical stress, and (4) material migration caused by an electrical field. This last case is often referred to as *electromigration*, which is the subject of this chapter (and the book); we describe its relationship to the other migration processes (1)–(3) in Sect. 2.5.

Current flow through a conductor produces two forces to which the individual metal ions[1] in the conductor are exposed, the first of which is an electrostatic force F_{field} caused by the electric field strength in the metallic interconnect. Since the positive metal ions are shielded to some extent by the negative electrons in the conductor, this force can safely be ignored in most cases. The second force F_{wind} is generated by the momentum transfer between conduction electrons and metal ions in the crystal lattice. This force, which one may visualize by analogy as a breeze or wind blowing through the leaves of a tree, acts in the direction of the current flow and is the primary cause of electromigration (Fig. 2.1).

If the resulting force in the direction of the electron wind (which also corresponds to the energy transmitted to the ions) exceeds a given trigger known as the activation energy E_a, a directed diffusion process starts. (In our earlier analogy, a leaf has been blown off the tree by the wind.) The resulting material transport takes place in the direction of the electron motion, that is, from the cathode (-) to the anode (+).

[1]The crystal lattice of metals is built up of ordered metal ions with an "electron fog" in-between, consisting of shared free electrons. The terms metal *atoms* and metal *ions* are considered equivalent in this context.

The actual diffusion paths are material dependent and are mainly determined by the size of their respective activation energies. Every material has multiple, different activation energies for diffusion, namely for diffusion (i) within the crystal, (ii) along grain boundaries, and (iii) on surfaces (Sect. 2.3.1). The relationships between the individual energy levels determine which of the diffusion mechanisms (i)–(iii) dominates, as well as the composition of the entire diffusion flux.

If one could assume the material transport was homogeneous at every location in the wiring, there would be no change throughout the interconnect: the same amount of material would be replenished as would be removed. However, the wiring of a fabricated IC chip contains numerous required features that result in inhomogeneities; as a result, the diffusion is also inhomogeneous. Among the features and resulting inhomogeneities encountered in chip designs are

- ends of interconnects,
- changes in the direction of interconnects,
- change of layers,
- varying current densities due to changes in interconnect cross-sections,
- changes to the lattice or the material,
- already existing damage or manufacturing tolerances,
- varying temperature distributions, and/or
- mechanical tension gradients.

These inhomogeneities cause divergences in the diffusion flow, leading to metal depletion or accumulation in the vicinity of such inhomogeneities. Such depletions and accumulations in turn result in damage to the interconnect, due to *voids* and interconnect breaks or *hillocks* that cause short circuits (Fig. 2.2). Another result of EM in wires is *whiskering*, which is a crystalline metallurgical phenomenon involving the spontaneous growth of tiny, filiform hairs from a metallic surface (see Fig. 2.2, right). *Whiskers* can cause short circuits and arcing in electronic circuits.

The two types of depletion that cause damage in integrated circuits are known as *line depletion* and *via depletion* (Fig. 2.3). Electron flow from a via to a line can

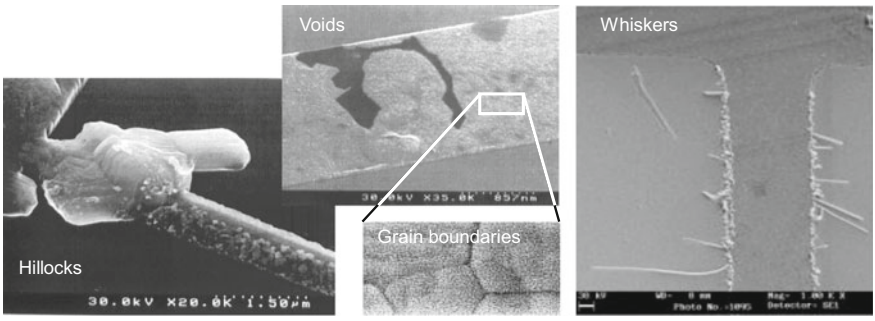

Fig. 2.2 Hillock and void formations in wires due to electromigration (*left*, photographs courtesy of G. H. Bernstein und R. Frankovic, University of Notre Dame). Whisker growth on a conductor is shown on the *right*

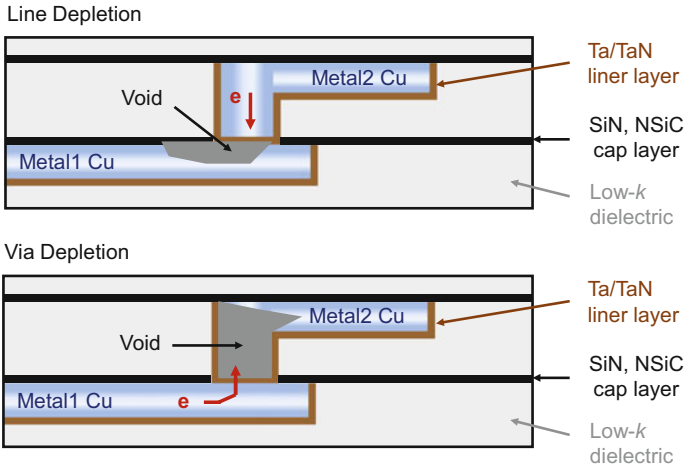

Fig. 2.3 Line depletion (*above*) and via depletion (*below*) are common failure mechanisms due to EM in integrated circuits

cause line depletion due to obstructed material flow through the cap and liner layers. Reversing the electron flow, i.e., electron flow from a line to a via, may result in via depletion, sometimes also called *via voiding*. Here too, its causes are a combination of geometry and process. As with line depletion, the material migration is hindered by the surrounding cap and liner layers. In addition, as the ratio of the line width to the via width increases, the via must carry more current for the same line current density, making the via more susceptible to the voiding process.

EM-induced damage to an IC that results from the growth of voids is further accelerated by a positive feedback loop (Fig. 2.4). Here, an initial (excessive) current density causes void growth and cross-sectional degradation, which increases the local current density. At the same time, the (increasing) current density causes a temperature rise due to (local) *Joule heating*, which occurs when an electric current passes through a conductor and produces heat. The increased heat also accelerates diffusion and thus further increases the void growth.

It is important to note that EM is only one of four different migration processes that occur in solid-state materials such as the wires on an electronic circuit. As shown in Fig. 2.5, the other processes are *chemical diffusion*, *thermal migration*, and *stress migration*, which are caused by the chemical and thermal gradients and mechanical stress, respectively. While we will consider their mutual interaction and influence on EM in Sect. 2.5, this book primarily focuses on solid-state electromigration.

In addition to the solid-state electromigration process, so-called *electrolytic electromigration* can occur in electronic circuits, often on printed circuit boards (PCBs). Its mechanisms are quite different compared to solid-state electromigration: recall that solid-state electromigration is the movement of metal within a conductive

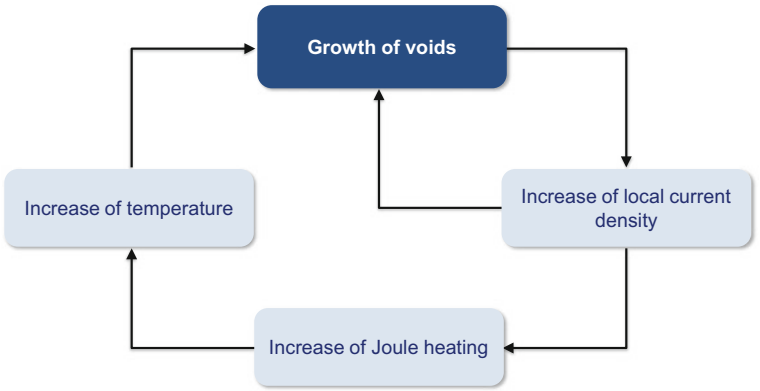

Fig. 2.4 Acceleration of the growth of voids by positive feedback at work: void growth increases current density, which in turn rises the wire's temperature due to Joule heating, which further accelerates diffusion and void growth

path due to electron momentum transfer (scattering) resulting from high current densities (>10^4 A/cm^2), often at higher temperatures. In contrast, electrolytic electromigration is the movement of metal across a nonconductive path at lower temperatures (<100 °C) and at low current densities (>10^{-3} A/cm^2) in the presence of moisture.

Electrolytic electromigration requires moisture on the surface and a high electric field, often caused by a combination of voltage difference and narrow line spacing in a wet environment. Migrating metal ions are dissolved in an aqueous solution (e.g., water) in this process. The material flows in a direction opposite to solid-state electromigration: a DC electric field between the anode and cathode will pull the

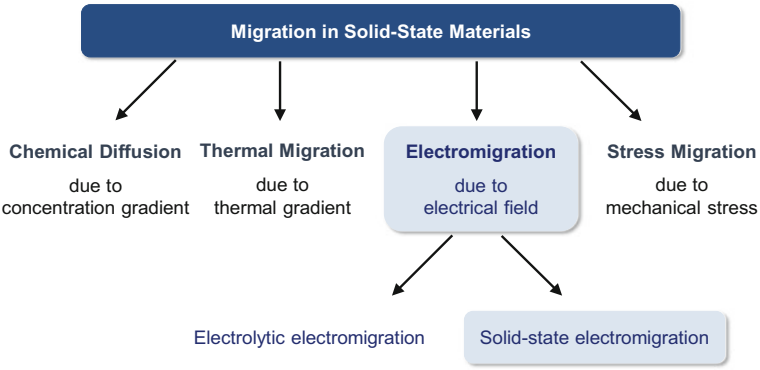

Fig. 2.5 Different migration mechanisms can occur in electronic circuits. While this book focuses on (solid-state) electromigration, their mutual interactions cannot be neglected and are covered in Sect. 2.5

free metal ions across to the cathode; hence, migration follows the direction of the electric field.

Since electrolytic electromigration can easily be avoided (by keeping the electronic circuit dry) and is visually recognizable on PCBs (tree-like structures of crystals, so-called dendrites, that traverse conductor spacing), it will not be covered further in this book.

2.2 Electromigration Quantification Options

A diffusion formula (see Sect. 2.4.1, Eq. 2.2) may be used for a detailed, quantitative analysis of the EM process, with the ultimate aim of determining the divergence in the material flow. This type of analysis yields the locations that have material accumulation and depletion, and identifies locations where initial damage is expected to occur. Such a quantitative approach also helps to obtain the mean service life duration of the interconnect.

While this analytical approach is sound from a theoretical basis, such extensive calculations are practical only in simple cases. Typically, many iterations and numerical analyses are required to determine the service life duration for even the simplest of cases. The same applies to short-term calculations for more complex architectures. As analytical solutions are often too time consuming and impractical, a numerical simulation may be necessary, even for a single change in direction or cross-section of the wire.

Fortunately, there is an empirical model for determining the *median time to failure* (MTF) for simple linear interconnects. This reliability characteristic is described by *Black's equation*, first introduced by J. R. Black in the 1960s [Bl69a], as follows:

$$\mathrm{MTF} = \frac{A}{j^2} \cdot \exp\left(\frac{E_\mathrm{a}}{k \cdot T}\right) \tag{2.1}$$

where A is a cross-section-dependent constant, that, among others, relates the rate of mass transport with median time to failure (MTF) [Bl69b], j is the current density, E_a is the activation energy, k is the Boltzmann constant[2], and T is the temperature.

In later variants of Eq. (2.1), the constant exponent ("2") of the current density j has been replaced by a variable n to allow the model to be applied to different types of dominant failure mechanisms. In effect, this meant different exponents were used for different interconnect materials, for example aluminum (Al) and copper (Cu). Furthermore, it has been established through studies on Al and Cu interconnects (e.g., [Hau04]) that void-growth-limited failure is characterized by $n = 1$, while void-nucleation-limited failure is best represented by $n = 2$.

[2]The Boltzmann constant, which is named after Ludwig Boltzmann (1844–1906), is a physical constant relating the average kinetic energy of particles with the temperature.

In the case of aluminum and its associated dominant grain-boundary diffusion, the activation energy E_a is approximately 0.7 eV for a current-density exponent of $n = 2$. Copper, by contrast, has the lowest activation energy at 0.9 eV for the dominant surface diffusion with a current-density exponent n between 1.1 and 1.3, depending on the dominant failure mode [FWB+09].

With Black's Eq. (2.1), the relation between service life duration and current and temperature can be readily estimated; the equation yields useful information for accelerated testing, as well. One caveat of the equation is that a steep rise in the current, and thus the current density, alters the failure mechanism—which is not modeled by the equation. Large temperature gradients may then arise as well, due to the characteristic heat increase of the interconnect (Joule heating), which can cause thermal migration (Sect. 2.5) or even thermal failure.

Black's equation is useful to a certain extent when designing interconnects for desired reliabilities. The main disadvantage is that the equation is designed for linear interconnects and cannot successfully be applied to entire net routes with changes in direction or changes in layer. Neither does it cover transitions between different materials and mechanical boundary conditions. This limits its usefulness, as the equation cannot therefore be used to compare different technologies. Parameters A and E_a are particularly technology-specific.

In [LT11], Li and Tan developed a different, more complex model for calculating the service life duration, which considered additional constraints, such as thermal and mechanical stress. Their model, which is based on the Eyring equation, contains far more parameters. It is easier to determine these parameters than with Black's equation, as the model is based on material properties and actual transport mechanisms. This is in contrast to Black's equation where the parameters are empirically defined and can be determined only by statistical investigations.

2.3 Design Parameters

EM-related design parameters and constraints can be divided into three groups as they are based on

- the technology, in particular the materials,
- the environment, especially the temperature, and
- the design, which is the main determinant of the current density.

We describe each of these groups in detail below.

2.3.1 Technology

The material used to construct the interconnect has a significant impact on electromigration. The key property of a conductor material is its activation energy E_a,

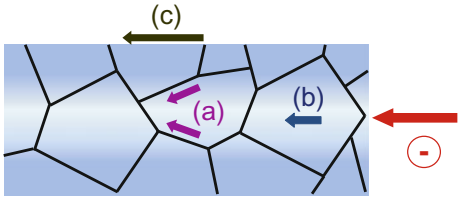

Fig. 2.6 Illustration of various diffusion processes within the lattice of an interconnect: **a** grain-boundary diffusion, **b** bulk diffusion, and **c** surface diffusion

which is a measure of the resistance of the metal ions to EM, as well as its resistance to diffusion in general. The activation energy is primarily determined by the bonding energy of the crystal metal lattice. Hence, its values are different for different interconnect materials, such as copper and aluminum. In addition, the ions in a crystal lattice have different binding energies, depending on their location within the lattice as illustrated in Fig. 2.6 and explained below.

The most stable bond, one having the maximum activation energy, is in the crystallite core. Only ions in this lattice region that are near crystallographic defects, such as voids (vacancy defects) or dislocations, are able to leave their positions. In contrast, ions at the grain boundaries in polycrystalline interconnects have weaker bonds to the lattice and thus have a lower activation energy, because the bonding forces are asymmetric. Similar behavior patterns exist at the external boundaries or surfaces of the interconnect, where the materials in the surroundings have a decisive impact on the activation energy.

In the case of aluminum, grain-boundary diffusion dominates the electromigration process, as the activation energy is lowest at the grain boundaries ($E_a \approx 0.7$ eV, Sect. 2.4.1). EM robustness therefore can be improved significantly for aluminum interconnect by doping with copper, for example, or by nucleating larger grains.

This contrasts with copper, where boundary or surface diffusion dominates ($E_a \approx 0.8$–1.2 eV, Sect. 2.4.1). This explains why at present there is a lot of investment and interest in research for barrier materials, to boost the activation energy.

The interconnect surroundings affect not only the activation energy of the surface diffusion, but also the mechanical constraints. EM can be counteracted and stopped with stress migration, which is initiated by exposing the interconnect to mechanical stress. The dielectric has a greater role to play here than the barrier materials. It is only with sufficiently large mechanical tension gradients that an appreciable stress migration can take place. For this reason, dielectrics with high Young's moduli (i.e., high stiffnesses) produce the best results. The dielectric specified by the technology affects the EM response in this context.

In general, technological restrictions specify constraints for the layout design, which are typically referred to as *design rules*. These design rules result in specific local geometrical configurations that have implications for EM behavior. The

overall design itself has very little impact on these configurations; instead, the technological specifications for the design are typically spacing, overlap, and width rules. There are often other rules as well, for example, for the surface ratios between metal and dielectric for every routing layer. Certain dimensions, such as the coating thickness of individual layers or the size of vias, are also typically specified by the technology.

2.3.2 Environment

We can see from Eq. (2.1) that the key environmental factor regarding electromigration is temperature and, as such, the physical location where the integrated circuit is deployed is critical. Some of the highest temperature standards apply for ICs in automobile electronics, where circuits are typically designed for ambient temperatures up to 175 °C (347 °F). These maximum temperatures can be reached in normal operations, in particular in gasoline engine compartments.

All electronic components and wire interconnects dissipate heat; this *power dissipation* is the difference between the energy supplied to an electrical component and that released during operation. High power losses, which frequently occur in digital circuits such as high-performance microprocessors or analog amplifiers, can cause increased temperature loading. This situation is further exacerbated if high power losses are combined with high ambient temperatures—this increases the likelihood of aging in integrated circuits.

Both of these temperature loads, from power losses and high ambient temperatures, reinforce EM by providing a portion of the activation energy as thermal energy. Furthermore, the diffusion process is accelerated by the increased mobility of ions. Copper is particularly susceptible to temperature changes; for example, if the operating temperature is increased by 10 K, the current needs to be cut by more than 50% to maintain the same median time to failure (service life duration). This critical relation can be derived with copper parameters from Black's Eq. (2.1). On the other hand, a 5 K decrease in operating temperature can lead to about a 25% increase in permissible current density (Fig. 2.7 illustrates this relationship for aluminum wiring).

The characteristic heat increase of the interconnect at high current densities due to Joule heating is another thermal factor that must be considered. As mentioned earlier, Joule heating is caused by interactions between the moving electrons and the metal ions that comprise the body of the conductor. Joule heating also leads to temperature gradients in the interconnect, which can cause thermal migration (Sect. 2.5).

Other environmental factors besides temperature also affect electromigration. For example, different substances can penetrate the metal layer by diffusion and impact the electromigration process. In addition, electrolytic migration (Sect. 2.1) can occur if water comes in contact with the wiring. Furthermore, oxygen also affects the processes by oxidizing the metals. These phenomena introduce major changes to the entire migration process that can rapidly cause severe damage. Such

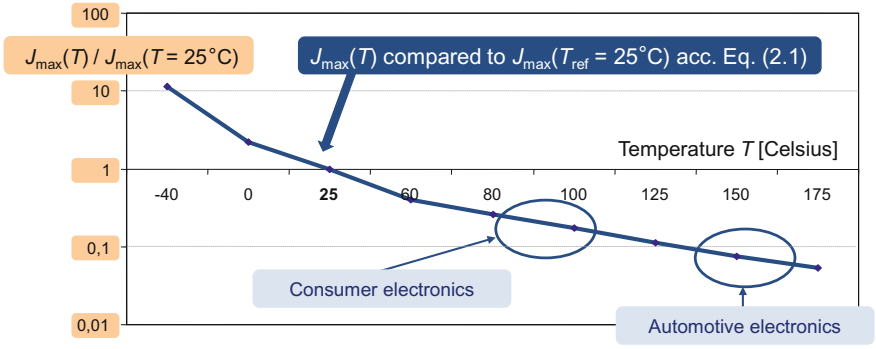

Fig. 2.7 Illustration of the relationship between maximum current density and temperature if the reliability *MTF* of an Al wiring in Eq. (2.1) is kept constant [Lie05, Lie06]. It becomes clear, that, for example, when the working temperature of an Al interconnect is raised from 25 °C (77 °F) to 125 °C (257 °F), the maximum tolerable current density must be reduced by about 90% in order to maintain the same reliability of the wire

environmental effects are not dealt with below as this type of diffusion of foreign substances can be prevented with suitable barriers.

2.3.3 *Design*

The design itself can significantly affect EM by defining the current densities that occur throughout the chip. The current density j, which is represented as the quotient of current and cross-sectional area (Eq. (1.1), Chap. 1), is determined at a specific location by the functional load, i.e., the electrical current I, and by the physical design solution, in particular, the cross-sectional area A of the interconnect at that location. The interconnect must be designed to deliver the currents required by the circuit; thus, the width of each interconnect must be adapted to accommodate the current.

Changes in direction and moving between layers cause local increases in current densities, which in turn compounds EM and leads to an agglomeration of damage (Fig. 2.8). All geometrical structures of the layout design, that is, those not exclusively specified by the technology, can be used to increase the EM-limited service life duration of the wiring, as illustrated in Fig. 2.8 by the use of suitable corner-bend angles.

Other factors that can reduce the impact of EM should be deployed as well, to prevent high local current densities. Service life duration can particularly benefit from limiting the length of the interconnects if the Blech length [Ble76] is leveraged. This is due to mechanical stress migration in interconnects that are less than a critical length, which counteracts EM and prevents damage occurring (Sects. 2.5 and 4.3).

Fig. 2.8 Current-density visualization of different corner-bend angles of a wire on an analog integrated circuit, *left* 90°, *middle* 135°, and *right* 150°. It shows that 90° corner bends must be avoided, since the current density in such a bend is significantly higher than that in oblique angles of, for example, 135°

In addition to current density, the frequency is another quantity arising from the design that impacts interconnect reliability. The change in direction of the current causes a corresponding change in the direction of diffusion, as well, and small (preexisting) damage to the interconnect can be partially cleared. This beneficial process is known as *self-healing* and greatly depends on the frequency of the current (Sects. 2.4.3 and 4.7).

2.4 Electromigration Mechanisms

As stated earlier, the dominant driving force for electromigration damage is due to momentum transfer from the moving electrons to the ions, which leads to a mass flux in the direction of the electron flow. The detailed mechanisms of this flux with regard to circuit materials, frequencies, and mechanical stresses are described next.

2.4.1 Crystal Structures and Diffusion Mechanisms

Interconnects in integrated circuits can have different crystal lattice structures (Fig. 2.9). The most common type of lattice structures in metallic interconnects is polycrystalline, fine-grained structures. Depending on the ratio between grain size and interconnect dimensions, there may also exist—in theory at any rate—polycrystalline interconnects composed of few grains, bamboo-like structures, monocrystals, and amorphous structures. These categories for crystal lattice

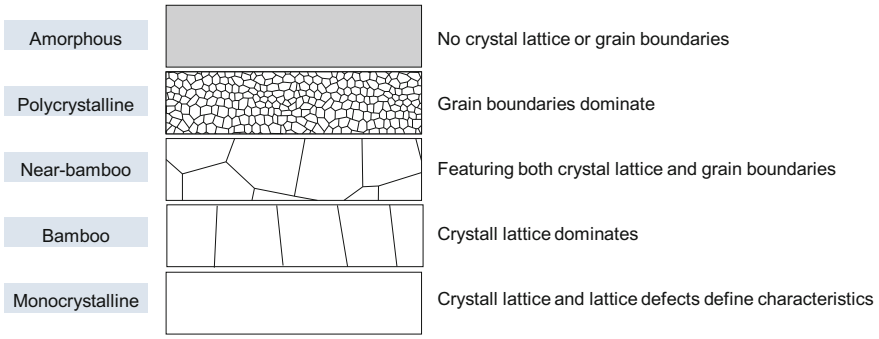

Fig. 2.9 Different crystal lattice structures in metallic interconnects

structures are particularly useful for characterizing the causes and effects of electromigration. We discuss below the properties of these crystal lattice categories.

In amorphous interconnects, atoms are not in ordered structures, but rather are arranged in irregular patterns and hence have a short-range order, rather than a long-range one[3]. There are thus neither grain boundaries nor crystalline zones, and the material has very specific properties. Because there is no long-range order, there are no diffusion channels as in a periodic crystal lattice. In an amorphous lattice, the cohesion and atomic density differ from the crystalline state. In practical terms, we note that metals can only be brought into the amorphous state in extreme conditions, with cooling rates on the order of 10^5–10^6 K/s [SW96]. Such conditions cannot be created for the fabrication of integrated circuits, and thus the use of metal-based amorphous lattices is more of theoretical interest for EM mitigation.

The other extreme, the monocrystalline state, can also only be achieved with massive investment in technology, which too makes it impractical. Typically, the crystal has to be grown from a single germ in the molten mass. This is virtually impossible in an interconnect surrounded by different substances.

All the same, we should not completely rule out the use of monocrystalline lattice structures in the future. A variant of monocrystal growth, which works below the molten temperature, was used in [JT97]. Here, aluminum monocrystals were produced on a monocrystalline sodium chloride layer. Different crystal orientations can also be promoted with this process. This technology, however, is currently only suitable for use in the laboratory and not for IC fabrication, not least because of the unwanted sodium chloride in the semiconductor processes. The other issue with monocrystals is that individual lattice defects can greatly impact interconnect properties. This undermines the required process stability, which is so important for reliability.

[3]Long-range order in a crystal means that atoms are organized in a periodic order across many atoms, such as in a periodic lattice.

For these reasons, the polycrystalline state in interconnects is the norm. There are many different types of polycrystalline lattice structures whose properties differ enormously from an EM perspective. We can consider the bamboo and near-bamboo lattice structures (see Fig. 2.9) as polycrystalline lattice variants, whose diffusion properties are dominated by specific features, as we discuss below. Lattice diffusion (also called volume or bulk diffusion) as well as grain-boundary diffusion can take place in fine-grained polycrystalline microstructures (see Fig. 2.9). Surface diffusion occurs, too, regardless of the lattice; we will deal with this type of diffusion in Sect. 2.4.2.

EM, like all other types of migration, obeys the laws of diffusion. A crystal metal lattice can be modeled in terms of EM with the simplified one-dimensional diffusion formula (also known as heat equation[4]) for homogeneous media, as follows:

$$\frac{\partial c}{\partial t} = D \cdot \frac{\partial^2 c}{\partial x^2}, \tag{2.2}$$

with the concentration c, the time t, the diffusion coefficient D, and the location x. The diffusion velocity v of the atoms, excited by the current density, can be expressed according to [AN91] as:

$$v = \frac{D}{kT} \cdot ez^* \varrho j. \tag{2.3}$$

In this equation, k is Boltzmann constant, T the absolute temperature, e the elementary charge, z^* the effective charge of the metal ion as a measure of the momentum exchange, ϱ the specific electrical resistance, and j the current density [AN91, Ble76].

The diffusion coefficient D expresses the magnitude of the atomic flux. It is a physical constant dependent on atomic size and other properties of the diffusing substance as well as on temperature and pressure. The diffusion coefficient is calculated in the case of the combined grain-boundary and bulk diffusion as follows:

$$D = D_\mathrm{v} + \delta \cdot \frac{D_\mathrm{b}}{d}, \tag{2.4}$$

where D_v is the diffusion coefficient for the bulk (volume) diffusion and D_b the diffusion coefficient for the grain-boundary diffusion. The width of the grain boundaries δ and the mean grain size d must be considered, as well [AN91].

As shown in Table 2.1, different diffusion paths are characterized by different activation energies E_a (see Black's Eq. (2.1)). While the maximum activation energy is needed for bulk diffusion, it is lower for grain-boundary diffusion and surface diffusion. Accordingly, the diffusion coefficient D for bulk diffusion is

[4]The heat equation is a differential equation that describes the distribution of heat (or variation in temperature) in a given region over time.

Table 2.1 Activation energies for different diffusion paths for electromigration in aluminum and copper

Diffusion process	Activation energy in eV	
	Aluminum	Copper
Bulk diffusion	1.2	2.3
Grain-boundary diffusion	0.7	1.2
Surface diffusion	0.8	0.8

smaller than for the other diffusion types. Hence, EM is more prevalent at grain boundaries and boundary layers. The material determines which of the two diffusion paths has the lowest activation energy.

If one ignores boundary effects and focuses on the core of an interconnect, one will see that it is primarily the grain boundaries that serve as diffusion paths. Hence, the density and direction of grain boundaries in the interconnect lattice significantly affect susceptibility to EM, and thus also the resulting reliability of the interconnects.

The link between grain size and electromigration damage was first detected at the end of the 1960s, and aggregate failures occurring at the transition between different grain sizes were measured [AR70]. Two-thirds of the defects found in aluminum strips were found to have occurred at the transition between extremely different grain sizes.

Polycrystalline lattice structures with a low grain-boundary density are potentially more robust to EM. Near-bamboo or bamboo-type structures (see Fig. 2.9) have fewer grain boundaries aligned in the direction of current flow. Grain-boundary diffusion can thus be partially stopped by using such variants.

Near-bamboo structures have individual crystallites—known as *blocking grains*—that expand across the entire width of the interconnect and inhibit the diffusion flux. However, damage tends to occur in the proximity of these crystallites as a result of void formation or material accumulation. This damage is caused by a divergence in the diffusion that occurs at these blockages or triple points. *Triple points* are points at which grain boundaries branch off, so that one grain boundary from one direction proceeds as two in other directions, or vice versa (Fig. 2.10).

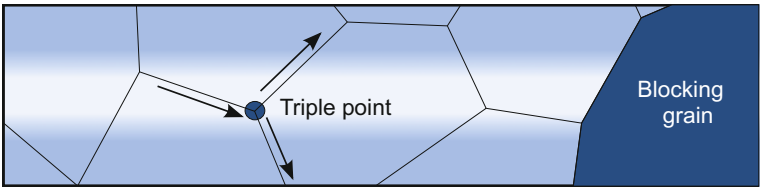

Fig. 2.10 Triple point(s) and blocking grain in a near-bamboo grain structure. In triple points, one grain boundary is split into two (or vice versa); blocking grains expand across the entire interconnect cross-section

2.4.2 Barriers of Copper Metallization

The use of copper interconnect has become dominant in recent years, but brings with it specific electromigration issues. Migration in copper wires is greatly affected by boundary effects due to the low activation energy for surface diffusion in copper (see Table 2.1).

Copper metallizations are primarily produced with *Damascene* technology (Fig. 2.11). This is a metal patterning process that can also be described as *additive patterning*. First, recesses, such as trenches (b) or via holes, are created in the previously deposited dielectric (a) in a lithographic process. Copper is then deposited on the wafer (c), so that the recesses are also filled. The wafer is then polished (d) by chemical-mechanical planarization (CMP), and the excess copper above the top edge of the recesses is removed. The interconnects and vias remain in the recesses.

Dual-Damascene technology can reduce the number of CMP steps involved: here, copper is deposited on an interconnect layer and a via layer underneath it in a single step. Hence, a trench and the underlying via may both be filled with a single copper deposition.

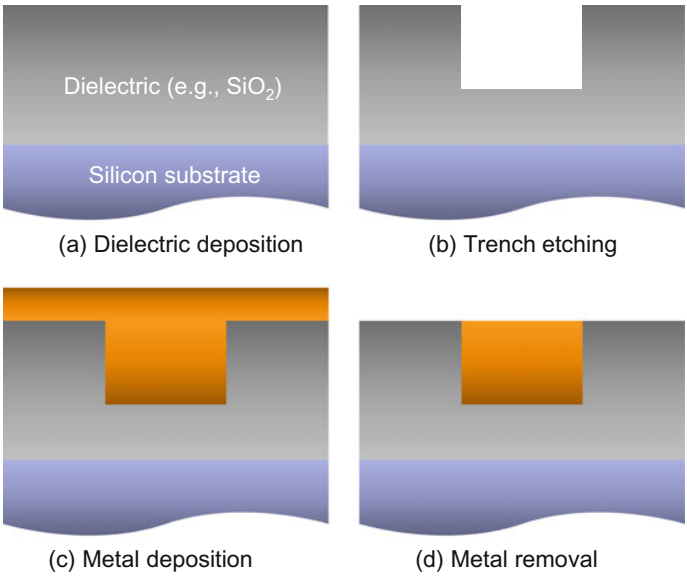

Fig. 2.11 A simplified schematic of the *Damascene* process on a cross-section of a copper track (**a**). The dielectric insulating layer is patterned with open trenches where the conductor is required (**b**). A coating of copper that significantly overfills the trenches is deposited on the insulator (**c**). Chemical-mechanical planarization (CMP) is used to remove the copper that extends above the top of the insulating layer (**d**). Copper sunken within the trenches is not removed and becomes the patterned conductor

It must be noted, however, that copper tends to diffuse considerably into neighboring silicon and silicon oxide at high temperatures [UON+96]. As a result, the above process is only beneficial if copper is treated with further technological measures.

In addition, temperatures on the order of 500 °C can be reached in the manufacture of the metallization—especially during the annealing process for creating bamboo structures (Sect. 4.2) [CS11]. The resulting diffusion has two major drawbacks: (i) a copper silicide layer with low conductivity is produced, and (ii) copper can degrade and destroy the semiconducting properties of silicon.

In order for circuits that incorporate copper metallization layers to function properly, *barriers* between metal and dielectric are essential. These diffusion barriers for copper and silicon must meet different criteria depending on their use. Good adhesion to copper and the dielectric, as well as thermal and mechanical stability with thin deposited layers (a few nanometers), are common criteria for these barriers.

The term *barrier* encompasses both the metallic diffusion barrier, the so-called *metal liner,* in the trench and the mostly dielectric protective coating, the *dielectric cap* (Fig. 2.12). There is therefore always a barrier between metal and dielectric (metal liner and dielectric cap) and between interconnect and the via above it (metal liner). This configuration is required to block diffusion especially during chip fabrication [UON+96].

The metal liner is deposited in the etched trench or via hole in the dielectric before the copper is deposited. The interconnect benefits from good electronic conductivity in the barrier, as the barrier layer (i.e., metal liner) is placed between the via and the underlying metal layer (see Fig. 2.12, right). In addition, the metal liner can also contribute to the current flow. This ensures a residual conductance especially in the event of faults arising from voids, thereby improving reliability.

The dielectric cap resides on top of the interconnects. Following the copper removal by CMP, a barrier to the above deposited dielectric is required. A dielectrical barrier is beneficial in preventing further structural modifications. A thin layer of dielectric cap material is deposited on the whole wafer prior to

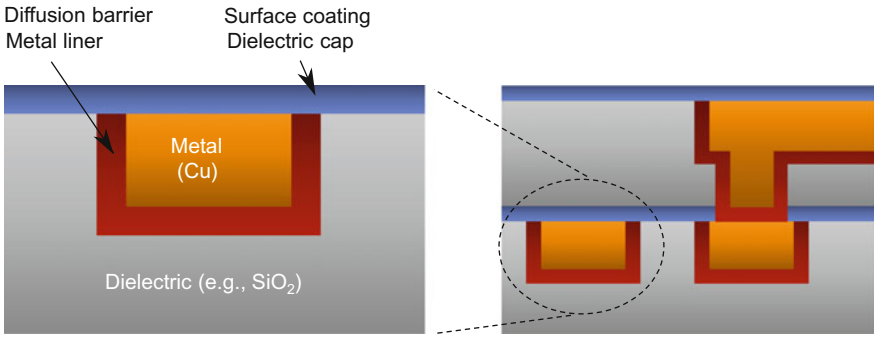

Fig. 2.12 Schematics of cross-section of copper tracks with the necessary, surrounding barrier layers (not to scale)

interlayer dielectric deposition. It needs only to be subsequently reopened when etching the via holes to make an electrical contact between the vias and the metal layer (see Fig. 2.12, right).

An electrically conductive cap would need to be structured lithographically, similarly to the underlying interconnect layer, in order to avoid shorts and parasitic conductance. Alternatively, the cap could be accumulated exclusively on the surface of the copper as a self-organizing process [CLJ08, LG09, VGH+12] and leaving out the exposed dielectric (Sect. 4.8.3).

With this better understanding of barrier construction and characteristics, we can now see, as noted earlier, that the barrier is a key factor for EM, as it forms a part of the boundary layer in copper metallizations that is critical for EM. Thus, the barrier greatly impacts the effective activation energy of the copper surfaces; we explore this below.

Theoretically, the activation energy of surface diffusion in the case of copper can be increased as well above the grain-boundary diffusion level by suitably selecting the barrier material, thus blocking surface diffusion. However, inhibiting one diffusion mechanism generally causes another mechanism to become predominant, leading to alternate damage scenarios. For example, the switch from aluminum to copper has eliminated grain-boundary diffusion, but it saw a significant increase in surface diffusion. Now, if surface diffusion is prevented by suitable dielectric and barrier layers, grain-boundary diffusion becomes an issue again. In the end, bulk diffusion may even emerge as the dominant process for electromigration, if all other mechanisms are suppressed. Every change in the dominant diffusion process therefore changes the failure modalities, as well, and increases the complexity of modeling procedures for EM prevention.

The difference between dielectric cap and metal liner also has a bearing on EM, as there are critical technological differences between the covered copper surfaces. In the dual-Damascene process [Gup09, Yoo08], a thick layer of copper is deposited on the wafer, and this layer is then removed by polishing (chemical-mechanical planarization, CMP). Copper is left only in the interconnect layer and underneath in the via layer. This process causes flaws in the surface of the metal, which also cannot be cleared in the process. The high defect density and vacancy concentration at the surface of the interconnects modify the surface characteristics at these locations and thus the activation energy. When combined with a worsening of adhesion of the dielectric cap, the top surface becomes more susceptible to electromigration damage, which is why voids typically occur on the top surface of an interconnect. These scenarios have implications on specific interconnect geometries (Sect. 4.4) and the materials used (Sect. 4.8).

2.4.3 Frequency Dependency of Electromigration

If the direction of the current in an interconnect is reversed, the direction of EM diffusion is also reversed. Due to this compensation by material backflow, damage

caused by EM can be partially cleared. This effect is known as a *self-healing*, which can significantly extend the lifetime of a wire.

Whether damage can be effectively remediated by self-healing, thus contributing to the service life of an interconnect, depends on the amount of damage done and to what extent the crystal lattice has been changed before the current reverses direction. Frequency is therefore the key parameter at work here, as, along with the duty factor[5], it defines the duration of the one-sided current load.

Very little metal is moved per half cycle at high frequencies. Hence, there are very few changes to the microstructure. The current flow in the second half cycle is approximately a mirror image of the flow in the first half cycle, so that it is highly likely that the changes are reversed. This delays the first occurrence of damage in the form of vacancy defects and voids. Tests carried out at different frequencies show that an alternating resistance change (the self-healing component) is superimposed on a slowly rising resistance [TCH93]. Partial self-healing is thus verified.

As described in [TCH93, TCC+96], the scale of self-healing can be expressed with the diffusion fluxes J as follows:

$$J_{\text{net}} = J_{\text{forward}} - J_{\text{back}} = J_{\text{forward}} \cdot (1 - \gamma), \tag{2.6}$$

where γ is the self-healing coefficient. This coefficient is determined by the duty factor r of the current and other factors influencing the scale of self-healing, such as the frequency.

In [DFN06], the self-healing coefficient γ is introduced by expanding Black's Eq. (2.1) as follows:

$$\text{MTF}_{\text{AC}} = \frac{A}{(r \cdot j^{+} - \gamma \cdot (1 - r) \cdot j^{-})^{n}} \cdot \exp\left(\frac{E_{\text{a}}}{k \cdot T}\right). \tag{2.7}$$

The self-healing coefficient γ is determined empirically in the same publication by:

$$\gamma = \frac{r \cdot \frac{j^{+}}{j_{\text{DC}}} - s \cdot \frac{\text{MTF}_{\text{DC}}}{\text{MTF}_{\text{AC}}}}{(1 - r) \cdot \frac{j^{-}}{j_{\text{DC}}}}. \tag{2.8}$$

The current density of the positive half cycle is j^{+}, and j^{-} for the negative half cycle. The scaling factor s is determined iteratively.

Tao et al. [TCH93] found a median lifetime (median time to failure, MTF) increase over low frequencies (DC, for example) for copper interconnects by a factor of 500 for frequencies ranging from 10 to 10^4 Hz (Fig. 2.13). Rectangular wave current signals were used in this study at frequencies ranging from a few mHz

[5]A duty factor is the fraction of one period in which a signal or system is active, i.e., it expresses the ratio of the positive pulse duration to the period. The duty factor is commonly scaled to the maximum of one. A duty cycle expresses the same notion; however, it is labeled as a percentage.

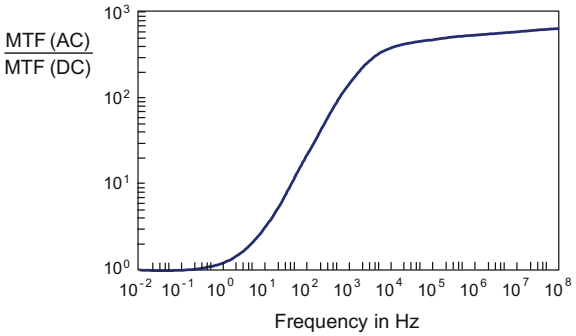

Fig. 2.13 Median time to failure (MTF) if interconnect is stressed by an alternating current (AC) compared to MTF if a directed current (DC) is applied [TCH93]. Note the almost linear increase in reliability when the frequency increases over several orders of magnitude (cf. Fig. 4.30, Chap. 4)

to 200 MHz. The reason for the limited lifetime of interconnects even at high frequencies, where we might hope for self-healing to extend the useful lifetime infinitely, is the interaction between EM and thermal migration, which degrades and destroys the interconnects. We discuss such interactions in Sect. 2.5.

It must be said, however, that the change in lifetime occurs in a frequency range that has very little relevance for today's digital circuits. Signals in this "low" frequency range are mainly handled by subcircuits that deal with the environment or the human-machine interface (Table 2.2).

Other signal frequencies are generally much higher (mega or gigahertz), while currents in supply lines consist of a dominant DC component with superimposed harmonics at very low frequencies. Hence, high frequencies on their own are not enough to prevent damage. The frequency dependency does, however, show that we need to differentiate between signal lines and power supply lines when dealing with EM.

An empirical model for healing damage is developed in [DFN06]; see Eq. (2.7). Shono et al. [SKSY90] also modeled the forward and backward transportation of metal due to the reversal in current flow. They assume that the amount of charge in both directions is the same (that is, there is no DC component), but that the current waveform is asymmetric w.r.t. time. While there are long current pulses of low

Table 2.2 Examples of relevant frequencies

Example	Frequency
Controlling the background lighting for a computer screen	10 mHz
Frame rate on a PC monitor	60 Hz
Sampling frequency for audio signals	44 kHz
Carrier frequency for radio frequency identification (RFID)	13.56 MHz
Processor clock frequency	3 GHz

amplitude in one direction, current pulses in the opposite direction are shorter with larger amplitudes. Hence, there is an asymmetrical material transport with a net flux in one direction due to the nonlinear relation between material transport and current density. The minimum lifetime is reached with the model at a duty factor, that is, the ratio of the positive pulse duration or pulse width (PW) to the period (T), of approximately 0.4.

Having shown the positive effects of alternating currents on reliability, we must also point out one drawback. Current is displaced from the current-carrying conductor at very high frequencies due to a phenomenon known as the *skin effect*[6]. At such high frequencies, the wire interior contributes very little to the current flow, which causes the current density to increase at the outer regions of the wire. A measure of the current displacement, the skin depth δ, is given by:

$$\delta = \sqrt{\frac{2\varrho}{\omega \cdot \mu}}, \tag{2.9}$$

where ϱ is the specific electrical resistance and μ the magnetic permeability of the conductor material. The variable ω represents the angular frequency with $\omega = 2\pi f$.

The current density decreases approximately exponentially, with the variable j_S representing equivalent surface current density and d as the distance from the surface, as follows:

$$j \approx j_S \cdot \exp\left(-\frac{d}{\delta}\right). \tag{2.10}$$

A better approximation of the current-density distribution as a function of the radius r in a long cylindrical conductor with current I can be analytically expressed as follows:

$$j_{\text{eff}}(r) = \frac{I}{2\pi r_0} \cdot \sqrt{\omega\kappa\mu} \cdot \sqrt{\frac{r_0}{r}} \cdot \exp[-\sqrt{\omega\kappa\mu} \cdot (r_0 - r)]. \tag{2.11}$$

In this formula from [KMR13], the electrical conductivity is represented by $\kappa = 1/\varrho$ and the cross-sectional radius of the conductor by r_0. As it stands, this analytical derivation of the current density cannot be applied to conductors with rectangular cross-sections. The mathematical model of a cylindrical conductor in Eq. (2.11) suffices here as an estimation of the magnitude.

In the case of copper, the skin depth at 50 Hz is approximately 9.4 mm and is proportional to $1/\sqrt{f}$. A critical frequency of 90 GHz was determined for the skin

[6]The skin effect is due to opposing eddy currents induced by the changing magnetic field resulting from the alternating current. This effect leads to a reduction in current from the outside to the inside of a metallic conductor as a function of the frequency and the electrical material constants of the conductor (permeability and conductivity).

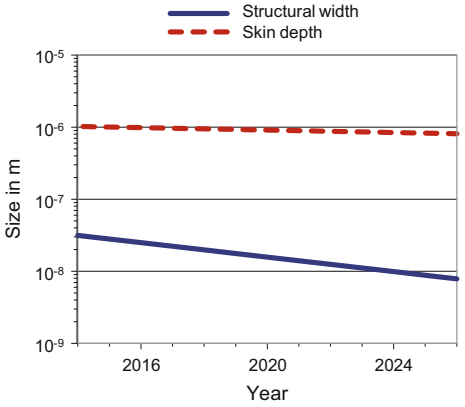

Fig. 2.14 A comparison between minimum structure sizes and skin depth in relation to the skin effect; data from [ITR14]. The graph shows that the skin effect can be ignored in future, as well, in the lower metallization layers for a semiconductor scale of 100 nm and less

effect for an interconnect of square cross-section with dimensions width W and height t with $W = t = 0.45$ µm in [WY02]. Using a similar calculation, the critical frequency of approximately 35 THz for the 22-nm technology node was found to be much higher.

Problems arising from the skin effect are not expected in digital circuits in the light of current developments in semiconductors with regard to track widths and clock frequencies [ITR14, ITR16]. The reason for this is that the interconnect dimensions are being downscaled more quickly than the frequency-dependent skin depth (Fig. 2.14).

We note that at present the skin effect can disturb the high-frequency signal components and thus the clock edges. Furthermore, the skin effect is reduced at lower conductivities and is thus weakened by the increasing influence of boundary effects on the interconnects.

2.4.4 Mechanical Stress

There are three main causes of mechanical tension (mechanical stress) in interconnects:

- The metal is deposited at high temperatures (approximately 500 °C) [CS11]. Mechanical stress is induced by the cooling to ambient temperature due to the different thermal expansion coefficients of metal and insulator.
- The growth of layers during metal deposition is generally uneven, which also produces mechanical stress in the metallization. This issue is more critical than the first effect according to [CS11]; the phenomenon can be illustrated by wafer curvature measurements [CS11, BLK04].

- The material transport caused by EM redistributes vacancies in the crystal metal lattice which, in turn, generate mechanical stress. A vacancy represents an absence of atoms; the absence of an atom needs less room than an atom at the same lattice site. Hence, the lattice can relax, leading to a local reduction in material volume and lower compressive stress.

The nature of the mechanical stress in interconnects can differ depending on the combination of materials and the production process. Damage is typically caused by tensile or compressive stress in the interconnect, which lead to a failure mechanism. Smaller tensions can be relieved by lattice dislocations and typically do not produce failure mechanisms.

As noted above, mechanical stress results from the fabrication of interconnects due to different thermal expansion coefficients and high temperatures during metal deposition. The temperature of the unstressed state, around 250 °C [ZYB+04], is generally significantly higher than the maximum operating temperature. Interconnects are exposed to mechanical tensile forces at standard operating temperatures, as the thermal expansion coefficient of copper, at 16.5×10^{-6} K^{-1} [Gup09], is much larger than the surrounding dielectric (SiO_2: 0.5×10^{-6} K^{-1} [YW97]).

Using the parameters Young's modulus E (a measure of the stiffness of a solid material) and temperature T

- $E(\mathrm{Cu}) = 117$ GPa,
- $E(\mathrm{SiO_2}) = 70$ GPa,
- $\Delta T = 200$ K,

and assuming identical widths of metal and dielectric (Fig. 2.15) for a one-dimensional calculation with the approximation:

$$\frac{\sigma}{E} = \varepsilon = \alpha \cdot \Delta T, \tag{2.12}$$

where ε is the strain and α the thermal expansion coefficient, we obtain a tensile stress σ of almost 140 MPa in the horizontal direction perpendicular to the longitudinal direction of the interconnect with:

$$\sigma = \frac{\alpha_{\mathrm{SiO_2}} - \alpha_{\mathrm{Cu}}}{\left(E_{\mathrm{SiO_2}}^{-1} + E_{\mathrm{Cu}}^{-1}\right)} \cdot \Delta T. \tag{2.13}$$

Tensile stresses promote the creation of voids. The modified topology resulting from the formation of voids tends to relieve tensile stresses, and the region at the edge of the voids typically becomes stress-free. Although voids may seem "beneficial" for their ability to relieve mechanical stress, void formation should be strongly avoided, as the mechanical contact between metal and dielectric is destroyed and the conductive cross-section of the interconnect is reduced.

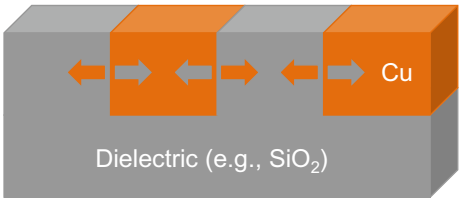

Fig. 2.15 Cooling of copper wires embedded in dielectric (silicon dioxide) leads to tensile stress, marked by arrows at the interfaces, due to differences in coefficients of thermal expansion (CTE)

The allowed compressive stresses in interconnects are usually greater than the allowed tensile stresses. If, however, a critical compressive stress threshold is exceeded, this also leads to a reduction in tension. In this case, interconnect extrusions are formed that spread into the neighboring dielectric as *dendrites, whiskers,* and *hillocks* (see Fig. 2.2). This is comparable to the transition from elastic to plastic deformation in solid mechanics.

Before extrusions arise, the vacancy concentration is scaled back further; this process is partially reversible through, e.g., self-healing (Sect. 2.4.3). Extrusions, however, are irreversible and lead to severe damage to the circuit, or its destruction.

2.5 Interaction of Electromigration With Thermal and Stress Migration

In addition to EM, there are three other types of diffusion in metallic connectivity architectures that can significantly impact reliability: thermal migration, stress migration, and chemical diffusion. IC designers must be especially aware of thermal and stress migration; both are introduced and described in their interaction with EM in this section.

Temperature gradients produce *thermal migration*. Here, high temperatures cause an increase in the average speeds of atomic movements. The number of atoms diffusing from areas of high temperature to areas of lower temperature is higher than the number diffusing in the opposite direction. As a result, there is a net diffusion in the direction of the negative temperature gradients, which can lead to significant mass transport.

Stress migration describes a type of diffusion that leads to a balancing of mechanical stress. Whereas there is a net atomic flow into areas where tensile forces are acting, metal atoms flow out of areas under compressive stress. Similar to thermal migration, this leads to diffusion in the direction of the negative mechanical tension gradient. As a result, the vacancy concentration is balanced to match the mechanical tension.

Chemical diffusion occurs in the presence of a concentration (or chemical potential) gradient, which also results in a net mass transport. This type of diffusion is always a nonequilibrium process; it increases system entropy[7] and brings the system closer to equilibrium. Since chemical diffusion is quite different from the migration processes mentioned above and does not directly relate to EM in metallic interconnects, it is not discussed further here.

Migration processes can lead to an equilibrium state, where the limiting (or counteracting) process is always another type of migration. There can be an equilibrium between electromigration and stress migration (the so-called *Blech effect*), between thermal migration and chemical diffusion (the so-called *Soret effect*), or any other combination of two or more migration types.

2.5.1 Thermal Migration

Temperature gradients produce thermal migration (TM), sometimes also referred to as *thermomigration*. Here, high temperatures cause an increase in the average speeds of atomic movements. Atoms in regions of higher temperature have a greater probability of dislocation than in colder regions due to their temperature-related activation. This causes a larger number of atoms diffusing from areas of higher temperature to areas of lower temperature than atoms in the opposite direction. The result is net diffusion (mass transport) in the direction of the negative temperature gradients (Fig. 2.16).

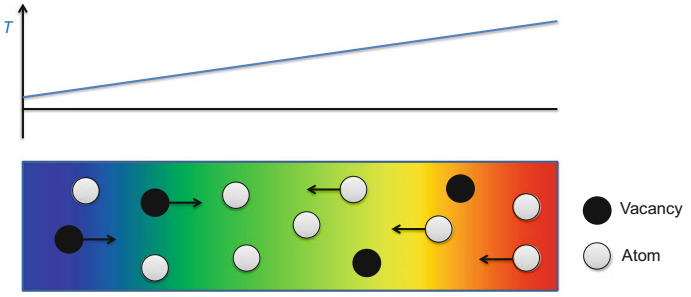

Fig. 2.16 Thermal migration (TM) is expressed by atomic and vacancy movement. It consists of mass transport from one local area to another, much like EM, with the difference that TM is driven by a thermal gradient rather than an electrical potential gradient (*T* temperature)

[7]Entropy is a measure of the "disorder" of a system. Hence, the more "ordered" or "organized" a system is, the lower its entropy. For example, building blocks that have been used to construct a wall are "highly organized" (i.e., they are arranged in a complex structure) and are thus in a *low-entropy* state. This state is achieved only by the input of energy. If this structure is left unattended, it will decay after a number of years, and the disorganized, high-entropy state will return (i.e., an unorganized heap of blocks).

The main reasons for temperature gradients in metal wires are

- Joule heating inside the wire caused by high currents,
- external heating of the wire, such as caused by highly performant transistors nearby,
- external cooling of the wire, which may result from through silicon vias (TSV) connected to a heat sink, in connection with low thermal conduction of the wire and its surrounding, such as through narrow wires surrounded by a thermally insulating dielectric.

Interestingly, thermal migration also contributes to thermal transport, as heat is coupled to the transported atoms. This means that thermal migration directly moderates its own driving force, which contrasts with EM, where current density is only indirectly reduced by increased resistance in some cases.

If the temperature gradients are beyond the control of the thermal migration, i.e., the equilibrium state of minimal energy and homogeneous temperature cannot be reached, a steady state can still be attained. In this case, migration is stopped by linear gradients of other migration processes' driving forces and entropy is generated by the heat flow [Soh09].

Thermal migration is very prominent in metal alloys such as solders, where migration dissolves the alloy due to different mobilities of the alloy components (the Soret effect) [Soh09]. Here, thermal migration and chemical diffusion set up an equilibrium. This, and the fact that temperature gradients are higher in packaging applications, makes thermal migration an interesting field of research especially in solder connections, such as flip-chip contacts.

The process has less influence in interconnect structures located within integrated circuits, as almost pure metals and no alloys are used, and the temperature gradients are tempered by the high thermal conductivities of metal and insulation.

Thermal migration has been an important field of study in solder joints, for it is likely to happen during regular operation. A temperature differential of 10 K across a flip-chip contact of 100 µm diameter creates a temperature gradient of 1000 K/cm, which suffices to induce thermal migration in the solder [Tu07].

2.5.2 *Stress Migration*

Stress migration (SM), sometimes also referred to as *stress voiding* or *stress-induced voiding* (SIV), describes atomic diffusion that leads to a balancing of mechanical stress. There is a net atomic flow into areas where tensile forces are acting, whereas metal atoms flow out of areas under compressive stress. Similar to thermal migration, this leads to diffusion in the direction of the negative mechanical tension gradient (Fig. 2.17). As a result, the vacancy concentration is balanced to match the mechanical tension.

The main reasons for mechanical stress as the driving force behind SM in metal wires are thermal expansion, electromigration, and deformation through packaging.

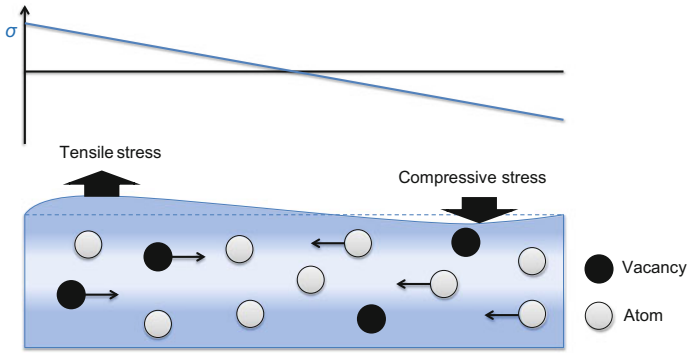

Fig. 2.17 Stress migration is a result of a mechanical stress gradient, either from external forces or from internal processes, such as electromigration or thermal expansion. Voids form as a consequence of vacancy migration driven by the hydrostatic stress gradient (σ mechanical stress)

A mismatch of the thermal expansion coefficients between metal, dielectric, and die material, and the temperature change from fabrication to storage, as well as the working conditions, cause most of the stress. By using TSVs for contacting 3D-stacked ICs, this initial stress is increased and it becomes less uniform, as well.

Metal lattices usually contain vacancies, i.e., some of the atomic positions in the lattice are unoccupied. Although they are aligned with the lattice grid, vacancies consume less space than atoms at the same positions. Therefore, the volume of a crystal that contains vacancies is to some extent smaller than the volume of the same crystal with atoms in the place of former vacancies. Vacancies play a major role in stress migration. Via Hooke's Law (which states that the strain or deformation of an elastic object is proportional to the stress applied to it):

$$\sigma = E \cdot \varepsilon \tag{2.14}$$

this volume is coupled with mechanical stress. Here, σ and ε are the mechanical stress and the strain, respectively, while E is Young's modulus. The change in volume (strain in three dimensions) correlates to an inverse pressure change. If the number of vacancies is reduced, pressure or compressive stress increases. The decline or increase in the number of vacancies is caused by the place change of atoms.

The stress gradient drives atoms from high pressure regions to regions with tensile stress and pushes vacancies in the opposite direction. This effect is equivalent to a highly viscous fluid that reacts slowly to an external pressure gradient. The external stress gradient is minimized in this case by structural deformation. Initially, microscopic atomic or vacancy motion facilitate this process. Temperature has a critical effect on the process, as it enables the "place changing" of atoms, which, in turn, causes vacancies to move.

In the case of external mechanical stress, the crystal lattice is stretched or compressed depending on the kind of stress. While there is an increased likelihood of atoms migrating to the stretched regions, atoms in the compressed regions are "pushed" outward to increase the number of vacancies; the required volume and the stress are thus reduced (Fig. 2.18). The result is an atomic flux from regions of compressive stress to regions of tensile stress until a static state with no stress gradient is reached.

If the stress is exerted *internally* by migration processes, e.g., by EM, there will be a greater concentration of vacancies in regions of tensile stress. This concentration will be balanced by stress migration to a steady state, where the atomic flux due to EM is compensated by SM.

If the number of vacancies induced by *external* stress or EM exceeds a threshold, the vacancies unite to form a void due to vacancy supersaturation. This phenomenon is often called *void nucleation*. Subsequently, the tensile stress is reduced to zero by the resulting crack [HPL+10]. At the same time, the driving force for SM changes, as well as the equilibrium state (Fig. 2.19).

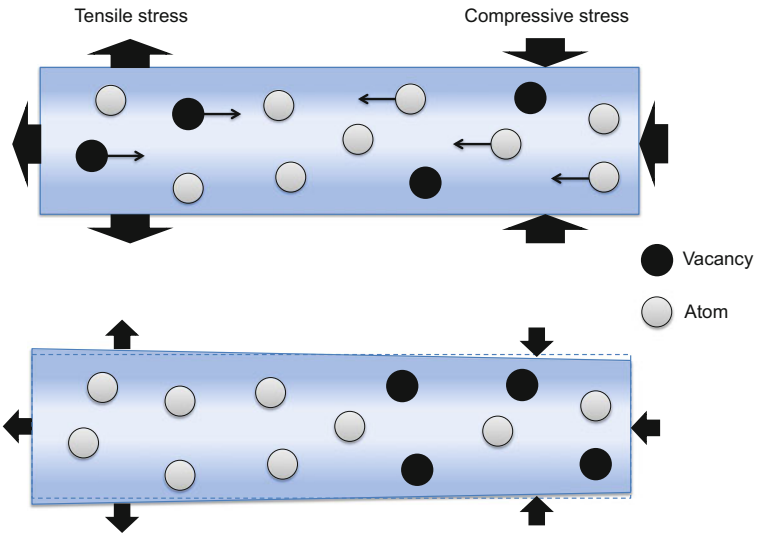

Fig. 2.18 Stress migration leads to diffusion of atoms and vacancies (*top*) to eliminate the origin of this migration (*bottom*). Atoms migrate into the stretched regions (left-hand side, outward-facing stress arrows), whereas atoms in the compressed regions are "pushed" outward (right-hand side, inward-facing arrows). Note that this material flow from compressive to tensile stress is in the opposite direction compared to the EM flow

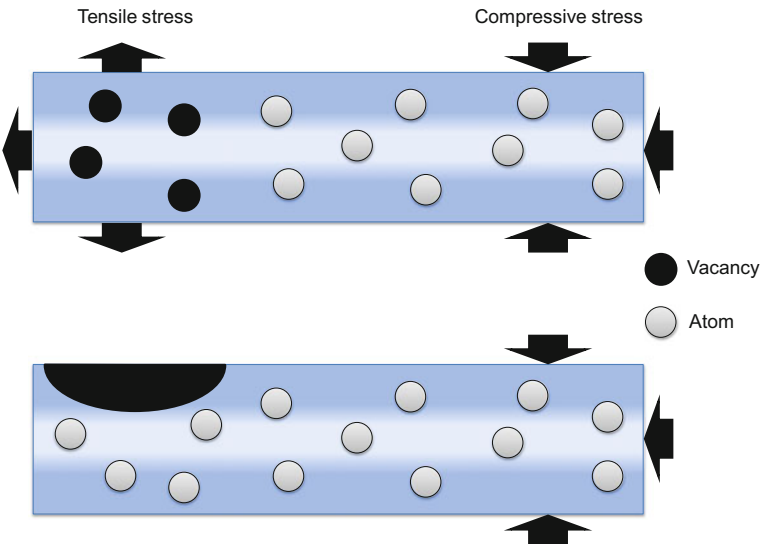

Fig. 2.19 Vacancy supersaturation (*top*) leads to the formation of voids (*bottom*), also called void nucleation. Note that the resulting crack at *bottom* eliminates the (external) tensile stress

2.5.3 *Mutual Interaction of Electromigration, Thermal and Stress Migration*

Electromigration (EM) interacts directly with stress migration (SM), as the dislocation of metal atoms induces mechanical stress, which is the driving force behind SM. SM works against EM, as its flow is directed from compressive to tensile stress which is the opposite direction to the EM flow. The resultant net flow is thus reduced, and the damaging dislocation due to EM is slowed or even halted.

Thermal migration (TM) on the other hand is not a dedicated EM countermeasure, as it is less dependent on the current direction than EM. Its direction can differ from the EM direction depending on the temperature gradient, which might stem from sources other than current density.

While temperature accelerates EM as well as the other migration types, we observe most likely a mixture of all three types in the event of a current-density hotspot. For the effective application of countermeasures, the dominant migration force must be identified.

EM, TM, and SM are closely coupled processes as their driving forces are linked with each other and with the resultant migration change (Fig. 2.20).

Current density increases the temperature through Joule heating, and temperature change modifies mechanical stress through differences in the expansion coefficients. Furthermore, temperature and mechanical stress affect the diffusion coefficient [see Eq. (2.20)], which in turn modifies the behavior of all three migration types. In

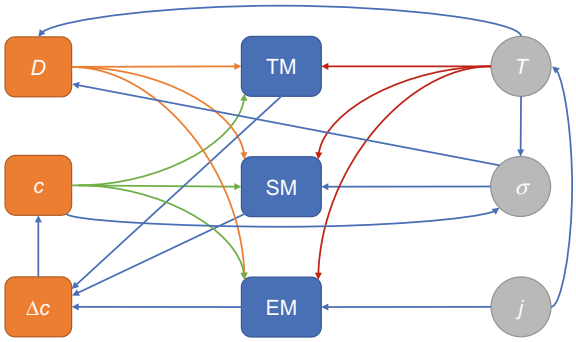

Fig. 2.20 Interaction and coupling between electromigration (EM), thermal migration (TM), and stress migration (SM) through their driving forces current density (j), temperature (T), and mechanical stress (σ). Also shown are the migration parameters diffusion coefficient (D), concentration (c), and concentration change (Δc), respectively

addition, the mechanical stress is influenced by the change in atomic concentration caused by all migration types individually.

The effects of different combinations of the three main migration types are depicted in Figs. 2.21 and 2.22. Depending on the origins of the driving forces, several different amplifying and compensating results are observed.

The causes and effects of migration are interrelated and at times self-reinforcing. For example, recall our earlier discussion on void growth, current density, and Joule

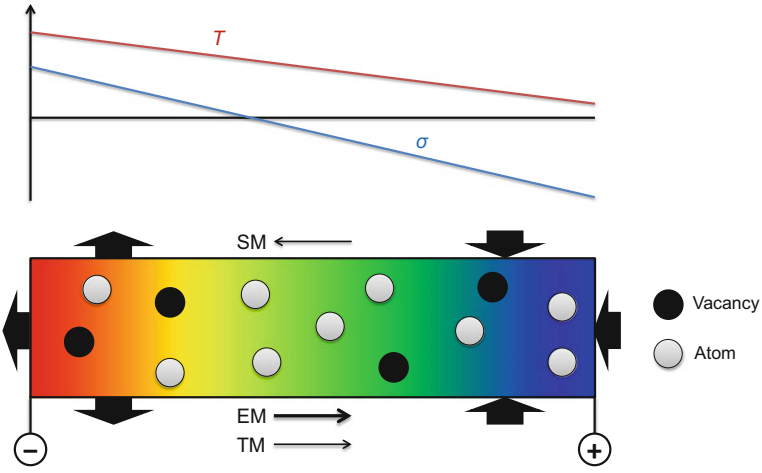

Fig. 2.21 Example of coupled migration processes in a wire segment, where electromigration and thermal migration proceed from left to right, while the stress migration flow moves in the opposite direction (T Temperature, σ mechanical stress)

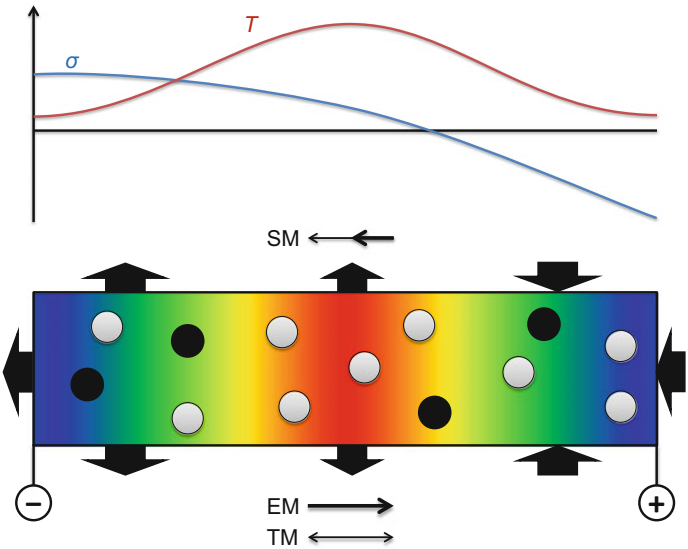

Fig. 2.22 Another example of coupled migration processes. Here, thermal migration is induced through a hotspot in the middle of the segment, while the stress is a superposition of tensile stress in the middle and EM-induced stress. This situation may occur near thermal vias or TSVs

heating in reference to Fig. 2.4, where we illustrated the acceleration of void growth by the positive feedback of a temperature rise. In general, the effects of different migration modes should be considered as interdependent. In particular, the material flows J_E from EM, J_T from thermal migration, and J_S from stress migration can be calculated as follows [WDY03]:

$$\vec{J_E} = \frac{c}{kT} \cdot D_0 \cdot \exp\left(-\frac{E_a}{kT}\right) \cdot z^* e \varrho \vec{j}, \tag{2.15}$$

$$\vec{J_T} = -\frac{cQ}{kT^2} \cdot D_0 \cdot \exp\left(-\frac{E_a}{kT}\right) \cdot \text{grad } T, \tag{2.16}$$

$$\vec{J_S} = -\frac{c\Omega}{kT} \cdot D_0 \cdot \exp\left(-\frac{E_a}{kT}\right) \cdot \text{grad}\, \sigma. \tag{2.17}$$

In these equations, c is the concentration of atoms, k Boltzmann's constant, T the absolute temperature, D_0 the diffusion coefficient at room temperature, E_a the activation energy, z^* the effective charge of the metal ions, e the elementary charge, ϱ the specific electrical resistance, j the electrical current density, Q the transported heat, Ω the atomic volume, and σ the mechanical tension (stress).

The resultant diffusion flux, defined as follows:

$$\overrightarrow{J_a} = \overrightarrow{J_E} + \overrightarrow{J_T} + \overrightarrow{J_S}, \tag{2.18}$$

is the net effect of the combined driving forces.

The individual diffusions can flow in the same or in opposite directions. There is also a coupling of the effects, that is, the feedback effect of the diffusion on the causes of the material transfer, which should not be ignored. For example, the critical length effects, covered later in this book (Sect. 4.3), arise from this type of negative feedback between EM and SM.

The resulting diffusion flow in one dimension is described in [Tho08] as follows:

$$J_a = \frac{Dc}{kT} \cdot \varrho j z^* e + \frac{Dc}{kT} \cdot \Omega \cdot \frac{\partial \sigma}{\partial x}, \tag{2.19}$$

where J_a is the atomic flux, D the diffusion coefficient of copper, represented by:

$$D = D_0 \cdot \exp\left(-\frac{E_a}{kT}\right), \tag{2.20}$$

c is the concentration of copper atoms, j the current density, z^* the effective charge of copper, e the elementary charge, k the Boltzmann's constant, T the temperature, Ω the atomic volume of copper, σ the mechanical tension (stress), and x the coordinate parallel with the segment with $x = 0$ at the cathode.

In order to prevent EM effects, the net diffusion flow must be reduced to zero. This means that the diffusion flow from EM and, for example, the corresponding diffusion flow from SM (in the opposite direction) may be used to cancel each other out.

2.5.4 *Differentiation of Electromigration, Thermal and Stress Migration*

The particular damage arising from a given migration type cannot be identified by appearance, as all damage, regardless of its root cause, results in voids caused by diffusion processes (Fig. 2.23). However, the locations and surroundings of these different damage types provide evidence as to their possible origin(s) (Fig. 2.24).

Diffusion barriers are key in all diffusion processes considered here because damage will most likely occur near such barriers, due to flux divergences and the effects of bad cohesion.

As discussed earlier, EM takes place inside wires and is driven by electric currents. Therefore, EM damage correlates mostly with the current direction and strength. EM damage is most likely to be found in areas of high current density, that is, high currents and small cross-sectional areas. In addition, current crowding at wire bends and vias is a strong EM indicator.

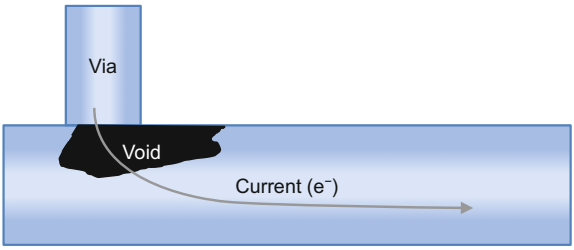

Fig. 2.23 Visualization of damage caused by the combined effect of EM, SM, and TM (side view)

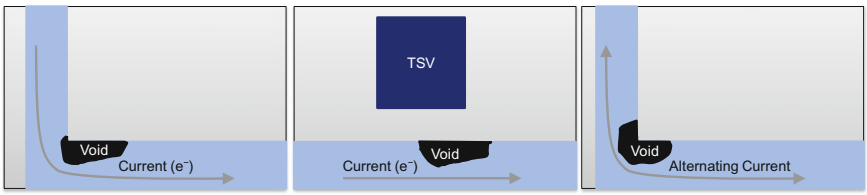

Fig. 2.24 Different types of damage typically caused by EM (*left*), SM (*middle*), and TM (*right*) (top view). In most cases, the respective damage cannot be differentiated by its appearance, but rather by its location and surroundings

TM correlates somewhat with EM, as large temperature differences appear near locations of high current densities. Therefore, current crowding spots are also high temperature spots that are a potential TM driver. Here, large temperature differences (in addition to current differences) "push" the atoms.

There are many other reasons for temperature gradients, such as external heating or cooling and the heating of active circuit elements, namely transistors. Furthermore, thermal conduction influences temperature gradients. Thermal conduction can also dislocate TM damage from hotspots in the wires toward cooling spots or areas of low thermal conductivity. This might be a TM indicator, whereas EM is always coupled to large current locations.

Another EM characteristic is its requirement of a directed current flow. Wires with alternating current flow, such as digital signal lines, often show TM as a partial source of damage growth (in addition to EM, see Fig. 2.24, right).

Due to the prevailing combination of different materials in an interconnect system, the resulting temperature inhomogeneities always lead to mechanical stress. Therefore, TM is mostly coupled with SM, with SM often being the dominant force. In order to apply appropriate countermeasures, we need to know whether large temperature gradients can occur inside the region of interest, or if the migration is driven by stress gradients only. These different migration scenarios require different countermeasures.

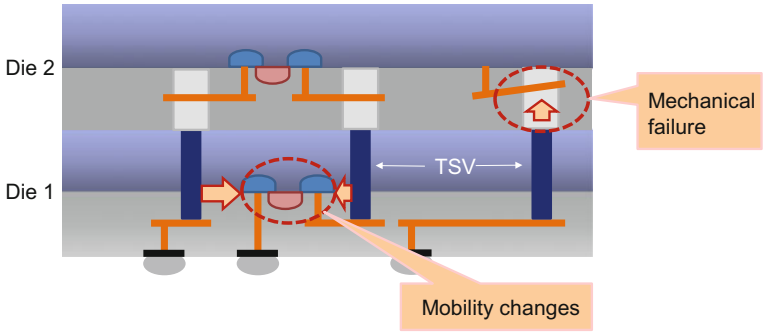

Fig. 2.25 TSVs in 3D-stacked ICs induce mechanical stresses in their surroundings because of the mismatch in the coefficients of thermal expansion between silicon and copper, and other effects [XK11]. This results in mechanical failures and electrical degradation, such as mobility changes in transistors. As one precaution, keep-out zones around TSVs are recommended

SM is often coupled with EM in terms of counteraction. EM-transported atoms induce mechanical stress that consequently leads to SM in the opposite direction to the causal EM. SM therefore has the potential to reduce EM damage in short wire segments (Sect. 4.3) and in locations of low current densities.

SM due to mechanical stress not only originates from EM, but also from fabrication, mismatches between different coefficients of thermal expansion (CTEs), and induced stress from obstacles like TSVs. With the increase in 3D-IC applications, damage near structures such as TSVs in 3D-stacked ICs is rapidly becoming critical. In most cases, it is SM related: TSVs induce stress on their surroundings due to the mismatch in the coefficient of thermal expansion values between silicon ($\alpha_{Si} \sim 3 \times 10^{-6}\ K^{-1}$) and copper ($\alpha_{Cu} \sim 16.5 \times 10^{-6}\ K^{-1}$) as a TSV fill. The resulting mechanical stress leads to, among others things, silicon wafer cracking, debonding between wafers and TSV protrusion, signal degradation and cracking (Fig. 2.25) [XK11]. Hence, to successfully implement TSVs, the mechanical stresses in the copper TSV itself as well as in the surrounding silicon substrate must be controlled. As one precaution, keep-out zones around TSVs are created for active devices to minimize their stress-related mobility changes[8] [KML12].

Finally, we would like to point out that hillocks and whiskers (see Fig. 2.2) usually indicate EM as their cause. However, SM can also participate in the overall diffusion flow and, hence, must be considered as well.

[8]Electron mobility is a measure of how quickly an electron can move through a material such as a metal or semiconductor, when pulled by an electric field.

2.6 Migration Analysis Through Simulation

This last section of this chapter introduces and describes the principles of a migration analysis through simulation. We discuss EM analysis using current-density simulation techniques, such as the finite element method (FEM), in Sect. 2.6.1. We also outline more sophisticated simulation strategies in the following subsections. For example, the atomic flux can be calculated from current density and other driving forces to get a deeper insight into the migration process (Sect. 2.6.2). We may also simulate mechanical stress development as the driving force behind stress migration (Sect. 2.6.3). Void growth can be simulated in order to gain a detailed look into damaging processes (Sect. 2.6.4).

2.6.1 Simulation Techniques

Migration is a complex problem that can be described by a system of differential equations. For this type of mathematical problem, several solving strategies exist and can be classified as follows:

- analytical methods,
- quasi-continuous methods,
- concentrated or lumped element methods, and
- meshed geometry methods, such as
  - finite element method (FEM),
  - finite volume method (FVM), and
  - finite differences method (FDM).

All these methods must respect numerous boundary conditions given by the simulation problem as well as the coupling effects of the different physics domains participating in the migration process. The solution space consists of a set of variables, also called "degrees of freedom," which must be adjusted to fit the boundary conditions and equations.

The system of differential equations can only be solved *analytically* in closed form and with acceptable effort for very simple geometries and boundary conditions, or by extremely simplifying the problem by neglecting some transport processes and simplifying the geometry, for example.

To facilitate the solution space, *quasi-continuous methods*, such as "power blurring" [ZPA+14], have been developed. In contrast to concentrated elements, this method provides a spatially resolved solution by superposition of analytical expressions for a finite number of spatial points, like a grid. It uses a matrix convolution technique similar to image processing methods to combine the separate point solutions to a global solution. This approach consumes less computational power than meshed solutions while losing some of the flexibility, as it is harder to implement inhomogeneous material properties. For temperature calculations, as

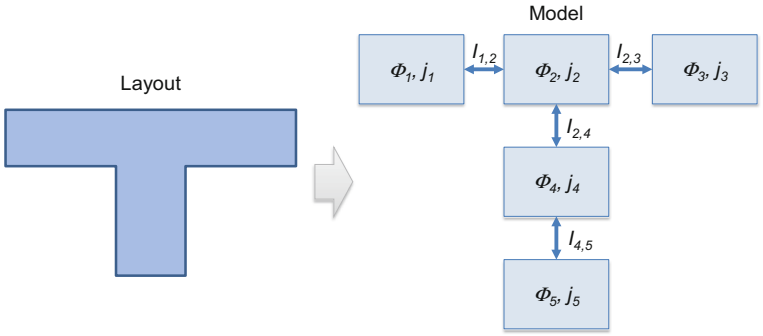

Fig. 2.26 Illustration of the lumped element model where several analytically or numerically solved geometries are combined (Φ electrostatic potential, j current density, I current)

used in power blurring, quite reasonable results can be obtained, even for full-chip analysis [KYL15].

A *concentrated or lumped element method* (Fig. 2.26) is really an extension of the analytical method, where several analytically or numerically solved geometries are combined. This method is very fast, but calculates only a single value for each degree of freedom and element. The results are global without any spatial resolution inside the segments, as the elements are typically quite large, e.g., one element per wire segment.

Meshed geometry methods (Fig. 2.27) offer several advantages for migration analysis. The degrees of freedom can be spatially resolved in a variable manner by adjusting the mesh granularity. The calculation effort is limited due to the bounded degrees of freedom—the mesh is finite. Using only basic geometries for the mesh elements further simplifies the simulation.

The *finite element method* (FEM) is a universal tool for calculating elliptic and parabolic equation systems. It is a numerically very robust method. Many tools

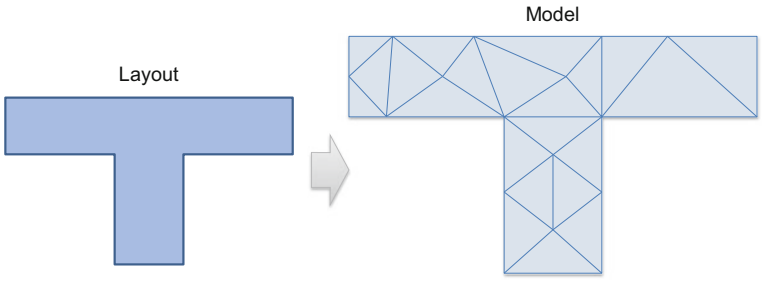

Fig. 2.27 Illustration of the meshed model where the spatial resolution of the degrees of freedom can be adjusted by the mesh granularity. Hence, each mesh node has its own degrees of freedom, such as the electrostatic potential

support FEM due to its great variety of applications. The system of equations is built from degrees of freedom for nodes and elements.

The *finite volume method* (FVM) uses polyhedrons to divide the given geometry, while solving the equations only at the center of each polyhedron. FVM is best suited for conservational equations, such as mass flow calculations for fluid and gas transport. It could be applied to migration when modeling atomic flux similar to gas diffusion.

The *finite differences method* (FDM) is numerically very simple and therefore well suited for theoretical analysis or very fast calculations. Due to its simplicity, its results are not as exact as with FEM. As its name suggests, the system of equations is based on the differences in the degrees of freedom.

All these methods are regularly deployed for solutions in computational fluid dynamics (CFD), which has a lot in common with migration simulation in solid state.

For reduced problem sizes, such as EM analysis restricted to power and ground nets, meshed methods deliver precise results in reasonable calculation times. However, when applying meshed methods to complex geometries, model preparation and calculation efforts are extremely high. These issues apply also in EM analysis, as geometries in VLSI circuits are becoming increasingly complex. Since signal nets are more and more EM-affected, filtering only EM-critical nets, as proposed in [JL10], will no longer sufficiently curb problem complexity. This growing challenge of complexity for finite element simulations for EM problems in VLSI circuits is clearly shown in Fig. 2.28.

Quick simulations are required in physical design. These simulations are only one part of the verification phase; they must be repeated iteratively in the design flow. For example, applying FEM for use in the full-chip verification of complex integrated circuits is too time consuming [TBL17].

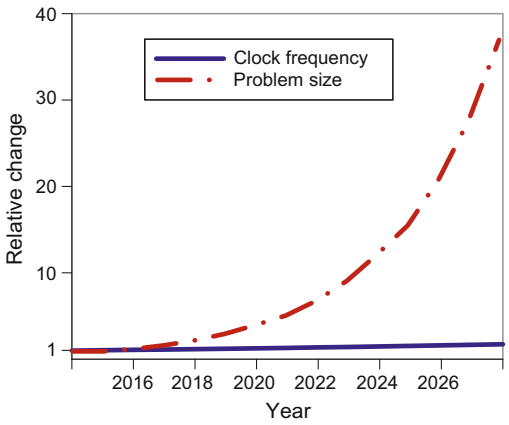

Fig. 2.28 Prediction of the analysis complexity for future digital circuits, i.e., shown is the growing problem size of finite element simulations of all signal nets in future technologies, as predicted by the ITRS, with 2014 as the base year. The respective CPU clock frequencies are also depicted for comparison purposes. Calculated from ITRS [ITR14, ITR16]

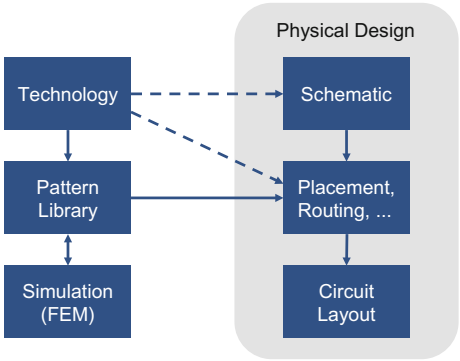

Fig. 2.29 To mitigate increasing circuit complexity, an EM simulation based on FEM should be uncoupled from the actual verification process. The resulting layout synthesis would then use a pattern verification method that restricts physical design to pre-verified (routing) patterns [TBL17]

In order to maintain FEM precision despite the increasing number of structures and geometries to be analyzed, we propose that EM simulations must be separated from the actual verification process. This means that FE analysis is performed prior to verification or even prior to routing. Routing will then be implemented exclusively with verified routing elements from a library. Hence, a whole library of routing elements with simplified parametric models attached will be verified in an FE analysis. The complete chip can then be verified rapidly. The library should include all routing elements required to build a complete layout; the library size can be minimized by selecting highly repetitive patterns. The verification is simplified to calculating only actual critical results from the actual boundary conditions by using the parametric models to check against current-density limits, or other migration metrics (Fig. 2.29).

An important prerequisite for the above-mentioned verification method of combining several discrete FEM simulations is that the partial solutions equate with the respective parts of the complete solution. This requirement is fulfilled if the boundary conditions are transformed correctly between the full and partition models, as we discuss next.

The method's prerequisite can be best explained in a typical example, where a complete wire connection is simulated as a whole and then split into separate parts. If we can transform the boundary conditions to the parts in a suitable manner, the simulation results will be equivalent.

There are several useful rules for finding the locations to split the model. The best place to split is at locations where the boundary conditions are homogeneous, as they can easily be applied to FE models. This is the case, for example, with current-density regions in a straight wire that are located at some distance from vias and branches. If, however, the layout element of interest consists only of the via region, some appendices will have to be added to the wires in order to establish a homogeneous boundary condition.

The atomic flux, on the other hand, stops at diffusion barriers, that is, the transition from one material to another (this typically occurs near vias). These diffusion barriers offer ideal boundary conditions for this model.

In the case of mechanical stress, it may not be easy to find ideal locations for dividing the model into smaller partitions because mechanical stress is also driven by the wire's surroundings; a homogeneous stress condition is difficult to find around a wire.

Temperature influences and mechanical stress from "unmodeled" surroundings should not influence the simulation results. Therefore, a larger wire surrounding area should be modeled, so that the difference between homogeneous model conditions and inhomogeneous real conditions can be neglected inside the wire.

The same applies when modeling temperature directly, as the surrounding dielectric distributes heat as well as the metal, only with lower conductivity.

In summary, it is important to verify that FE routing models can be partitioned without losing accuracy if one wants to apply FEM for full-chip current-density analysis. This verification is best done by comparing the simulation results for generic sample patterns calculated both separately and combined. Figures 2.30, 2.31, and 2.32 visualize this using a T-shape wire segment inside one metal layer and a via connection. Figure 2.30 shows the current-density results from two separate (distinct) simulations. The simulation of both patterns combined is pictured in Fig. 2.31; the combined results correspond well with the separately calculated results. Figure 2.32 indicates current-density distribution at the interface between the two patterns in a joint simulation; this is a measure of the error in the individual simulations. The maximum error is 3% in the visualized case; this is an acceptable value that has been verified for other patterns as well [TBL17].

By pre-evaluating interconnect structures in advance and building the layout exclusively from evaluated structures, verification is significantly accelerated: even a single circuit simulation, i.e., generating the (simulated) library patterns and using

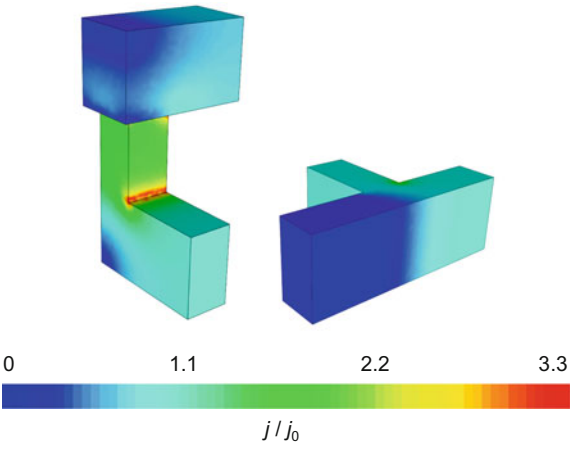

Fig. 2.30 Current-density distribution using FEM for a T-shape wire segment and a via connection. Shown are results of separate simulations of the two single patterns with homogeneous constraints at the cut surfaces

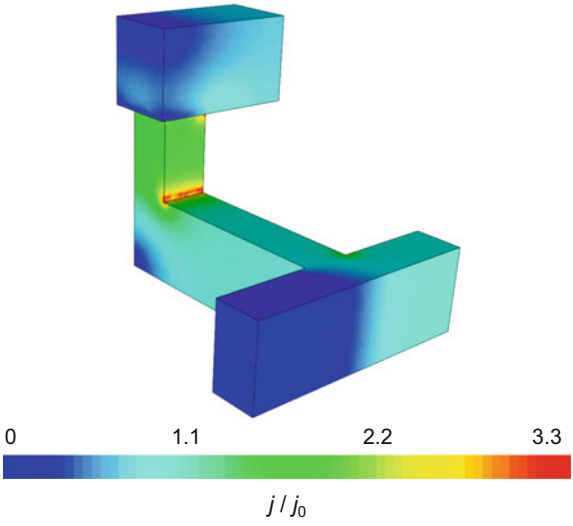

Fig. 2.31 Visualizing the joint FEM current-density simulation of the two patterns in Fig. 2.30 when combined indicates sufficient similarity with the results of the disjoint simulations (cf. Fig. 2.30)

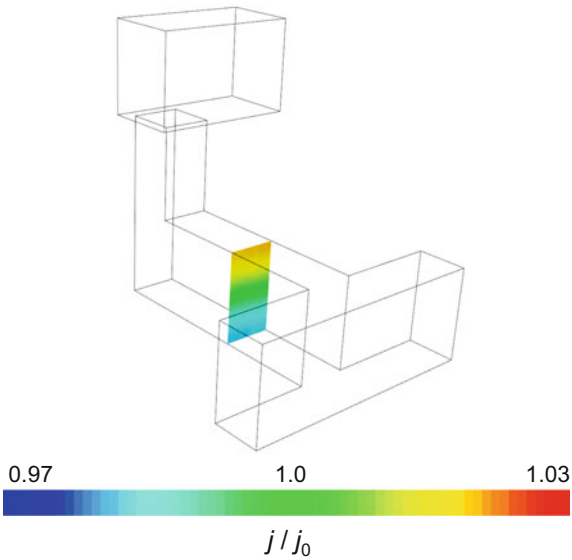

Fig. 2.32 Verifying homogeneity of the current density at the cut surface between the two FEM submodels (the maximum deviation is 3% here) can be used to ensure that distinct and combined simulations show matching results. Hence, FE wiring models can be partitioned without accuracy loss if one wants to apply FEM for full-chip current-density analysis

them only once, can be faster than a conventional, complete FEM simulation of the entire final layout [TBL17].

The aforementioned method of pre-verifying routing patterns allows FEM, including its precision and spatial resolution, to be applied in the EM verification of complex circuits. All circuit nets can be verified by following the proposed method. We believe this is a particularly important result, as it will fill a looming gap in the

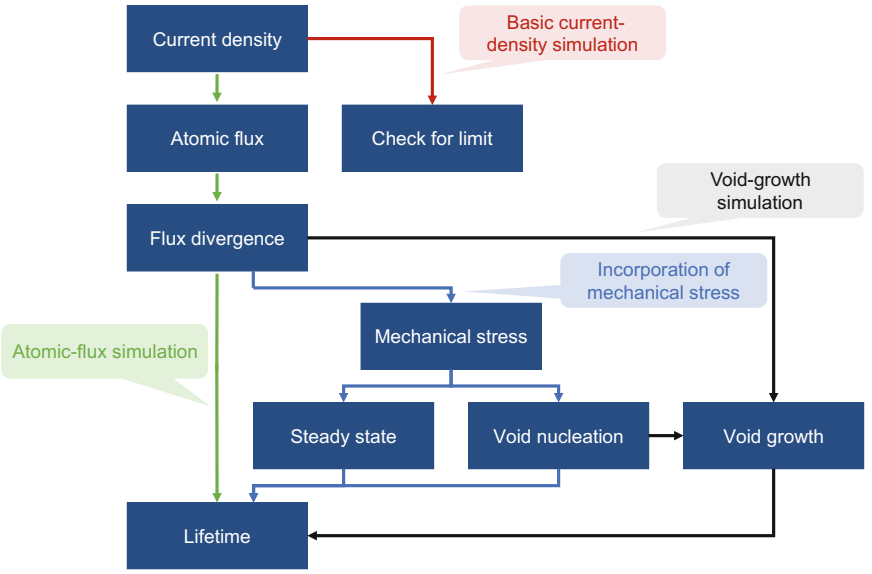

Fig. 2.33 Simulation strategies for EM analysis based on different parameters affecting migration

near future when all segments will be severely EM-affected (Chap. 1, cf. Fig. 1.6, red area).

So far we have discussed EM analysis using current-density simulation and a subsequent comparison with current-density limit(s). There are also several other, more sophisticated simulation strategies for EM analysis (Fig. 2.33); these are outlined in the following subsections. For example, the atomic flux can be calculated from current density and other driving forces to get a deeper insight into the damaging process (Sect. 2.6.2). Furthermore, we can simulate mechanical stress development as the driving force behind stress migration and compare it with the critical stress (Sect. 2.6.3). Void growth can be simulated in order to gain a detailed look into damaging processes, in terms of both void nucleation (mechanical stress change) and void growth (Sect. 2.6.4).

2.6.2 *Atomic-Flux Simulation*

The diffusing atom flux is used to quantify the rate of diffusion. The flux is defined as either the number of atoms diffusing through a unit area per unit time (atoms/(m^2·s)) or the mass of atoms diffusing through a unit area per unit time (kg/(m^2·s)).

The atomic flux can be calculated by solving the systems of equations for all migration driving forces and deriving the sum of all fluxes. In our case of EM analysis, the migration driving forces are the current density for electromigration,

the temperature gradient for thermal migration, and the mechanical stress gradient for stress migration.

In this section, we explain how to calculate the atomic flux when the driving force is known. Numerous models are available for solving this task. In the following discussion, we go from the smallest scale to more abstract models.

The most natural approach is to calculate the *movement of single atoms*, also called atomistic simulation. In the case of interconnect structures, this yields a statistical model or, in small scale, a stochastic material transport model. The driving force or work W_p is translated into a material flux or mean velocity $\bar{v}$ by relating it with an energy barrier and the atomic mobility. The resistance of an atom to motion is given by its binding energy E_b and its mass, or mobility m. This leads to the exemplary equation as follows:

$$\bar{v} = \left(W_p - E_b\right) \cdot \frac{1}{m}. \tag{2.21}$$

Single atomic migration can be calculated on this basis. Probabilistic calculations must be made in order to obtain an atomic flux from this approach.

A more abstract method of calculating atomic flux uses collective atomic properties to calculate a *mean flux*. Here, statistics over a certain number of atoms are included in the model equation.

The most abstract model uses Eqs. (2.15)–(2.20) from Sect. 2.5.3 to calculate an atomic flux from the driving forces of the migration types. This deterministic model gives only mean flux results.

The atomic flux can be calculated in a quasi-static simulation (Fig. 2.34) which determines the initial atomic flux and the spatial flux divergence. Hence, critical regions can be directly identified in the locations of large divergences. Lifetime and robustness can then be estimated by extrapolating this flux.

The microstructure has a significant influence on EM, as diffusivity differs for bulk and grain boundaries [COS11]. Hence, different local EM properties are

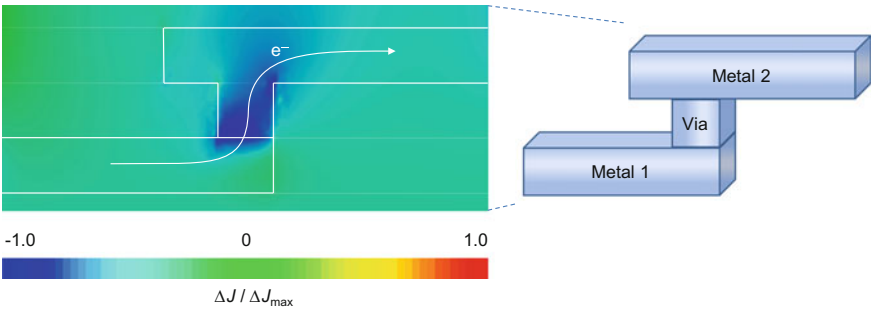

Fig. 2.34 Atomic flux divergence calculated from electromigration (FEM results) shows via depletion (side view)

changed due to microstructural variations. Furthermore, mechanical properties depend on crystal orientation—an important factor in SM as an EM countermeasure. Therefore, the microstructure must be included in the geometric models.

The microstructure can be incorporated in the geometric models by using a microstructure generator to establish a structure from median grain size and a given standard deviation, as noted in [COS11]. As microstructure and crystal orientation cannot be completely controlled by process technology, this method gives results for one arbitrary configuration only. In reality, however, the positions of grain boundaries and the crystallographic orientations cannot be arranged. Hence, deterministic methods will not yield realistic simulation results. A probabilistic analysis of the microstructure effects is, therefore, required for reliable outcomes [COS11].

The divergences can be deduced from the atomic-flux simulation results; these allow the lifetime of the layout structure, for example of a wire, to be estimated by extrapolation.

2.6.3 Simulation of Mechanical Stress

In addition to simulating atomic flux due to EM, it is mandatory to calculate the mechanical stress caused by atomic flux, as it is key to determining the steady-state condition in the metal wire. In particular, the total flux in short wires greatly depends on mechanical stress.

The obtained steady state leads either to an "immortal" wire (cf. Sect. 4.3) or the void size in this state gives an indication as to the wire's lifetime.

As metal wires in integrated circuits are confined, i.e., encapsulated, by dielectric material, every material movement annihilates and/or generates vacancies. There are different models of mechanical stress generation and evolution due to this process, such as the Korhonen model[9] [Ye03]. It describes the stress by the one-dimensional equation as follows:

$$\frac{\partial \sigma}{\partial t} = \frac{\partial}{\partial x}\left[\frac{D_{\mathrm{a}} B \Omega}{kT}\left(\frac{\partial \sigma}{\partial x} - \frac{z^* e \varrho}{\Omega} j\right)\right], \tag{2.22}$$

where σ is the hydrostatic stress, t is the time, D_{a} is the atomic diffusivity, B is the applicable modulus, Ω is atomic volume, k is Boltzmann's constant, T is absolute temperature, z^* is the effective charge number, e is electron charge, ϱ is the resistivity, and j is the current density [Ye03].

[9]The Korhonen model combines vacancy dynamics with stress development. It assumes that the recombination and generation of vacancies alter the concentration of the available lattice sites, which influences the hydrostatic stress distribution. Specifically, the loss of the available lattice sites increases the hydrostatic stress.

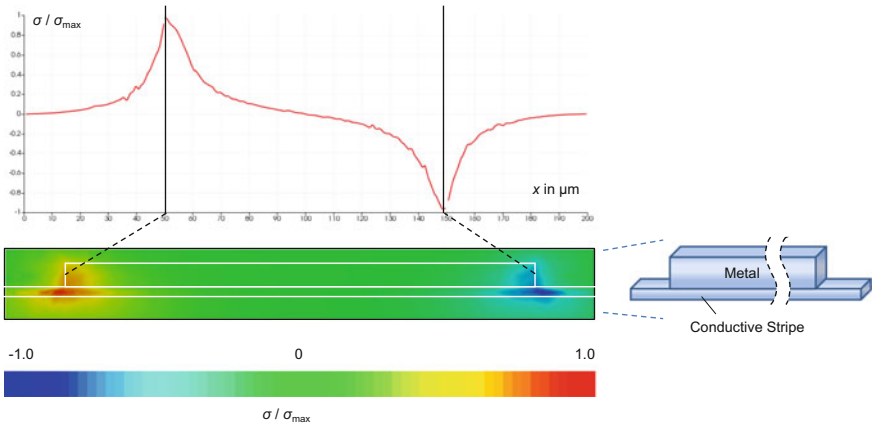

Fig. 2.35 Simulation results for mechanical stress through EM after a fixed stressing time. The nonlinear stress gradient inside the wire is shown (side view)

In addition, several similar and more sophisticated models exist for three-dimensional calculations [Ye03].

Having determined the mechanical stress due to EM, overstepping the critical stress threshold indicates where void nucleation starts [CS11]. In the case of a transient EM simulation to this point in time, the nucleation time and, depending on the dominant failure mechanism, the wire lifetime can be estimated.

This failure criterion—void nucleation—is equivalent to a small resistance increase in experiments, according to [CS11]. Simulation results can thus be experimentally verified.

EM lifetimes vary widely due to high stress thresholds and large variations in grain distribution [CS11]. Hence, probabilistic calculations are necessary here as well.

To illustrate these mechanical stress considerations, simulation results are shown in Figs. 2.35 and 2.36. Figure 2.35 illustrates the mechanical stress buildup after a fixed simulation time, and Fig. 2.36 depicts a steady-state condition in a short wire.

2.6.4 Void-Growth Simulation

Void growth can be simulated to provide deeper insight into the electromigration processes and the effects that lead to failure. We can thus estimate the lifetime of different layout structures in a very detailed fashion. In general, void-growth simulation is the third step in a migration analysis, following the estimation of driving forces and the atomic flux calculation. Therefore, it incorporates relatively complex mathematics to calculate its results.

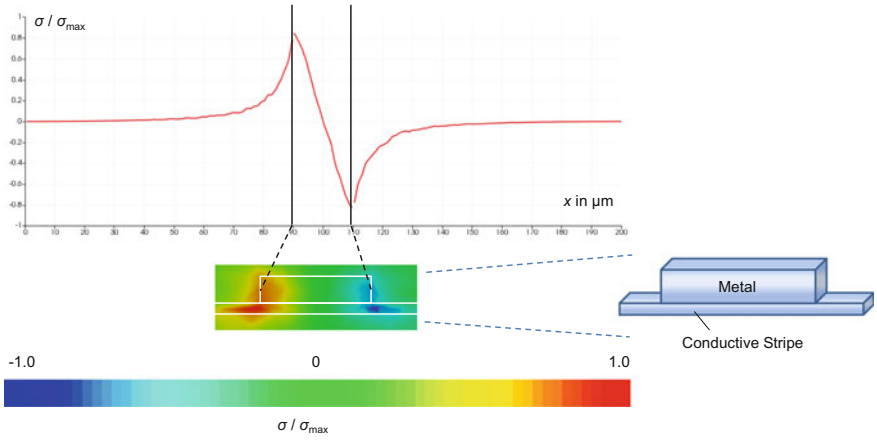

Fig. 2.36 Simulation results for a short-length segment including mechanical stress. The steady state with linear stress profile inside the segment is shown (side view)

After having calculated the (static) atomic flux, actual atomic *motion* increases the vacancy concentration in certain locations and voids are created by vacancy supersaturation. This process and the change of the void shape must be modeled as well in order to estimate void growth and, hence, the lifetime of a layout structure. A transient simulation is necessary to calculate the void growth.

As there are many parameters in the complex calculations and some assumptions may be necessary, the results may not be reliable. We also need to conduct a statistical analysis on input parameter variations to make useful conclusions based on the simulation results.

When considering void nucleation it is important to note that during EM, and in combination with mechanical stress, a significant grain-boundary movement takes place [CS11]. Here, grain boundaries drift into the neighboring crystallite lattice (grain) as a result of atomic rearrangements. Under these circumstances, one grain grows at the expense of another. This process must be considered as well, as it influences the overall diffusion flow and causes electrical resistance fluctuations.

The applicability of finite element models for simulating migration processes and void growth until failures occur has been shown in [BS07] and [THL07].

Two methods are available for modeling void growth in a meshed geometry:

(1) geometry modification depending on volumetric loss of affected elements (Fig. 2.37), similar to a method from [OO01], and
(2) deletion of mesh elements upon exceeding a certain mass flux divergence limit (Fig. 2.38), as presented in [WDY03].

Both methods must also include surface tension models to generate the energy-based void shape modification. The aims of these models are to gain a deeper understanding of void growth and, thus, to identify methods for lifetime

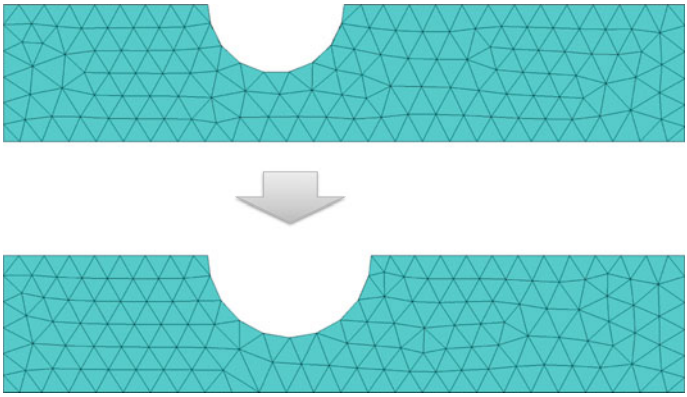

Fig. 2.37 Void-growth model using mesh geometry modification [OO01]

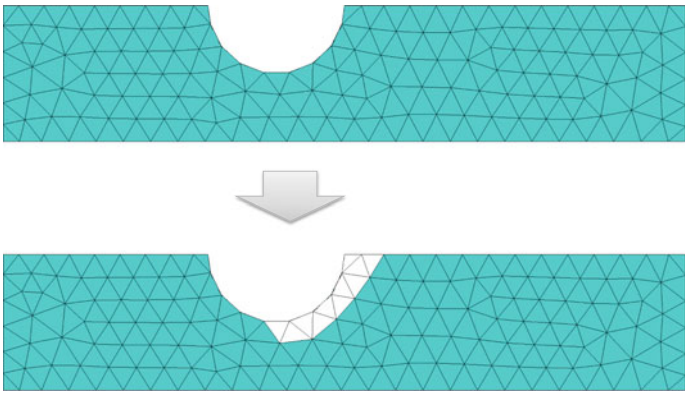

Fig. 2.38 Void-growth model using deletion of mesh elements [WDY03]

extension. The latter can be achieved by modifying wire geometries or by implementing special reservoirs; both methods are presented in detail in Chap. 4.

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