

Chapter 2

Getting Hands on Altera® Quartus® II Software

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Abstract This chapter provides users with overview and capabilities of Altera® Quartus® II design software in programmable logic design. The book is designed around the Altera DE2 development platform. The Altera Quartus II software is the most comprehensive environment available for system-on-a-programmable-chip (SOPC) design. Here we provide a guide that will help one to install the Quartus software, setting up the license for installed Quartus. This chapter also gives the details about the steps involved in creating the first embedded project, building projects' steps, and how to port the programming file onto the development board.

Keywords Altera • Quartus II • SOPC • Embedded platform

This chapter provides users with overview and capabilities of Altera® Quartus® II development software tool in programmable logic design. Quartus II software platform is more suitable for system-on-a-programmable-chip (SOPC) design in many applications. This chapter will give simple and easy steps to user about how to install software setup and the license creating first embedded design and simulation of entire design.

2.1 Installation of Software

This chapter gives the minimum requirements of the system and installing procedures of Quartus II software.

System Requirements

Following minimum system requirements need to be verified before Quartus II software installation.

- Pentium II PC runs at more than 400 MHz with at least 256 MB RAM
- Disk space 1 GB where you are installing the Quartus II software
- Windows NT version 4.0, Windows 2000, or Windows XP
- CD-ROM drive
- Following ports availability:
 - Parallel port for ByteBlaster™ II or Byte BlasterMV™
 - Serial port for Master Blaster™
 - USB port for USB-Blaster™
- Internet Browser, i.e., Internet Explorer 5.0 or later

Uninstalling Previous Versions of Quartus II Software

Before starting with the fresh installation of Quartus II, it is recommended by Altera to uninstall the previously installed version of Quartus II by following below steps. Sometimes user can install new version without removing the old one by simply specifying the new installation directory.

Choose Start > All Programs > Altera > Quartus Uninstall, Repair or Modify.

Running the Setup of Quartus II

Following steps need to be followed to install the Quartus on user system:

Quartus software installation is allowed only if user has administrator privileges.

1. Insert CD having Quartus II Software into CD-ROM drive. Immediately, several installation options pop up and one can click on install option. Setup can also be started manually by performing the following steps:
 - a. Start > Run.
 - b. In the dialog box, type <CD-ROM drive>:\install.
 - c. Press OK.
2. After clicking on Install Quartus II Software, installation starts automatically and guides user during installation process.

2.2 Setting Up of License

Licence.dat file needs to be obtained before setting up of license for Quartus II.

Steps to Obtain the license file

- (1) Browse the portal address www.altera.com/licensing.
- (2) Select **Get licenses** link which is the first blue link on the page.
- (3) Press on **Get a license for Quartus® II Web Edition software**.
- (4) One can get one time access if you create an account using you email id.
- (5) Once you create username, go back to Step 2.
- (6) To get license you have to provide system network interface card number (NIC).

NIC number is a twelve digit hexadecimal number that recognizes your system, and one can easily find the NIC of system by typing `ipconfig/all` at a windows command prompt.

To obtain NIC number, following command typed on command prompt window:

```
Ipconfig/all
```

Search for following line

```
Physical Address .....00-ED-6C-59-91-4F
```

Then on licensing tab, user has to enter the above NIC without the (-).

Once you submit the required information, the license file will be emailed to you.

Once the user receives license file, next step is to do the license setup if the user has Windows XP system, and then specify the location of the license file by following the below steps:

- i. Choose start > Control Panel.
- ii. Click on System in Control Panel window.
- iii. Then click on Advanced tab > click Environment Variables.
- iv. Click on New tab Under System Variables. Then new system variable dialog box appears.
- v. Specify Variable Name as `LM_LICENSE_FILE`.
- vi. In the value box, type either `<drive>:\flexlm\license.dat` or server host name `<port>@<host>`. If there are more than one license file or server, separate the port and host specifications with semicolons (;), with no spaces between the names and numbers.
- vii. Click OK.

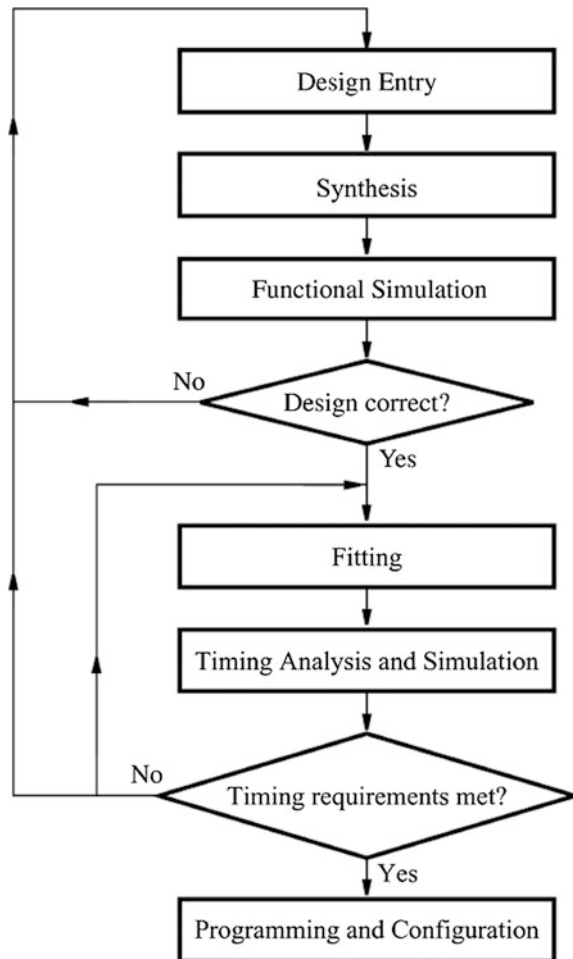
2.3 Creation of First Embedded System Project

Here we will briefly introduce the Quartus II CAD for simple system. CAD flow is used for designing circuits which are implemented in FPGA using Quartus II software. How to use Quartus II Software for creation of simple embedded project on FPGA is explained in this section. The tutorial explained here uses VHDL to create design entry; here user clearly defines the desired circuit in the VHDL. Two other methods are Verilog description and Block Design file (BDF).

Background

A FPGA CAD flow is illustrated in Fig. 2.1. CAD tools make it easier for designer to implant the desired logic.

Fig. 2.1 FPGA design CAD flow



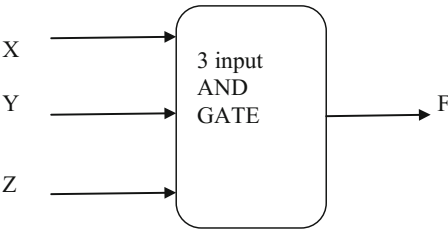
Following are the steps of CAD design flow:

- Design entry—Here user defines the circuit in BDF or HDL, i.e., VHDL or Verilog.
- Synthesis—The entire design is synthesized into a circuit which consists only logical elements.
- Functional simulation—This verifies the functional correctness; Here timing issues are not taken into consideration.
- Fitter—This tool helps to find the exact placement of LEs in FPGA as specified in the Netlist; it also selects wire routings to make the necessary connections of specific LEs.
- Timing analysis and simulation—Propagation delays along the various paths in the fitted circuit which are analyzed to provide an indication of the expected performance of the circuit.
- Timing—The fitted circuit is tested to verify both its functional correctness and timing configuration.
- Programming—The designed design is downloaded on the FPGA chip by programming which configures the various logical elements (LEs).

Embedded project design for three-input AND Gate

Here we consider simple three-input AND Gate, and detail steps to create a project are given below.

Logic Block Diagram



TRUTH TABLE

+-----+-----+			
INPUT		OUTPUT	
+-----+-----+			
--	X Y Z	F	
-- +-----+-----+			
--	0 0 0	0	
--	0 0 1	0	
--	0 1 0	0	
--	0 1 1	0	
--	1 0 0	0	
--	1 0 1	0	
--	1 1 0	0	
--	1 1 1	1	
-- +-----+-----+			

VHDL code

```

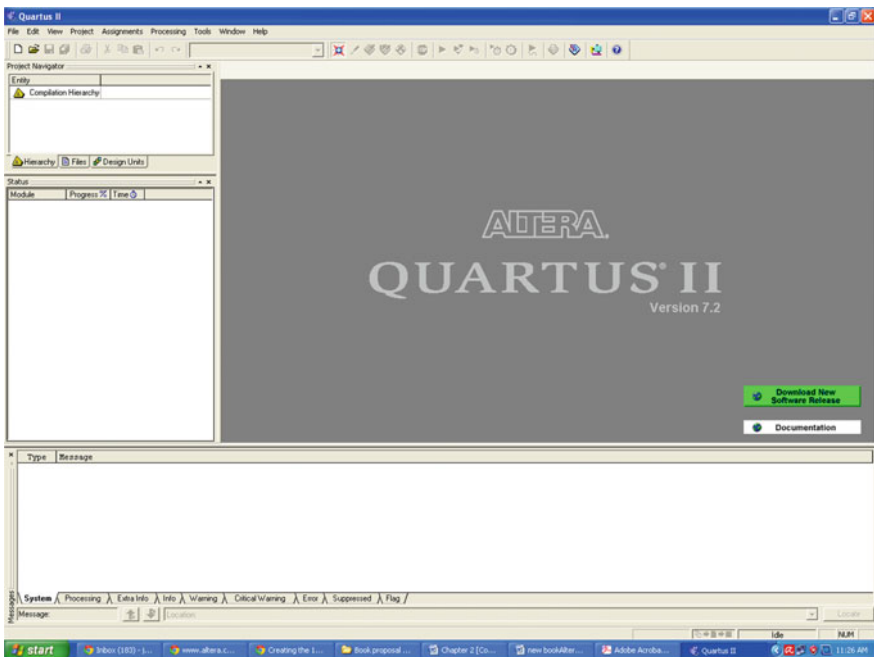
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;

entity and3 is
port (X,Y,Z: in STD_LOGIC;
      F: out STD_LOGIC);
end and3;

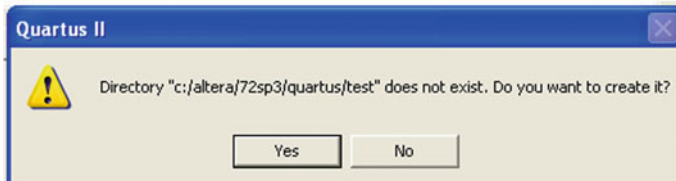
architecture BEHAVIORAL of and3 is
begin
  F <= (X AND Y AND Z);
end BEHAVIORAL;

```

- (1) Goto Start > All programs > Altera > Quartus II 7.2 sp3 web edition the following window appears.



- (2) Once the licensing setup is done, you can start working on Quartus by creating a project. Click on File → Create New Project wizard.
- (3) The window shown in Fig. 2.2 pops up and one has to enter the directory to save project files, then assign name to file and a project, and click Next. (Note: top-level entity name must be same as file name).
- (4) Then click Next in the following popup that comes, and it says directory does not exist. Do you want to create it? Say yes.



- (5) Next window appears which will ask you to provide filename, do not assign any file name at this point just click on next Fig. 2.3 appears which will ask you to select the FPGA Family and Target on your respective Development Board (Cyclone II EP2C35F672C6).
- (6) Click Next two times, you will get summary of project (Fig. 2.4) which complete the project creation. Then click finish.
- (7) Select File > click on New, the window shown in Fig. 2.5 appears, select VHDL File, and press OK.

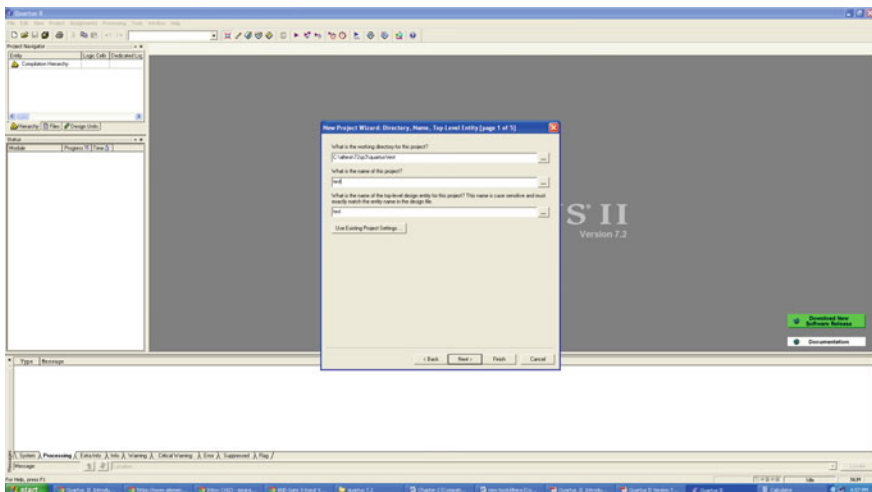


Fig. 2.2 Top level entity design name

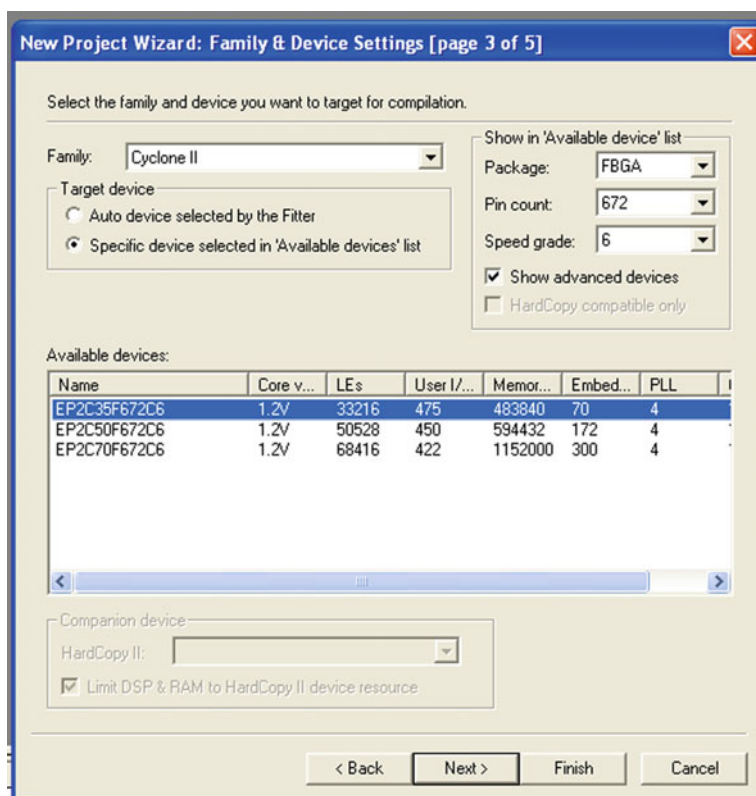


Fig. 2.3 Select FPGA device

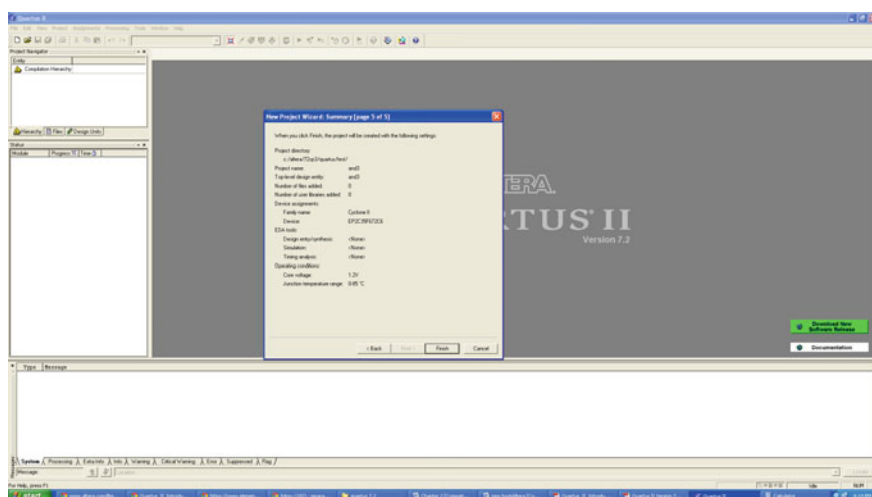
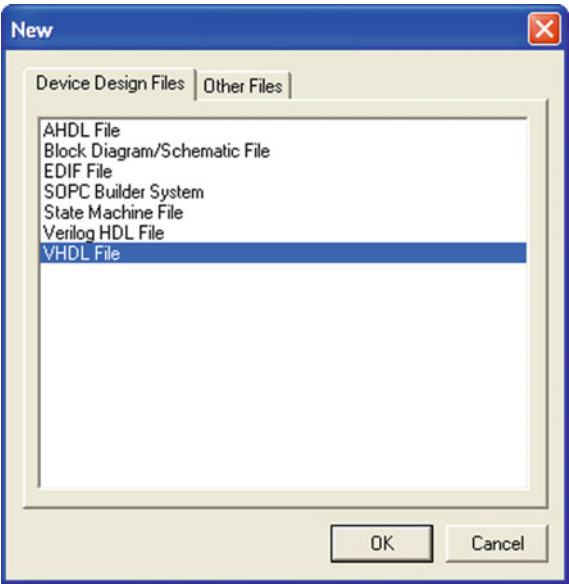


Fig. 2.4 Summary of project settings

Fig. 2.5 Choosing VHDL file



- (8) Then type in your logic code in the editor (Fig. 2.6) then go to file > save as, assign the file name same as entity name.
- (9) **Next step is assignment of FPGA pins.**

There are two ways of assigning the pins, manual pin assignment and automatic pin assignment:

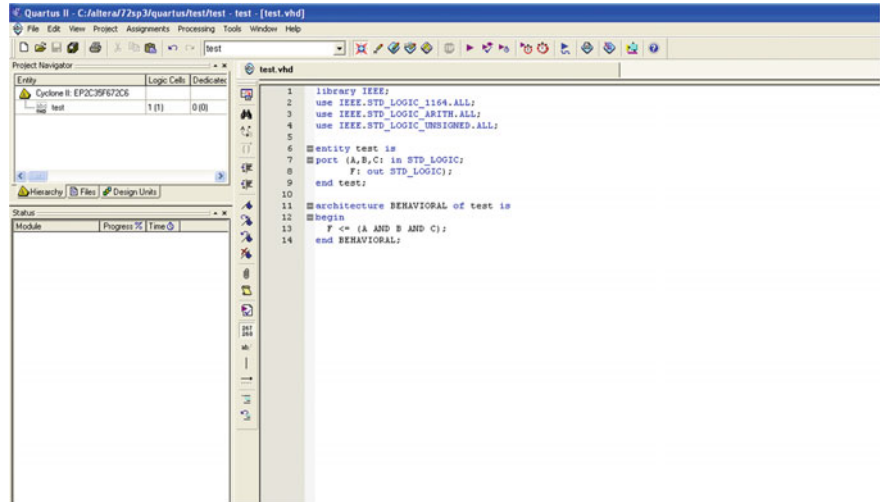


Fig. 2.6 Three-input adder VHDL code

(1) Manual Pin Assignment:

Here to see the pins in Assignment editor, directly one has to compile the entire system by clicking the start compilation under the processing toolbar; once the entire system is compiled without any errors (warnings generated are accepted), then go to Assignment → Pins.

Assign the respective pins of input to switches and output pins to LEDs.

(2) Automatic Pin Assignment

- Store the DE2 board pin assignment excel file on the computer
- Click on Project → Import design partition then select the location of pin assignment file stored on computer → click OK
- Go to project → generate tcl script for project then click OK.

2.4 Project Building and Compilation

- (1) After completing the design, next step is to compile the design for errors.
- (2) Click on Processing tab → start compilation This is shown in Fig. 2.7.

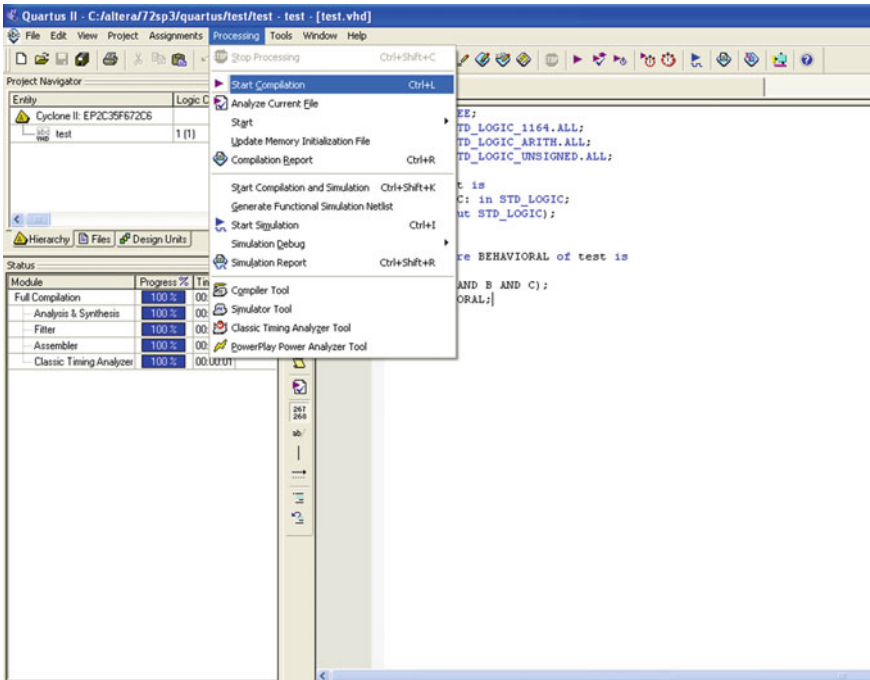


Fig. 2.7 Compilation of project

- (3) After successful analysis and synthesis, compilation report is generated as shown in Fig. 2.8. If there are errors, then click on that error so that it helps you for debugging the design.
- (4) If you want to see the designed system at Netlist (Gate) level, on the menu bar select tools > click on Netlist Viewer > RTL Viewer as shown in Fig. 2.9.

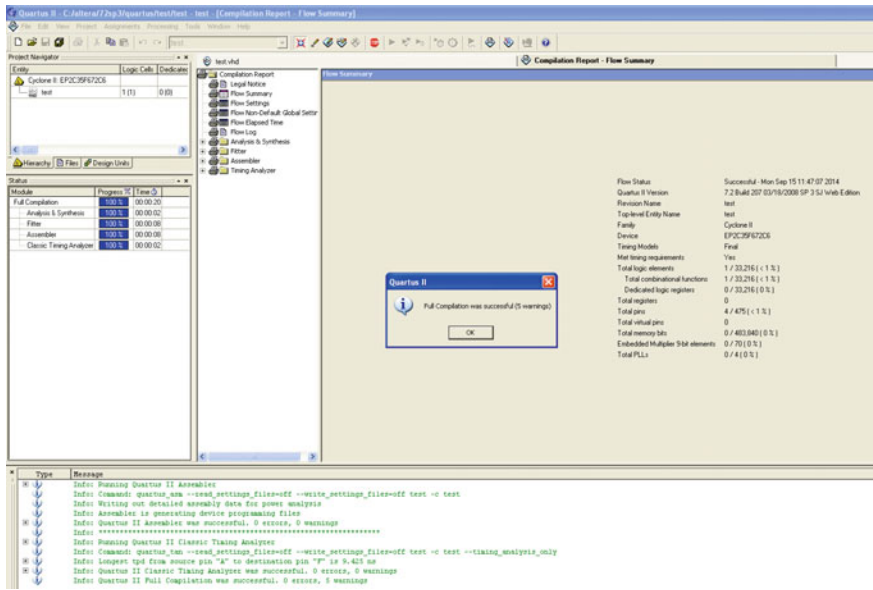


Fig. 2.8 Report of compilation

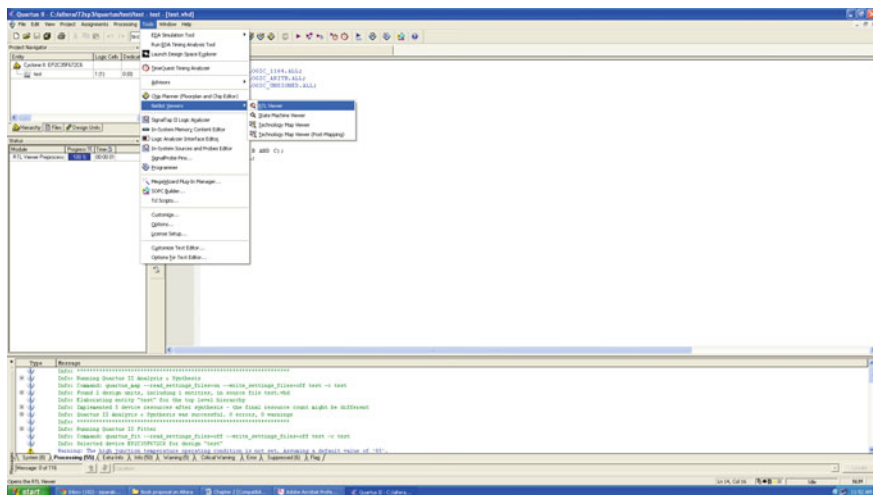


Fig. 2.9 RTL viewer selecting window

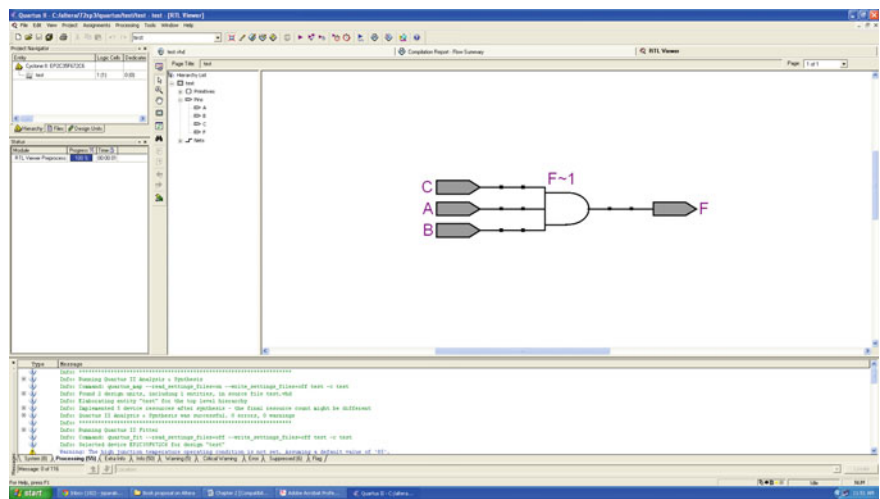


Fig. 2.10 RTL schematic of three-input AND Gate

After clicking on RTL, viewer, it will show Gate-level architecture as shown in Fig. 2.10.

Simulation of designed system

After successful compilation, the designed system can go for simulating the waveforms.

Select **File** → then click on **New** → **Other Files** → **Vector Waveform Files**, the window shown in Fig. 2.11 appears.

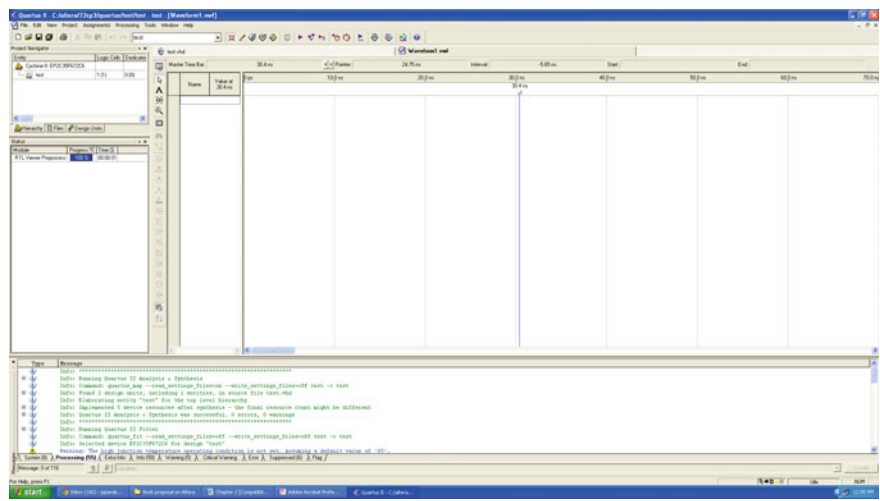


Fig. 2.11 Window for editing waveform

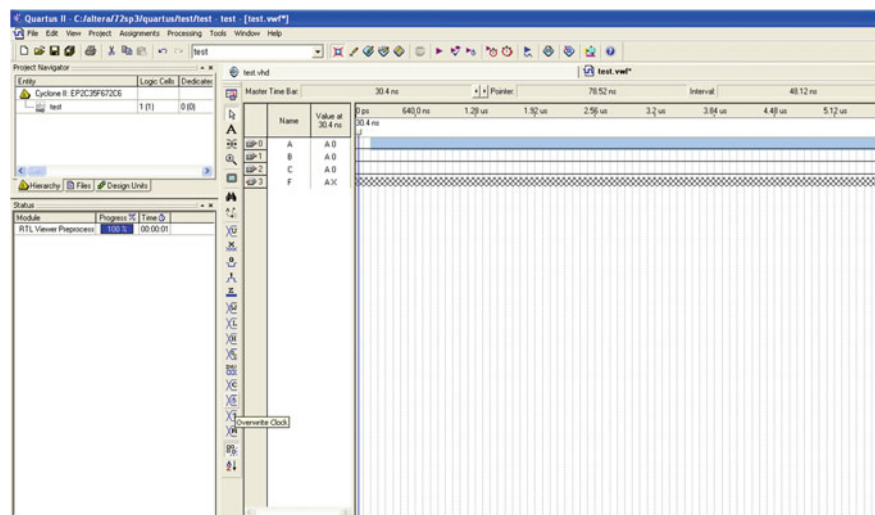
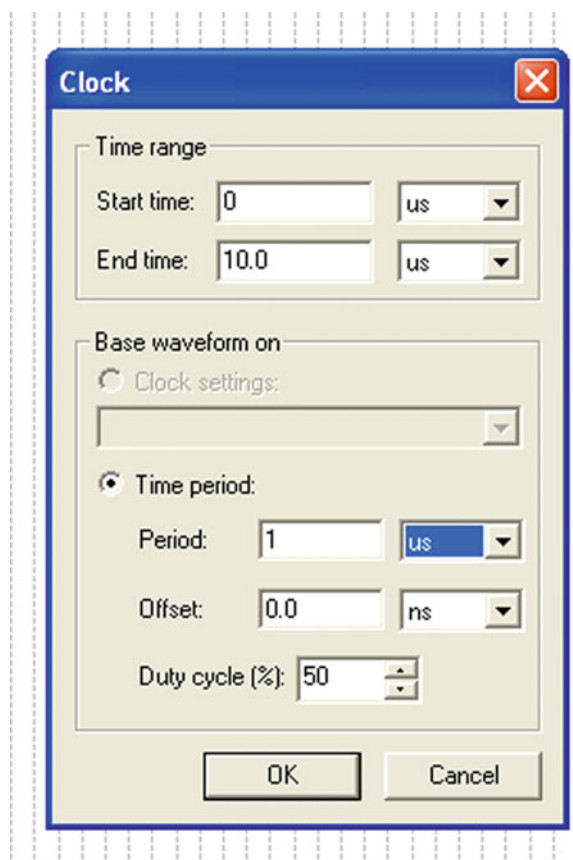


Fig. 2.15 Time period specifying using overwrite clock

Fig. 2.16 Period and start time entry



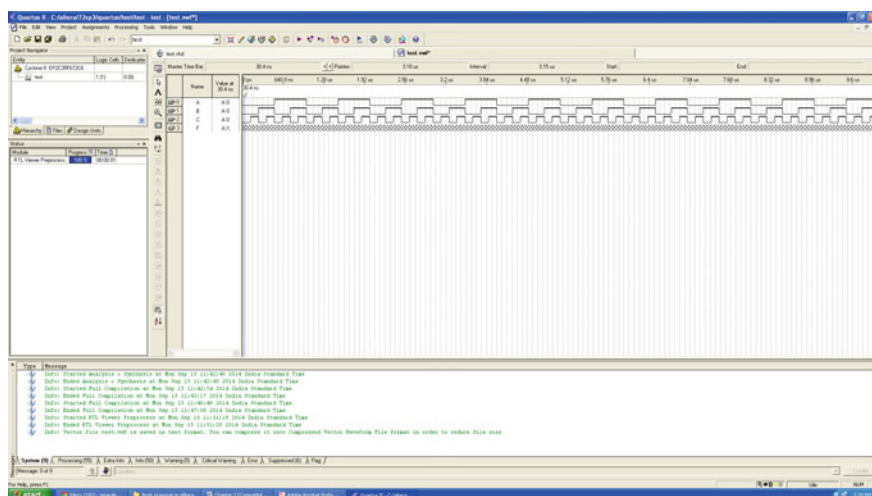


Fig. 2.17 Simulated input waveforms

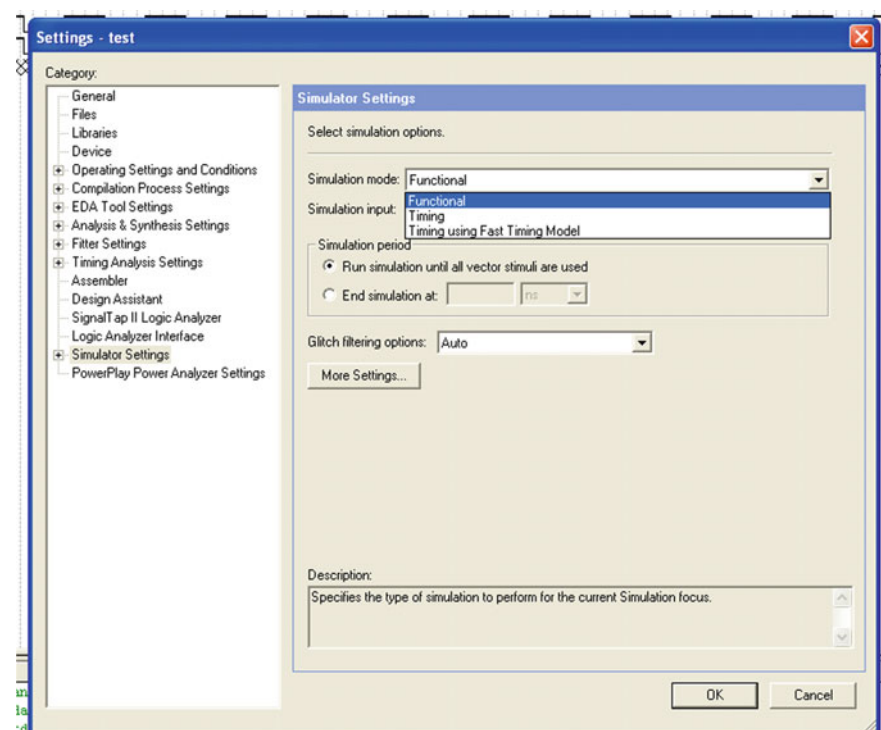


Fig. 2.18 Settings of functional simulation

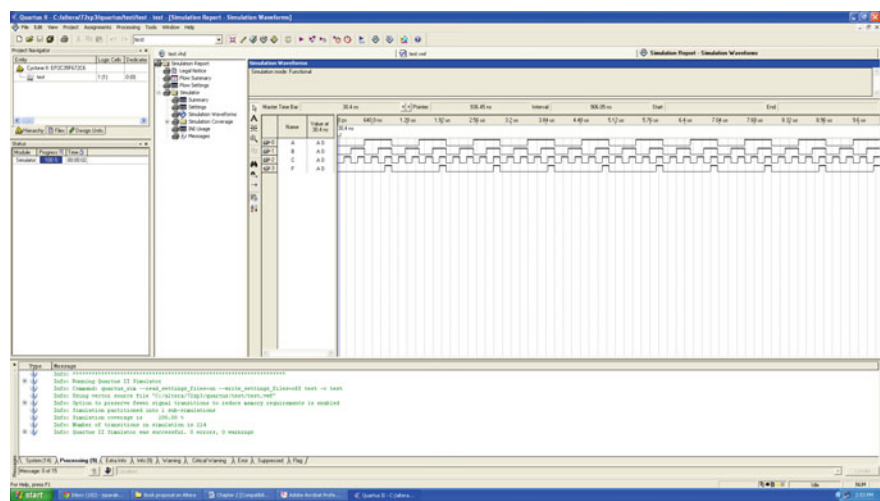


Fig. 2.19 Simulated waveform

- Then click on **Processing** tab → select **Start Simulation**. The final simulated output of three-input AND Gate is shown in Fig. 2.19.

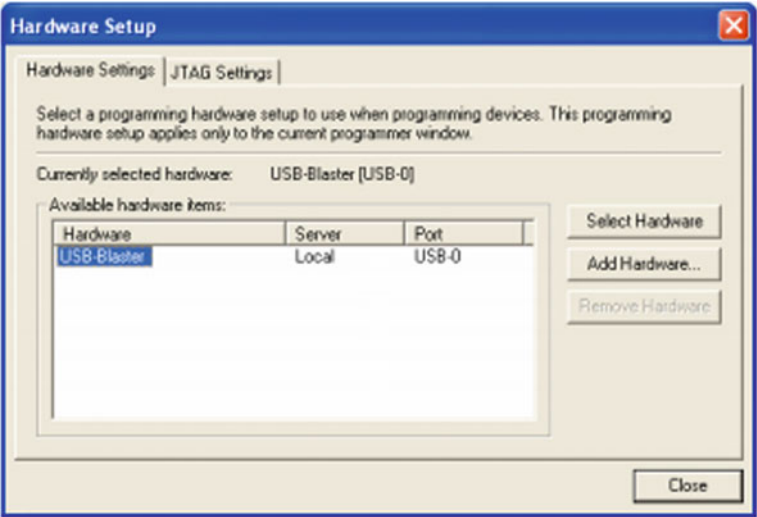
2.5 Programming and Configuring the FPGA Device

To implement the designed system on FPGA, it is necessary to program the FPGA. Altera’s DE-series board supports two different configurations, i.e., JTAG and AS modes. The file containing configuration data is downloaded from host PC to the board by using USB port. To use port connection, one has to install USB-Blaster driver.

FPGA devices are programmed directly by using JTAG mode. If the FPGA is programmed using JTAG mode, then it will retain its configuration as long as the power remains turned on. The configuration data is automatically erased when there is no power. The second configuration mode is active serial (AS); here the device is provided with some memory to load the configuration data file which is later on loaded on the FPGA device upon power-up. The selection between the two modes is made done by RUN/PROG switch on the DE-series board. JTAG configuration mode is selected by RUN position switch, while AS mode is selected by putting switch in PROG position.

Steps for programming and hardware setup

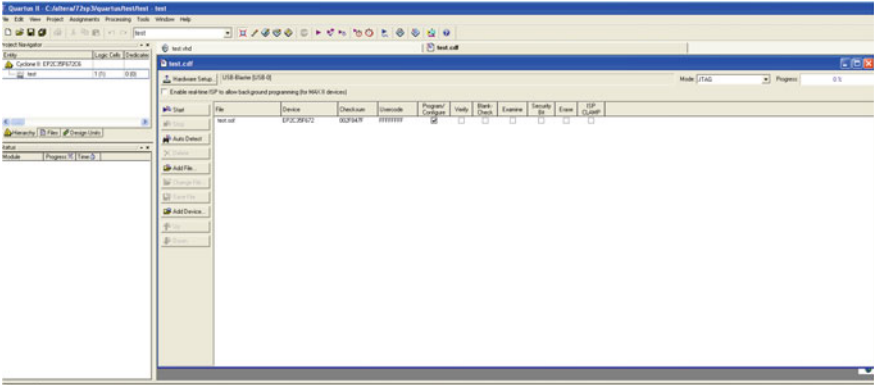
Click on Tools > programmer, the following window shown in Fig. 2.20 appears and one should do the hardware setup before downloading the configuration design file.



4. Select USB-Blaster from the drop-down menu.
5. Then Click on Close.

Following above five steps will complete the USB-Blaster setup.

Next step is to tick mark (✓) the Program/Configure option as shown below and click on start, and this will start the device programming and shows the status of programming on progress bar.



Once the programming is done, then next part is to test the logic onto the DE2 Board.

Hands-on Experience with Altera FPGA Development
Boards

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