

Chapter 2

Background

In this chapter, fundamental knowledge on reliability are discussed, including reliability definition, fault classification and fault models. In the next soft error and its evaluation metrics are elaborated, which is heavily used in the following chapters.

2.1 Reliability Definition

Reliability is in a broad sense one attribute of *dependability*, which describes the ability of the system to deliver its intended service [53]. Reliability measures the capability of *continuous* delivery of *correct* service. Formally, reliability $R(t)$ at time instance t defines the probability that system performs without failure in time range $[0, t]$, provided that system functions correctly at time 0. Reliability is a function of time, where longer time will reduce the system reliability. Another attribute of dependabilities is *availability*. Availability $A(t)$ defines the probability that system performs correctly at time t , which is often used when occurrence of failures is tolerated. For instance, system down time per year in network application is a measure of availability, since short failure time in network is allowed by the users.

2.2 Fault, Error and Failure

The definition of reliability shows its strong relationship with failure, which indicates the occurrence of unexpected behavior of a *system*. The definition of failure differs with the scope of the system. In a software system, the failure can be defined as a wrong value in the program outputs. In a hardware system such as the architecture of a processor, the failure can be interpreted as a mismatch value of the values stored into

memories. Generally, failure is strong correlated with the system under discussion.

Error is a wrong value during *computation*, which is the cause of failure. For instance, error can be viewed from architecture perspective as a logic value which differs the state of the circuits from the correct one. Explicitly, an error occurs when the sequential logic of the circuits exhibits an unexpected value. The sequential logic includes register file and pipeline registers. Not all errors lead to failure. For instance, the erroneous values in register file is overwritten before stored into the data memory. An error in the pipeline register can be ignored when the computation never uses such operand. Generally, errors can result in different effects, such as benign fault, Silent Data Corruption (SDC), Detected Unrecoverable Error (DUE) and system crash. The author in [210] illustrates various system-level effects of error.

Fault from hardware perspective is the *physical* defect or temporal malfunctions, which is the cause of error. Fault can be also defined from software perspective such as a bug in the program due to incorrect specification or human mistakes. The book concentrates on hardware related faults. Not all faults can result in errors. Generally, four masking mechanisms prevent the faults in outputs of combinatorial gates from forming errors in the storages:

- **Electrical Masking:** The fault in the form of current pulse attenuates its electrical strength during the propagation through logic network. The duration of the pulse increases while the amplitude decreases. When the pulse reaches the sequential logic, the attenuated amplitude may not be strong enough to be launched into the storage cell. A technique to model electrical masking is presented in [140].
- **Logic Masking:** Combinatorial logic has its intrinsic masking ability. For instance an 2-to-1 AND gate which has one input of value zero, will mask the fault on the other input.
- **Timing Masking:** The faulty current pulse propagates to the input of sequential logic with enough strength. However, it can not be latched into the flip-flop since it does not arrive within the timing window for data latching. The timing window is the sum of setup and hold time of the flip-flop [7].

2.3 Hardware Faults

2.3.1 Origins

2.3.1.1 Transient Fault

Transient fault, which are often named as soft fault or glitches, is temporal hardware fault which keeps active for a limited time duration. Transient fault is no longer present when its driving source disappears. The causes of radioactive related transient faults can be alpha particles, cosmic arrays and thermal neutrons. When such particles strike the transistors, electron-hole pairs are formed and collected by the transistor's source and drain area. Once the charges are stronger enough, a current pulse occurs

and can potentially flip the value of the memory cell, which resulted in a *Single Event Upset* (SEU) or produce glitches named *Single Event Transient* (SET) to the logic output. The smallest amount of charge to cause the SEU is called *critical charge* Q_{crit} . Higher Q_{crit} will reduce the probability of SEU, however, also reduce the speed of the logic transition for the circuits.

- **Alpha Particle** consists of two protons and two neutrons. They are usually from radioactive nuclei during their decay. The emitters of alpha particles are usually the impurities in the device package, which can potentially affect the active region. As the progress of packaging technologies such as 3D packaging, the active region has become very close to the solder bumps so that alpha particles with low energy can also cause transient faults.
- **Cosmic Rays** are the main source of transient faults for chips applied in terrestrial domain. Cosmic array is a high energy neutron flux, whose density is mainly determined by altitude and locations. Neutrons are uncharged particles which do not interact with charged electrons or holes. Consequently they are highly penetrating and cause low protection efficiency by shielding. Recently, SEU caused by cosmic array are increasingly reported, even at ground conditions [55].
- **Thermal Neutrons** In contrast to the high energy neutrons from cosmic rays, thermal neutrons are the terrestrial neutron flux from the surrounding environment. Recently, the circuits become sensitive to the thermal neutron flux due to the appliance of boron-based glasses in manufacturing [50].

2.3.1.2 Permanent Fault

Permanent faults refer to the faults which are unrecoverable. For CMOS technology they can be classified as extrinsic and intrinsic faults. Extrinsic faults are caused during device manufacturing by contamination or burn-in testing. Intrinsic faults are directly related to the CMOS ageing effects, where the performance of device degrades through time. Several ageing effects are briefly reviewed as following.

- **Electromigration (EM)** refers to the mechanism that causes void region in metal lines or devices, which prevents the further movement of electrons. Electrons hit the metal atoms during the movement through metal wires. With sufficient momentum of the electrons, the atoms can be displaced in the direction of electron movement. High temperature increases the momentum of electrons which leads to faster displacement of atoms. Such mechanism finally result in a void region in the metal wire.
- **Hot Carrier Injection (HCI)** degrades the maximal operating frequency of the chip. HCI originates from the ionization effect when the electrons in the channel hit the atoms around the drain-substrate interface. The electron-hole pairs with sufficient energy, which are caused during ionization, can potentially enter the oxide to occur damage. Such effect raises the threshold voltage of transistor and reduces the operating frequency by 1–10% during the device lifespan of 15 years.

- **Negative Bias Temperature Instability (NBTI)** also degrades operating frequency by increasing the threshold voltage of PMOS transistor. The negative bias under high temperature cause the stress to the PMOS transistor, which results in the breaking of silicon-hydrogen bonds in the oxide interface. The free hydrogen atoms create traps at oxide-channel interface by combining with oxygen or nitrogen atoms. This finally leads to the reduction in holes mobility and negative shift of PMOS threshold voltage. NBTI is predicted to be the most critical ageing effect for CMOS technology under 45 nm technology [19].

2.3.2 Fault Models

To investigate the effects of physical faults on higher level of design abstractions, faults are usually modelled with predefined behaviors. Several prevalent fault models are presented in the next. In practice, the effects of physical fault are modelled using the combination of different fault models below.

- **Stuck-at Fault** is used to model the effect when the memory cells or logic gates permanently stuck at the logic value zero or one. Stuck-at faults are the most common type of fault model.
- **Single Bit-flip Fault** is used to model the transition of logic value to another value. It can be classified as simple bit-flip, where the logic value changes when the fault is injected, and bit-flip within the time window, where the value flips back to its original value after the duration of the fault.
- **Multiple Bit-flip Fault** is used to model the simultaneous change of logic values for multiple bits. It can also model the coupling fault, such as short between multiple logic cells or wires.

2.4 Soft Error

Most of the work in this book focuses on analysis and tolerance of transient faults, which manifest into soft errors. Soft error is a synonym of SEU, which represents the bit-flip of logic value in a memory cell or flip-flop. It results from either the strike of radioactive particles in the memory/flip-flop cell or the latched erroneous value from SET of logic faults. According to the location of errors effected by the fault, SEU can be further classified as Single Bit Upset (SBU), Multiple Bit Upset (MBU) and Multiple Cell Upset (MCU) [94]. Recently, MBU and MCU become important threats for nanoscale technologies [88]. In this section, the evaluation metrics for soft error and its scaling trend are introduced.

2.4.1 Evaluation Metrics

- **Mean-Time-to-Failure (MTTF)** represents the average time between two errors or failures. Assume n components exist in the system, the system MTTF is computed from MTTF from individual component using:

$$MTTF_{sys} = \frac{1}{\sum_{i=1}^n \frac{1}{MTTF_i}} \quad (2.1)$$

- **Failure-in-Time (FIT)** FIT with is more favorable than MTTF since it is additive in computation. One FIT indicates an error within 10^9 hours. If the components in the system are independent, the system FIT is the addition of FIT for individual components using:

$$FIT_{sys} = \sum_{i=1}^n FIT_i \quad (2.2)$$

FIT is a typical representation of Soft Error Rate (SER).

2.4.2 Scaling Trends

The drastic reduction of technology size and supply voltage has significant impact on SER of different components. The SER scaling trends for SRAM, DRAM (Fig. 2.1a and b) and combinatorial logic (Fig. 2.2) are presented.

- **SRAM** has a flat decreasing SER trend as technology scales. This is due to the fact that both Q_{crit} of the SRAM cell and the cell area for the particles to strike

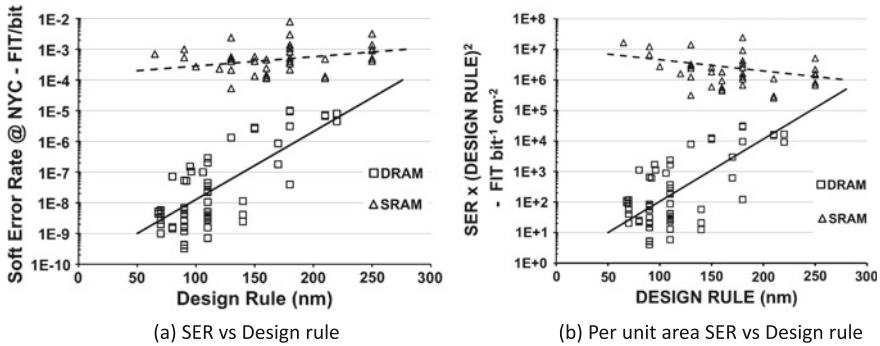
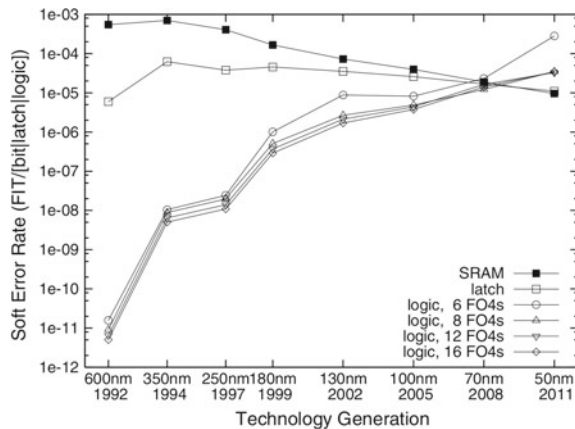


Fig. 2.1 SER scale trend for SRAM and DRAM [177] Copyright ©2010 IEEE

Fig. 2.2 SER scale trend for combinatorial logic [172]
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decrease, which leads to a saturation for the SRAM SER. Figure 2.1b also shows the SRAM SER per unit area indicating the per chip SER, which is even increasing. Another trend shows the fast increment of MCU, where the ratio of MCU to SBU grows from a few percent at 250 nm to 50% at 22 nm [89]. The work in [66] also investigates the MBU rate for 65 nm.

- **DRAM** reduces its SER significantly for new technologies. The reason is that with reduced cell area, the Q_{crit} for DRAM cell remains roughly constant, which makes the particles difficult in upsetting the cell. DRAM vendors achieve this by implementing deeper trenches, more tracks and larger capacitors.
- **Combinatorial logic** Fig. 2.2 shows the predicted trend of logic SER rate from Shivakumar [172] from 600nm till 50nm technology, where the logic SER approaches SRAM. The SER is also predicted to increase with running frequency. Such prediction is based on simulation, where recent work in [68] presents that the logic SER is below 30% of nominal latch SER for 32 nm fabricated chips.

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