

Chapter 2

Review of the PWM Control Circuits for Power Converters

2.1 Voltage-Mode Control Circuit for Power Converters

Power converters are electrical control circuits that transfer energy from a DC voltage source to the output loading and regulate the output voltage to meet the user design. Energy is transferred via electronic switches made with transistors and diodes to an output filter and then transferred to the output loading.

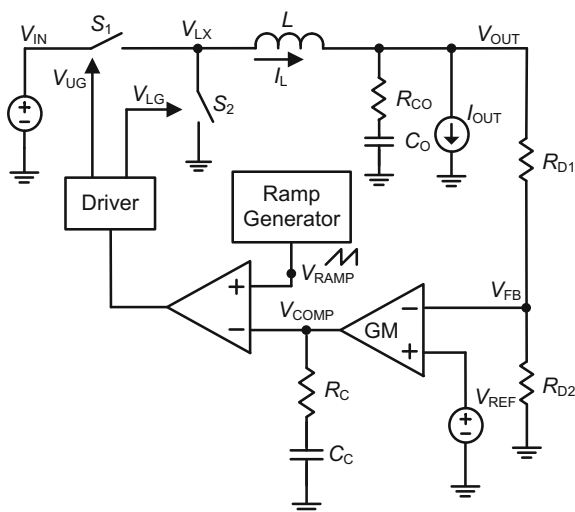
These converters employ square-wave PWM to achieve voltage regulation. The output voltage is regulated by varying the duty cycle of the power semiconductor switch driving signal. The voltage waveform across the switch and at the input of the filter is a square wave in nature and generally results in high switching losses when the switching frequency is increased. However, these converters are easy to control, are well understood, and have a wide load control range. These converters also operate at a fixed-frequency, variable duty cycle. This type of control signal is called PWM control signal. Depending on the duty cycle, these converters can operate in either CCM or discontinuous conduction mode (DCM). If the current through the output inductor never reaches zero, then the converter operates in CCM. If the current through the output inductor reaches zero, then the converter operates in DCM.

The output voltage is equal to the average value in the switching cycle of the voltage applied at the output filter. For real switches with parasitic elements, efficiency depends on conduction and switching losses, but the efficiency of power converters remains higher than that of linear regulators such as LDO.

Power converters are widely applied in portable electronic equipment and products, especially those designed to reduce standby power loss. They demonstrate high efficiency and present a fast transient response due to system design. The fixed-frequency PWM control scheme for power converters [1–24] is commonly used with current-mode and voltage-mode control circuits.

Voltage-mode control circuit is the simplest circuit structure for PWM control scheme for power converters. The major characteristic of this design is the presence

Fig. 2.1 Circuit diagram of the voltage-mode control circuit for buck converter



of a single voltage feedback path, with PWM performed by comparing the voltage error signal with a constant ramp waveform. Current limiting must be conducted separately. The advantages of voltage-mode control are as follows: the single feedback loop is easy to design and analyze and a large-amplitude ramp waveform provides good noise immunity for a stable modulation process. Figure 2.1 shows the circuit diagram of the voltage-mode control circuit for buck converter. S_1 and S_2 are the power switches integrated on-chip, L is the output inductor. R_{CO} is the ESR of output capacitor C_O . Current source I_{OUT} is the output load current. The driver circuit uses the input signal on-time width to generate two control signals V_{UG} and V_{LG} , these two signals should be avoided to turn on at the same time, because this operation makes this system to have a shoot-through problem. The compensator of R_C and C_C should be designed for optimization to increase the transient response. Only the feedback signal V_{FB} and reference voltage V_{REF} are built inside the IC. The output signal of the comparator depends on the input signals V_{COMP} and V_{RAMP} results.

The PWM three-terminal model [23, 24] is a good tool to analyze loop stability because power switches S_1 and S_2 can be modeled as equivalent circuits similar to a dependent voltage source, a dependent current source, and an ideal transformer. The PWM three-terminal model with voltage-mode control circuit for the buck converter is shown in Fig. 2.2. In Fig. 2.2, a transfer function for control-to-output $G_{CTO}(s)$ is obtained with Eqs. (2.1)–(2.7). Based on the $G_{CTO}(s)$ transfer function, the voltage-mode control circuit for the buck converter has one zero and two poles system, as shown in Fig. 2.3. The DC gain of control-to-output depends on the input voltage by Eq. (2.2), and a large input voltage has a large DC gain. The voltage-mode control circuit for the buck converter is unsuitable for a wide input voltage range. The zero S_{Z1} depends on output capacitor C_O and ESR R_{CO} of the output capacitor. With regard to output capacitor selection, tantalum capacitors are

Fig. 2.2 PWM three-terminal model with voltage-mode control circuit for buck converter

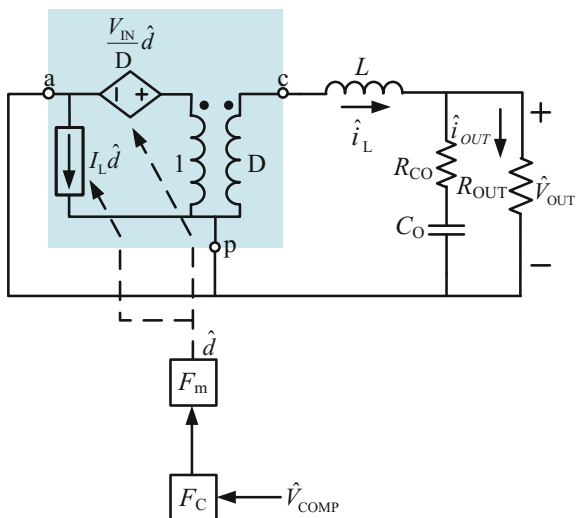
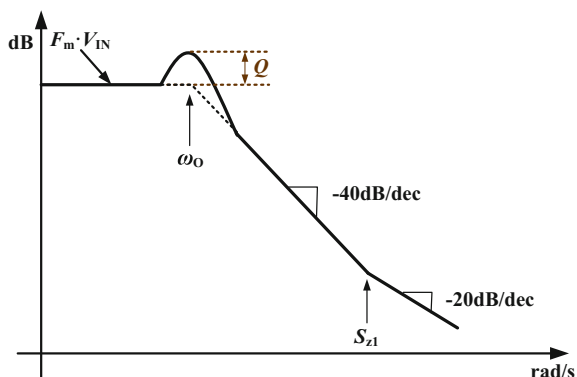


Fig. 2.3 Control-to-output with one zero and two poles system of voltage-mode control circuit for buck converter



a poor choice for output capacitors because tantalum capacitors usually fail to create a short circuit across their terminals, thereby raising the possibility of a fire hazard. Ceramic or aluminum electrolytic capacitors are preferred because they do not have this failure mode. Ceramic capacitors possessing small footprint, low profile, low ESR, low cost, and high reliability are widely used in microprocessor decoupling and power converter filtering applications. Thus, ceramic capacitors are a good choice when the evaluation board area, cost reduction, or component height is considered. The low ESR of ceramic capacitors results in high performance and efficiency but may cause the system loop to become unstable. Generally, the ESR of a ceramic output is less than $10\text{ m}\Omega$, and the S_{Z1} zero location is set at a high frequency of the voltage-mode control circuit for the buck converter. Thus, the control-to-output $G_{CTO}(s)$ is changed to a two poles system.

$$G_{\text{CTO}}(s) = \frac{\hat{V}_{\text{OUT}}}{\hat{V}_{\text{COMP}}} = F_m \cdot V_{\text{IN}} \frac{1 + s/S_{Z1}}{1 + s/(\omega_O \cdot Q) + s^2/\omega_O^2} \quad (2.1)$$

$$G_{\text{CTO}}(0) = F_m \cdot V_{\text{IN}} \quad (2.2)$$

$$\omega_O = \frac{1}{\sqrt{L \cdot C_O}} \quad (2.3)$$

$$Q = R_{\text{OUT}} \cdot \sqrt{\frac{C_O}{L}} \quad (2.4)$$

$$F_m = \frac{1}{V_{\text{RAMP}}} \quad (2.5)$$

$$F_C = 1 \quad (2.6)$$

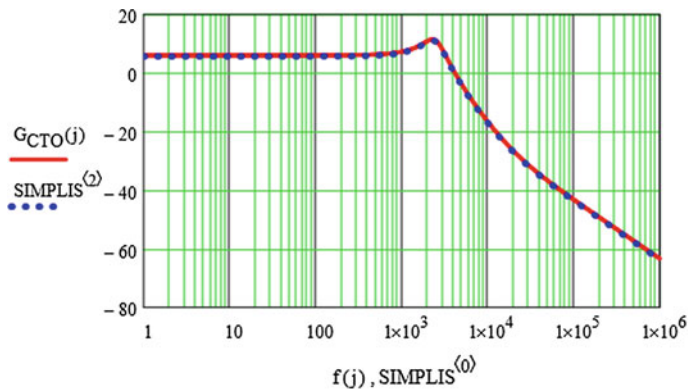
$$S_{Z1} = \frac{1}{C_O \cdot R_{\text{CO}}} \quad (2.7)$$

Table 2.1 lists the operation conditions of the voltage-mode control circuit for the buck converter. According to Table 2.1, the comparison of MathCAD predictions and SIMPLIS simulation results of the open-loop control-to-output bode plot for the buck converter is plotted in Fig. 2.4. In Fig. 2.4, the MathCAD predictions verify the SIMPLIS simulation results. The red-colored line represents the MathCAD predictions, and the blue-colored dot represents the SIMPLIS simulation results. The DC gain curve of the open-loop control-to-output bode plot is equal to 6.02 dB as obtained by Eq. (2.2). The two poles are located at 2.475 kHz by Eq. (2.3). The two poles cause a sharp phase drop of 180°, so the voltage-mode control circuit requires the addition of one zero to cancel the effect of the two poles. Based on these operation conditions using a large output capacitor, the zero is located at 18.09 kHz, so it can help increase the phase degree (30°). In general, the output capacitor uses a ceramic capacitor with high switching frequency, and the capacitance of a single capacitor should be less than 50 μF . Thus, the zero is mainly located at more than 300 kHz with 10 m Ω of ESR. The zero at high frequency cannot help increase the phase degree.

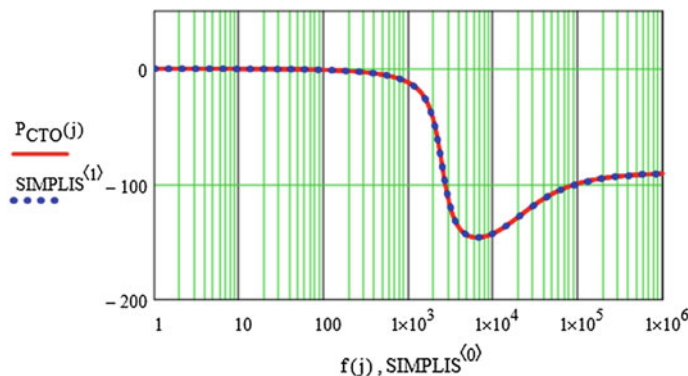
A buck converter can achieve step-down voltage from its input power supply to its output terminal, so it is also widely used to convert a computer's main supply

Table 2.1 Operation conditions in voltage-mode control circuit for buck converter

V_{IN} (V)	4.8 V	F_S (kHz)	500 kHz	L (μH)	4.7 μH
V_{OUT} (V)	1.2 V	R_{D1} (k Ω)	100 k Ω	C_O (μF)	880 μF
I_{OUT} (A)	5 A	R_{D2} (k Ω)	40 k Ω	R_{CO} (m Ω)	10 m Ω
V_{REF} (V)	0.8 V	V_{RAMP} (V)	2.4 V		



(a) Gain



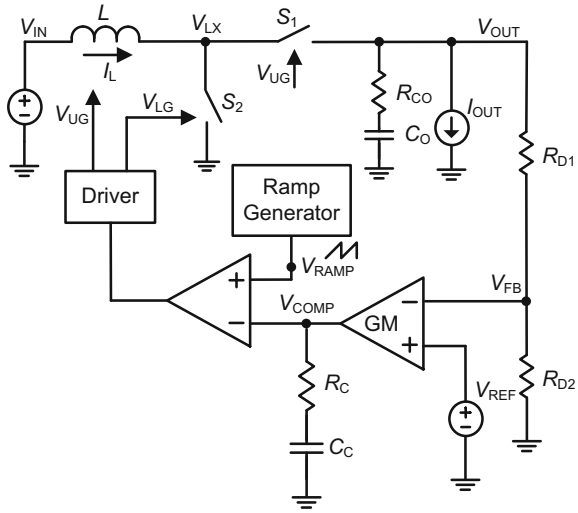
(b) Phase

Fig. 2.4 MathCAD predictions of open-loop control-to-output bode plot for buck converter

voltage (often 12 V) down to lower voltages needed by USB, DRAM, and the CPU (1.8 V or less), or the output voltage is designed to be lower than the input power supply. A boost converter is different from a buck converter because a boost converter achieves step-up voltage from its input power supply to its output terminal; hence, it is widely used to convert a power supply voltage up to larger voltages needed by the display power driver and LED driver, or the output voltage is designed to be larger than input power supply.

Figure 2.5 shows a circuit diagram of the voltage-mode control circuit for boost converter. S_1 and S_2 are the power switches integrated on-chip, L is the output inductor. R_{CO} is the ESR of output capacitor C_O . Current source I_{OUT} is the output load current. The driver circuit uses the input signal on-time width to generate two control signals V_{UG} and V_{LG} , these two signals should avoid to turn on at the same time, because this operation make this system to have a shoot through problem. The compensator of R_C and C_C should be designed an optimization to

Fig. 2.5 Circuit diagram of the voltage-mode control circuit for boost converter



increase the transient response. Only the feedback signal V_{FB} and reference voltage V_{REF} are built inside the IC. The output signal of comparator depends on the input signals V_{COMP} and V_{RAMP} results.

The PWM three-terminal model [23, 24] with the voltage-mode control circuit for the boost converter is shown in Fig. 2.6. In Fig. 2.6, a transfer function for

Fig. 2.6 PWM three-terminal model with voltage-mode control circuit for boost converter

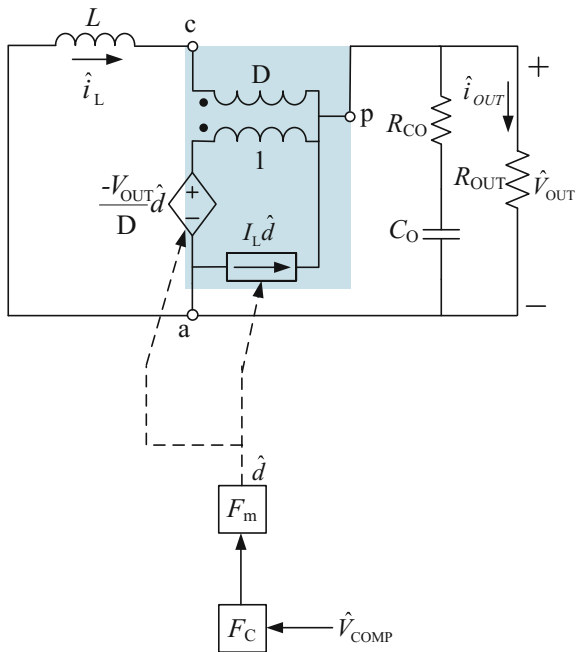
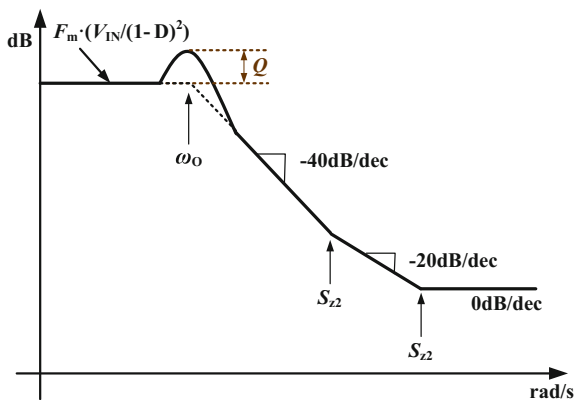


Fig. 2.7 Control-to-output with one zero, one RHP zero, and two poles system of voltage-mode control circuit for boost converter



control-to-output $G_{CTO}(s)$ can be obtained by Eqs. (2.8)–(2.16). Based on the $G_{CTO}(s)$ transfer function, the voltage-mode control circuit for the boost converter has one zero, one right-half-plane (RHP) zero, and two poles system as shown in Fig. 2.7. The DC gain of control-to-output depends not only on the input voltage but also on the duty cycle according to Eq. (2.9). A large duty cycle has a large DC gain. Given this effect, the voltage-mode control circuit for the boost converter is unsuitable for generating very large output voltages. For example, if the duty cycle is 0.9, the DC gain of control-to-output should be increased to 40 dB with the same input voltage. A large DC gain of control-to-output makes it difficult to design an optimal compensator to ensure loop system stability. The first zero S_{Z1} depends on output capacitor C_O and ESR R_{CO} of the output capacitor. Ceramic capacitors possessing a small footprint, low profile, no failure mode, low ESR, low cost, and high reliability are widely used in microprocessor decoupling and power converter filtering applications. The low ESR of ceramic capacitors for output capacitors results in high performance and efficiency but may cause the system loop to become unstable. In general, the ESR of the ceramic output is less than 10 m Ω , and the first zero S_{Z1} location is set at a high frequency of the voltage-mode control circuit for the boost converter. Thus, the control-to-output $G_{CTO}(s)$ is changed to two poles and one RHP zero system. The second zero S_{Z2} is an RHP zero. RHP zero has the same 20 dB/decade rising gain magnitude as a conventional zero, but with a 90° phase lag instead of lead. This characteristic is difficult, if not impossible, to compensate. The designer is usually forced to roll off the loop gain at a relatively low frequency. The crossover frequency may be a decade or more below what it otherwise could be, resulting in severe impairment of the dynamic response. In general, RHP zero is set at a frequency higher than two poles for the boost converter. The RHP zero phase drop starts a decade earlier and negatively affects the potential phase margin of the converter's control loop. This is the nature of instability of a voltage-mode controlled boost converter running in CCM.

$$G_{\text{CTO}}(s) = \frac{\hat{V}_{\text{OUT}}}{\hat{V}_{\text{COMP}}} = \frac{V_{\text{IN}}}{(1-D)^2} \cdot F_{\text{m}} \cdot \frac{(1+s/S_{\text{Z1}}) \cdot (1-s/S_{\text{Z2}})}{1+s/(\omega_{\text{O}} \cdot Q) + s^2/\omega_{\text{O}}^2} \quad (2.8)$$

$$G_{\text{CTO}}(0) = \frac{V_{\text{IN}}}{(1-D)^2} \cdot F_{\text{m}} \quad (2.9)$$

$$\omega_{\text{O}} = \frac{1}{\sqrt{L_{\text{D}} \cdot C_{\text{O}}}} \quad (2.10)$$

$$Q = R_{\text{OUT}} \cdot \sqrt{\frac{C_{\text{O}}}{L_{\text{D}}}} \quad (2.11)$$

$$F_{\text{m}} = \frac{1}{V_{\text{RAMP}}} \quad (2.12)$$

$$F_{\text{C}} = 1 \quad (2.13)$$

$$S_{\text{Z1}} = \frac{1}{C_{\text{O}} \cdot R_{\text{CO}}} \quad (2.14)$$

$$S_{\text{Z2}} = \frac{R_{\text{OUT}}}{L_{\text{D}}} \quad (2.15)$$

$$L_{\text{D}} = \frac{L}{(1-D)^2} \quad (2.16)$$

Table 2.2 lists the operation conditions of the voltage-mode control circuit for the boost converter. According to Table 2.2, the comparison of MathCAD predictions and SIMPLIS simulation results of the open-loop control-to-output bode plot for the boost converter is plotted in Fig. 2.8. In Fig. 2.8, the MathCAD predictions verify the SIMPLIS simulation results. The red-colored line represents the MathCAD predictions, and the blue-colored dot represents the SIMPLIS simulation results. The DC gain curve of the open-loop control-to-output bode plot is equal to 25.666 dB according to Eq. (2.9). The two poles are located at 6.741 kHz by Eq. (2.10). The two poles cause a sharp phase drop of 180°, so the voltage-mode control circuit requires the addition of one zero to cancel the effect of the two poles. Based on this operation condition using the 44 μF output capacitor, the first zero S_{Z1} is located at 361.7 kHz by Eq. (2.14), and the second zero S_{Z2} is located at

Table 2.2 Operation conditions in voltage-mode control circuit for boost converter

V_{IN} (V)	5 V	F_{S} (kHz)	1000 kHz	L (μH)	2.2 μH
V_{OUT} (V)	12 V	R_{D1} (kΩ)	120 kΩ	C_{O} (μF)	44 μF
I_{OUT} (A)	0.3 A	R_{D2} (kΩ)	8.57 kΩ	R_{CO} (mΩ)	10 mΩ
V_{REF} (V)	0.8 V	V_{RAMP} (V)	1.5 V		

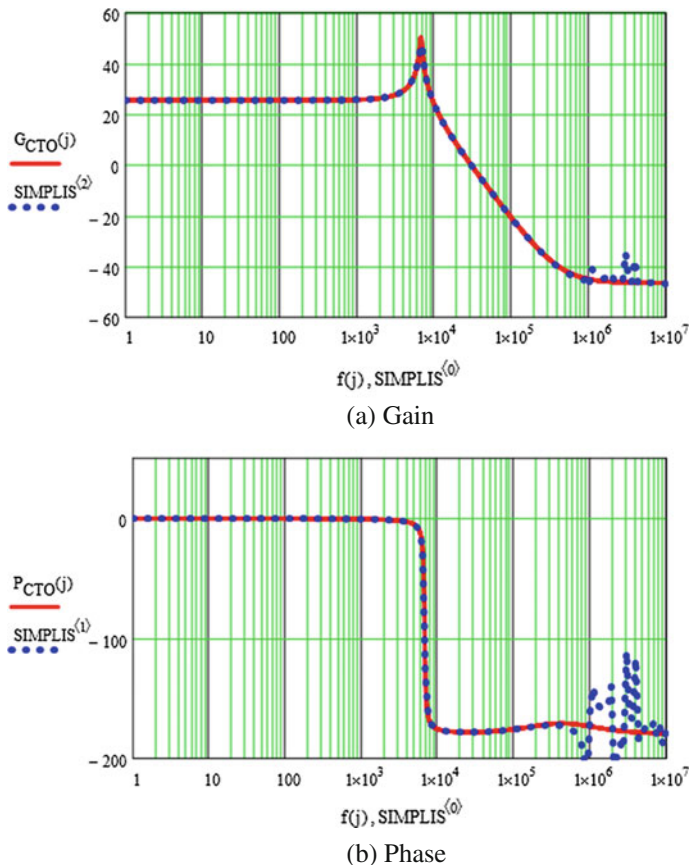


Fig. 2.8 Comparison of MathCAD predictions and SIMPLIS simulation results open-loop control-to-output bode plot for boost converter

502 kHz by Eq. (2.15). Thus, the first zero S_{Z1} can cancel the effect of the second zero S_{Z2} . The phase of open-loop control-to-output maintains a two-pole behavior similar to a sharp phase drop of 180° . Meanwhile, the RHP zero S_{Z2} depends on the output loading and duty cycle, so the user needs to consider an optimal compensator at the worst conditions to ensure that the RHP zero S_{Z2} does not affect the system loop stability.

2.2 Current-Mode Control Circuit for Power Converters

The current-mode control circuit contains two feedback control signals and differs from the voltage-mode control circuit. The output voltage is fed to an error amplifier to generate control signal V_{COMP} . Inductor current I_L is sampled into voltage signal

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