

Performance Analysis of Dual Metal Double Gate Tunnel-FETs for Ultralow Power Applications

D. Gracia and D. Nirmal

Abstract Dual metal double gate tunnel FET device has been presented to overcome the challenges in conventional TFET. This device gives a very good $I_{\text{on}}/I_{\text{off}}$ ratio and an average subthreshold slope. The performance analysis is done for various values of oxide thickness and doping concentrations for the device. It has very low leakage current (9.27×10^{-20} A/ μm), a huge on-current (4.85×10^{-7} A/ μm), $I_{\text{on}}/I_{\text{off}}$ ratio of 10^{12} , and a steep subthreshold slope of 34 mV/dec.

Keywords Dual metal · Tunnel FET · High- k dielectric · Subthreshold slope

1 Introduction

Tunnel field-effect transistors (TFETs) are the upcoming devices for its less leakage current and steep subthreshold slope and are much useful to applications which use less power [1–3]. TFETs are based on the passage of the majority charge carriers and an electric field formed in the channel region which is the switching mechanism for tunneling [2–5]. The conventional TFET is a p-i-n gated structure having non-uniformly doped source and drain, and the carrier passage takes place from one band to another.

The major challenges in TFET are small drive current and ambipolarity. To master these challenges, high- k dielectrics in the double gate TFETs are proposed [6, 7]. It increases on-current and reduces the leakage current, and hence, on-to-off current ratio is increased [6]. Device analogue/RF characteristics are investigated for gate–drain underlap area [8]. The device uses non-local path (BTBT) model for

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simulation. Due to the tunneling process, the device requires a fine mesh around area where the switching mechanism takes place. In [9], the tunneling takes place from the source to drain depletion regions. The paper [10] discusses the device electrostatic role of three diverse TFET structures, i.e., tunnel FET with two gates, tunnel FET with different dielectrics, and tunnel FET with two metals with different dielectrics. The latter excels the other two TFET structures.

Several structures are proposed by the researches to enhance the on-current of the TFET. In [11–15, 16] dual-gate tunnel FET with different junction for applications that consumes less power is discussed. Vertical TFET with n- and p- type source underlapped structure with submicron 10-nm technology is discussed [17]. In [18], junctionless tunnel FET and [19] gate all around TFET have been discussed. In [20], a dopingless FET (DL-FET) source/drain (S/D) areas were created by metal work function engineering and show a fine control over short channel effects. The problem of ambipolarity is the device operates for both positive and negative values of gate voltage making the TFETs not suitable for digital circuits. Several techniques [21, 22] to control ambipolarity are reducing the drain electric field, reducing the doping concentration, and using large bandgap heterostructures in the drain end. Molybdenum has been shown as a potential candidate for the future metal gate technology in [23–25].

This paper deals with the performance analysis of dual metal double gate TFET for different doping concentrations, and oxide thickness has been analyzed. The dependence of on-current, off-current, SS on device parameters is studied in detail. Section 2 covers the structure design and simulation. Section 3 summarizes the findings and discussion. Section 4 provides the conclusion followed by acknowledgment and references.

2 Structure Architecture and Parameter Description

In Fig. 1, the 2-D structure of double metal dual-gate TFET is shown. The structure creation and the simulations are performed using Sentaurus Technology Computer-Aided Design (TCAD) software [26]. The gate oxide thickness (T_{ox}) is 2 nm with channel thickness of 10 nm. Molybdenum and aluminum are used as metal with the minimum energy of 4.4 and 4.0 eV, respectively. In addition to conventional SiO_2 , high- k dielectric HfO_2 is used as gate oxides. The source region is heavily doped with p-type material, while the drain is oppositely doped with n-type impurities. The most important models used for simulation are non-local BTBT model, bandgap narrowing model, SRH model. The transfer characteristics of dual metal gate with heterodielectric TFET have been investigated by varying doping concentrations and thickness of gate oxides.

Table 1 gives the structure dimensions. Figure 2 gives the band diagram of the device in its active as well as in off state. The graph is plotted between the energy band and the position along the length of the device. In its put off state, tunneling

Fig. 1 2-D structure of dual metal double gate TFET

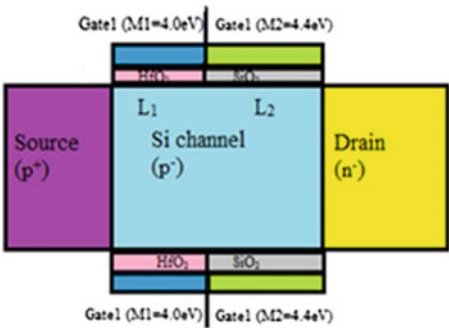
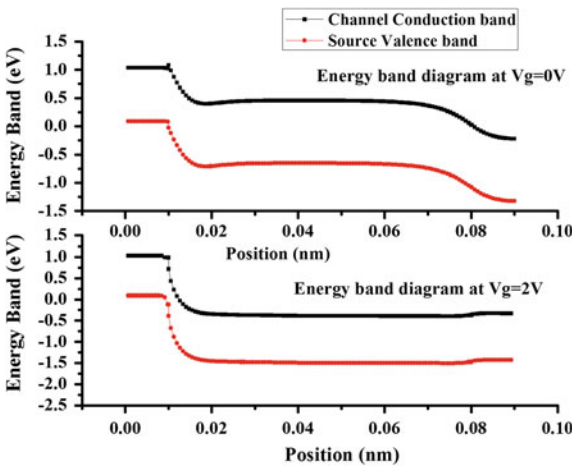


Table 1 Device dimensions

Parameter	Values
Gate length (L_g)	50 nm
Oxide thickness (T_{ox})	2 nm
Channel thickness (T_{si})	10 nm
Source concentration (N_a)	$1e^{20} \text{ cm}^{-3}$
Channel concentration (N_{ch})	$1e^{15} \text{ cm}^{-3}$
Drain concentration (N_d)	$1e^{18} \text{ cm}^{-3}$
Gate voltage (V_g)	2 V
Supply voltage (V_d)	0.5 V

does not occur if the gate bias is very low due to the barrier width between the valence band of the source area and the conduction band of the channel area are high. Furthermore, in the active case, for positive gate bias, the barrier width, a potential boundary leading to tunneling of carriers, is reduced because the gate pulls down the barrier closer to each other.

Fig. 2 Energy diagram of dual metal double gate TFET



3 Results and Discussion

3.1 Transfer Characteristics

Figure 3a gives the dual metal double gate TFET transfer characteristics. The analysis has been carried out by swinging the V_g from 0 to 2 V, and the drain current variation is observed. The simulated on-current of the device is 4.85×10^{-7} , and the leakage current is 9.27×10^{-20} giving a very good I_{on}/I_{off} ratio in the order of 10^{12} for a low supply voltage of $V_{dd} = 0.5$ V. In TFET [27], BTBT is the primary device physics to be modeled. This is fundamental to all lateral BTBT devices. In the simple local BTBT model, the carrier generation rates are determined mainly from the local electric field only [27]. In one common expression, based on the Kane's derivation,

$$G^{BTBT} = A \cdot E^{\alpha} \exp\left(-\frac{B}{E}\right) \quad (1)$$

Figure 3b shows the $I_d - V_d$ of the device. The analysis is carried out by swinging the drain voltage from 0 to 0.7 V for different gate voltages. The drain current is 4.8457×10^{-7} A.

3.2 Steeper Switching Behavior

The subthreshold swing is the variation in voltage that is used in order to provide a change of one order of magnitude of the drain current. Subthreshold swing is given by

$$S = \frac{dV_g}{d(\log I_d)} [\text{mV/dec}] \quad (2)$$

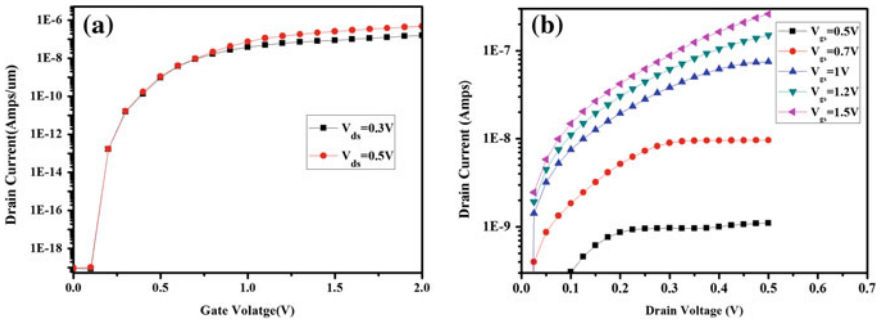


Fig. 3 a $I_d - V_d$ for different V_{ds} , b $I_d - V_d$ for different V_{gs}

The operating mechanism of MOSFET is based on thermionic injection where electrons travel over an energy barrier, which confines the SS by the Boltzmann distribution of charge to 60 mV/decade. For dual metal double gate TFET, sub-threshold swing is 34 mV/decade. Using high- k in gate oxide provides a steeper slope.

3.3 Effects of Various Doping Concentrations

Figure 4 shows the device characteristics for different doping concentrations. Doping concentration is proportional to on-current, and therefore, increasing source doping will enhance the drive current of the device even at low supply voltage, and hence, TFETs are promising candidates to low power applications.

3.4 Effects of Different Oxide Thickness

Figure 5 shows the $I_d - V_g$ for different oxide thickness keeping the supply voltage 0.5 V. Oxide thickness plays a vital role in the tunneling mechanism. According to the Eq. (3), the current in the active state (on-current) will increase by increasing the oxide thickness of the transistor.

$$I_d = \mu_n c_{ox} \frac{w}{l} \left[\left(V_{gs} - V_t \right) V_{ds} - \frac{V_{ds}^2}{2} \right] \quad (3)$$

where mobility is given by μ_n , c_{ox} is the capacitance of the gate oxide, w/l is the scaling parameter.

Fig. 4 $I_d - V_g$ for different doping concentrations

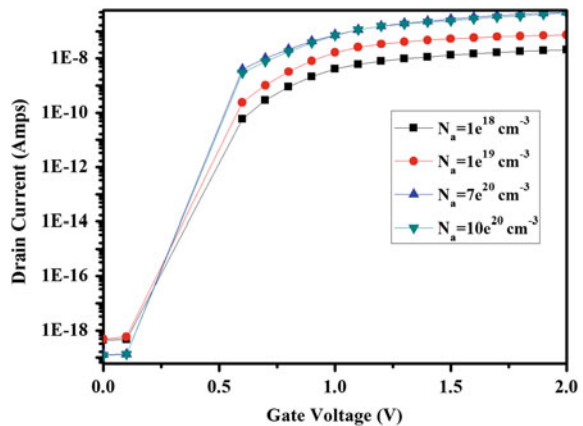
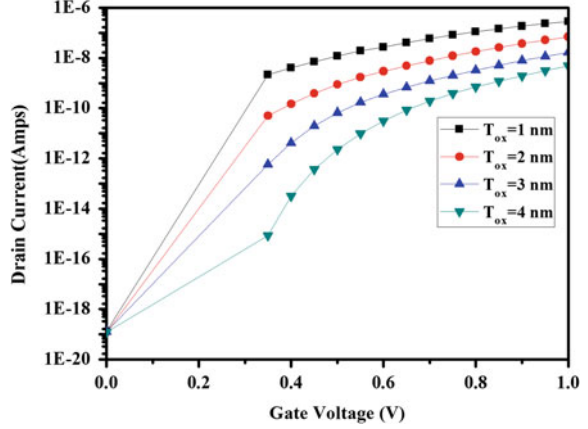


Fig. 5 $I_d - V_g$ for different oxide thickness



where oxide capacitance is given by,

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} \quad (4)$$

4 Conclusion

The dual metal double gate TFET and their characteristics for different device parameter are discussed. This device gives excellent I_{on}/I_{off} ratio of 10^{12} for a very small supply voltage of 0.5 V. Drive current can be increased by increasing the doping concentration and by using thin gate oxide. The dual metal double gate TFET device is a good candidate for applications that use less power. This work can be extended further by using Ge and III–V materials to enhance the mobility.

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References

1. Seabaugh, A.C., and Q. Zhang. 2010. Low-voltage tunnel transistors for beyond CMOS logic. *Proceedings of the IEEE* 98 (12): 2095–2110.
2. Choi, W.Y., B.G. Park, J.D. Lee, and T.J.K. Liu. 2007. Tunneling field-effect transistors (TFETs) with subthreshold swing (SS) less than 60 mV/dec. *IEEE Electron Device Letters* 28 (8): 743–745.

3. Choi, W.Y., and W. Lee. 2010. Hetero-gate-dielectric tunneling field-effect transistors. *IEEE Transactions on Electron Devices* 57 (9): 2317–2319.
4. Ghosh, Bahniman, and Mohammad Waseem Akram. 2013. Junctionless Tunnel Field Effect Transistor. *IEEE Electron Device Letters* 34: 584–586.
5. Gandhi, Ramathan, Zhixian Chen, and Navab Singh. 2011. CMOS Compatible Vertical Silicon nanowire GAA p-type TFET with ≤ 50 mV/dec Sub threshold Swing. *IEEE Electron Device Letters* 32: 1504–1506.
6. Boucart, K., and A.M. Ionescu. 2007. Double-gate tunnel FET with high- κ gate dielectric. *IEEE Transactions Electron Devices* 54 (7): 1725–1733.
7. Charles Pravin, J., D. Nirmal, P. Prajoun, and J. Ajayan. 2016. Implementation of nanoscale circuits using dual metal gate engineered nanowire MOSFET with high-k dielectrics for low power applications. *Physica E Low-Dimensional Systems and Nanostructures* 83: 95–100.
8. Vijayvargiya, V.B.S., P. Singh Reniwal, and S.K. Vishvakarma. 2016. Analogue/RF performance attributes of underlap tunnel field effect transistor for low power applications. *Electronics Letters* 52 (7): 559–560.
9. Prabhat, Vishwa, and Alope K. Dutta. 2016. Analytical surface potential and drain current models of dual-metal-gate double-gate tunnel-FETs. *IEEE Transactions on Electron Devices* 63 (5): 2190–2196.
10. Upasana, Rakhi Narang, Manoj Saxena, and Mridula Gupta. 2015. Modeling and TCAD assessment for gate material and gate dielectric engineered TFET architectures: circuit-level investigation for digital applications. *IEEE Transactions on Electron Devices* 62 (10): 3348–3356.
11. Ahish, Shylendra, Dheeraj Sharma, Yernad Balachandra Nithin Kumar, and Moodabettu Harishchandra Vasantha. 2016. Performance enhancement of novel InAs/Si hetero double-gate tunnel FET using gaussian doping. *IEEE Transactions on Electron Devices* 63 (1): 288–295.
12. Ajayan, J., and D. Nirmal. 2015. A review of InP/InAlAs/InGaAs based transistors for high frequency applications. *Superlattices and Microstructures* 86: 1–19.
13. Sharma, A., A. Goud, and K. Roy. 2015. GaSb-InAs n-TFET with doped source underlap exhibiting low subthreshold swing at sub-10-nm gatelengths. *IEEE Electron Device Letters* 35 (12): 1221–1223.
14. Knoch, J., and J. Appenzeller. 2010. Modeling of high-performance p-type III–V heterojunction tunnel FETs. *IEEE Electron Device Letters* 3 (4): 305–307.
15. Verhulst, A.S., W.G. Vandenberghe, K. Maex, S. De Gendt, M. Heyns, and G. Groeseneken. 2008. Complementary silicon-based heterostructure tunnel-FETs with high tunnel rates. *IEEE Electron Device Letters* 29 (12): 1398–1401.
16. Jain, Prateek, Vishwa Prabhat, and Bahniman Ghosh. 2015. Dual metal-double gate tunnel field effect transistor with mono/hetero dielectric gate material. *Journal of computational electronics* 14 (2): 537–542.
17. Kim, Jang Hyun, Sang Wan Kim, Hyun Woo Kim, and Byung-Gook Park. 2015. Vertical type double gate tunnelling FETs with thin tunnel barrier. *Electronics Letters* 51 (9): 718–720.
18. Ghosh, B., and M.W. Akram. 2013. Junctionless tunnel field effect transistor. *IEEE Electron Device Letters* 34 (4): 584–586.
19. Lee, J.S., J.H. Seo, S. Cho, J. Lee, S. Kang, J. Bae, E. Cho, and I.M. Kang. 2013. Simulation study on effect of drain underlap in gate-all-around tunneling field-effect transistors. *Current Applied Physics* 13: 1143–1149.
20. Jagadeesh Kumar, M., and Sindhu Janardhanan. 2013. Doping-less tunnel field effect transistor: design and investigation. *IEEE Transactions on Electron Devices* 60: 3285–3290.
21. Nigam, Kaushal, Pravin Kondekar, and Dheeraj Sharma. 2016. Approach for ambipolar behaviour suppression in tunnel FET by workfunction engineering. *Micro & Nano Letters* 11 (8): 460–464.

22. Anghel, Costin, Anju Gupta Hraziaa, Amara Amara, and Andrei Vladimirescu. 2011. 30-nm tunnel FET with improved performance and reduced ambipolar current. *IEEE Transactions on Electron Devices* 58 (6): 1649–1654.
23. Kwasnick, R.F., E.B. Kaminsky, P.A. Frank, G.A. Franz, R.J. Saia, K.J. Polasko, and T.B. Gorczya. 1988. An investigation of a molybdenum gate for submicrometer CMOS. *IEEE Transactions on Electron Devices* 35 (9): 1432–1438.
24. Saurabh, S., and M.J. Kumar. 2011. Novel attributes of a dual material gate nanoscale tunnel field-effect transistor. *IEEE Transaction Electron Devices* 58 (2): 404–410.
25. Lee, J.S., et al. 2003. Low-frequency noise characteristics of ultrathin body p-MOSFETs with molybdenum gate. *IEEE Electron Device Letters* 24 (1): 31–33.
26. TCAD Sentaurus Device Manual. 2010. *Synopsys Inc.* CA, USA: Mountain View.
27. Shen, C., L.T. Yang, E.-H. Toh, C.-H. Heng, G.S. Samudra, and Y.-C. Yeo. 2009. A new robust non-local algorithm for band-to-band tunneling simulation and its application to tunnel-FET. *Solid-State Electronics* 57 (1): 23–30.

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