

A Preliminary Study of Oscillators, Phase and Frequency Detector, and Charge Pump for Phase-Locked Loop (PLL) Applications

R. Prithiviraj and J. Selvakumar

Abstract The great advancement in CMOS technology, high speed and frequency, low jitter, low noise and phase noise, and less expensive phase-locked loop are very important in transceiver fields. This work aims at reviewing the performance of oscillators, phase and frequency detector (PFD), and charge pump (CP) for type-I PLL. In this work, the oscillators are reviewed as voltage-controlled oscillators (VCOs) and coherent-based phase-locked synchronous oscillator (CPSO). The phase and frequency detector is evolved as XOR gate PFD, double edge-triggered PFD, and digital pulse amplifier. The condition for stable operation and low-phase noise is established. The different types of oscillators and PFDs are reviewed. A detailed analysis of various methods to design oscillator, phase and frequency detector is provided. The best method to design phase and frequency detector is digital pulse amplifier. It minimizes the dead zone and phase error that can be easily recognized by flip-flop which is type D, and this amplifier has AND gates and is connected in series to raise the pulse width. The best method to design an efficient oscillator is the coherent phase-locked synchronous oscillator from various oscillators under study. It provides a method for improved frequency and lock-in range, capture range over the other oscillators. It retains the normal oscillator characteristics with less phase shifts across the frequency tuning and locking range.

Keywords Phase and frequency detector • Coherent phase-locked synchronous oscillator • Phase error

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1 Introduction

Phase-locked loop (PLL) is a feedback system which follows negative feedback that compares the output frequency and phase with the input frequency and phase. It is widely used in frequency multiplier, frequency synthesizer, clock recovery, high-speed communication, clock generation, spread spectrum, clock distribution, jitter, noise reduction, deskewing, and high-speed communication systems [1]. The history of PLL goes long back to 1918 by the invention of superheterodyne. But there are high number of tuned stages as drawback. During 1930s, there were many experiments trying to compare the frequency of oscillator with input of phase detector, the results are led to the introduction of PLL by Henri de Bellesize [2]. In analog transceivers, PLL is locked to synchronized pulses in the broadcast signal. Since the PLL has been keeping on improving with lot of researches and advancement in various constraints of PLL such as lock-in range, hold in range, capture range, acquisition range, loop bandwidth, phase noise, and jitter. There are several variations of PLL. They are analog PLL (all blocks are analog), digital PLL (digital phase detector, analog VCO), all-digital PLL (ADPLL) (all blocks are digital), software PLL (all working blocks are implemented by software rather than specified hardware). This paper consists of 5 sections. Sect. 2 gives prior work of PLL, Sect. 3 gives overview of Digital PLL architecture, Sect. 4 gives modeling of PLL, and Sect. 5 presents conclusion.

2 Prior Work of PLL

The basic PLL has three building blocks, namely phase and frequency detector, loop filter, and voltage-controlled oscillator (VCO) [1]. The phase difference between the input signal and feedback signal is sensed by a phase and frequency detector, which changes the control voltage of VCO to make its feedback (or) output signal equal to the input signal. The operating states of PLL are unlocked, capture, and lock state. In unlocked state, PLL will be in open loop, where the VCO operates in natural frequency. In capture, PLL will be in closed loop, where the VCO frequency will be changed to make it synchronized with the input frequency. In lock state, phase noise and phase error are zero.

- In 2007, the linear capacitor is replaced by ferroelectric capacitor in VCO, which produce low cycle to cycle jitter because of its behavior of non-linear dielectric constant [3].
- By auto-correlating jittered signal, the jitter has been reduced. It is called jitter reduction technique [4].
- In 2010, the digital circuitry has been introduced to noise reduction from VCO. This was the first time, the VCO has been implemented using digital-distributed synchronous clock. But the drawback in the system is comparison of the clock

input with feedback clock is difficult due to the inaccuracy of digital to analog converter [5].

- In 2010, the charge pump has been replaced by integral path and proportional path where phase and frequency corrections are done separately. But the phase noise gets added up in both separate paths [6].
- In analog PLL, more number of algorithms has been presented and modeled [7, 8] to generate modeling of mathematical relations in order to verify the level of noise from all the blocks of PLL.

3 Overview of Digital PLL Architecture

A digital PLL consists of components, phase and frequency detector, charge pump, loop filter, and voltage-controlled oscillator. The basic component of phase detector is replaced by phase and frequency detector (PFD), and the PFD produce phase difference which is in the form of digital. The phase difference will be given to charge pump which acts as the control signal. The charge pump will generate the required VCO control voltage through loop filter. In place of voltage-controlled oscillator, the coherent phase synchronous oscillator (CPSO) has been replaced. The basic block-level architecture diagram of PLL is shown in Fig. 1. Different methods used to design these blocks are described in Fig. 1.

A. Phase and frequency detector

A phase detector is a component in DPLL, which produces the phase difference between the inputs, which is linear. Varieties of implementation have been seen in the literature on PFDs. The history of PFD goes long back to EXOR gate-based PFD as shown in Fig. 2. It was used for phase correction. The drawback in EXOR gate implementation is lack of sensitivity to edges.

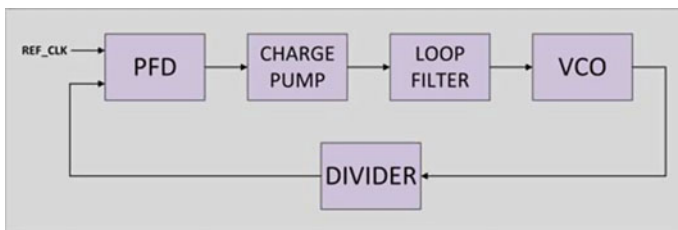
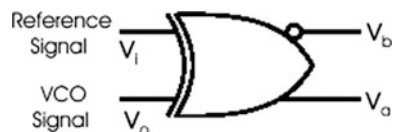


Fig. 1 Block-level architecture of PLL

Fig. 2 EXOR implementation of phase detector



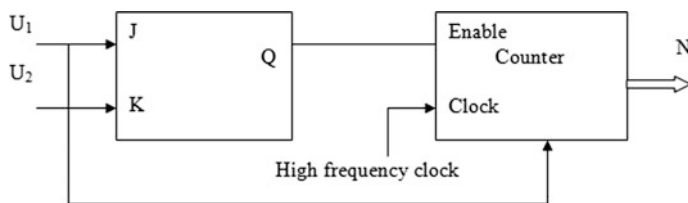


Fig. 3 Phase detector based on edge-triggered JK

This drawback can be overcome by edge-triggered JK operation. The drawback in this method is lack of sensitivity to edges as given in Fig. 3. This edge-triggered JK mechanism belongs to sequential phase detectors where EXOR PFD belongs to multiplier circuits [9].

Then it is improvised and presents the PFD with two-type D flip-flops and an AND gate. By using master slave-type flip-flop, the design specification on rise and fall time of the PLL can be achieved [10]. The phase difference, when it is very small, is very difficult to select. These phase error can get enlarged by using digital pulse amplifier (DPA) [11, 12]. DPA reduces the dead zone as well as fast detectable by D flip-flop. The DPA has AND gates connected in cascade to increase the pulse size (width) [11]. The design of DPA is shown in Fig. 4 [12]. Then after some years, PFD was designed by using Hilbert transform. In Hilbert transform, the input signal has been converted into analytic signal, by using Cartesian to polar conversion, the analytic signal has been converted into phase error.

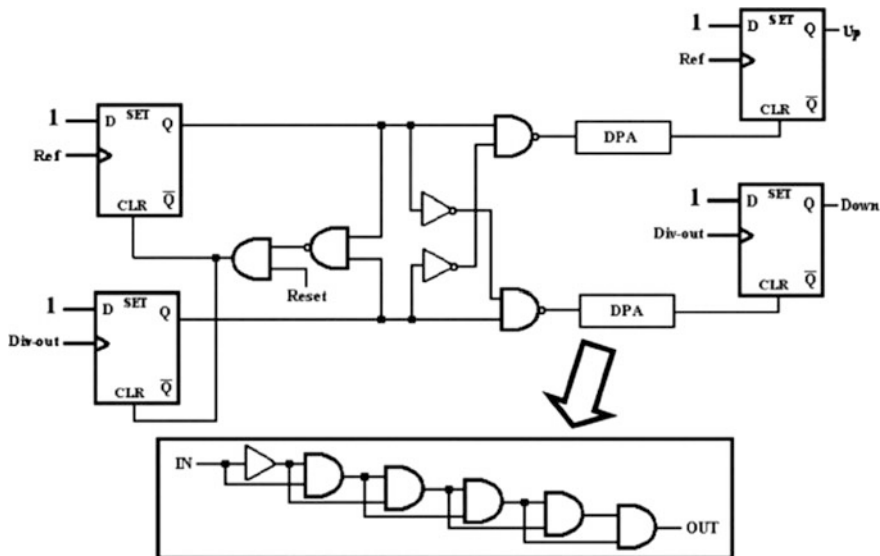


Fig. 4 Digital pulse amplifier

B. Charge pump and loop filter

A charge pump circuit converts digital signal to analog signal, to control the VCO. The PFD outputs, UP and DOWN signals will control the Q2 and Q3 MOSFET switch. When UP goes high, it will charge the Q3 MOSFET, when DOWN goes low, it will discharge the Q2 MOSFET. Q1 and Q4 act as current sources [13, 14]. The charge pump diagram is shown in Fig. 5. The type of loop filter which is chosen for the PLL is important property. The filter which is more suitable for lock time is type-I loop filter. It has low noise immunity [10].

Instead of charge pump, they have used the two types of deglitching filter circuit [15]. The proposed filter circuit will remove glitches from PFD, so that consumption power will be less and produces digital outputs (0, 1) according to the output of PFD [16]. The digital low-pass filter (LPF) is shown in Fig. 6.

C. Proposed Voltage and Controlled Oscillator (VCO)

The VCO is a main block of the PLL, which produce controllable oscillation. There are many types of VCOs. The VCO keeps on evolving with many features like low-power consumption, less area, wide tuning range, less complexity. LC VCO is one of the types of VCO. In [17] frequency-tripling technique in the VCO, with a single cross-coupled pair and dual tank topology, the wideband PLL demonstrated a wide tuning range increased with less power. However, LC-based oscillator has limitations such as high complexity, narrow tuning range, high power consumption

Fig. 5 Charge pump

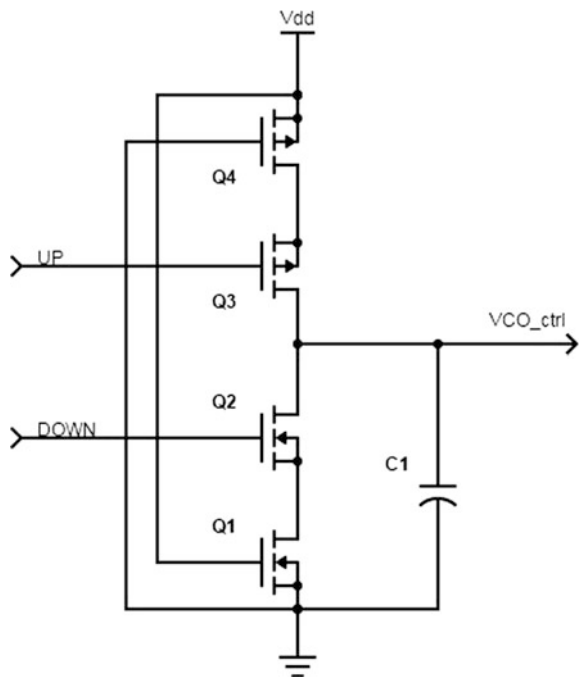
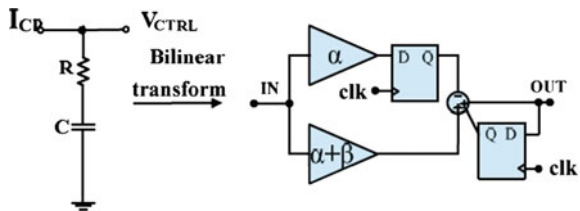


Fig. 6 Logical configuration of digital LPF



and large area [18–21]. The other type of VCO is ring oscillator. In Fig. 7, by using voltage to current converter, the supply current to the inverters is controlled based on the control voltage [22]. The capacitor will reduce the supply noise

The advanced oscillator is coherent-based phase synchronous oscillator (CPSO) [18]. It is shown in Fig. 8. The synchronous oscillator is operated by using the concept of injection locking. It has a basic circuit which consists of a parallel tank and a non-linear negative conductance shown in Fig. 8. V_i represents the signal given into the oscillator and g_m represents the transconductance of the V_i given device. At initial condition, the signal is given into the oscillator, the output is not phase locked to the given signal, which results in a frequency mismatch (Fig. 9). After many cycles, slowly the phase and frequency will be getting locked, the given oscillator is perfectly synchronized with the injected signal as shown in Fig. 10.

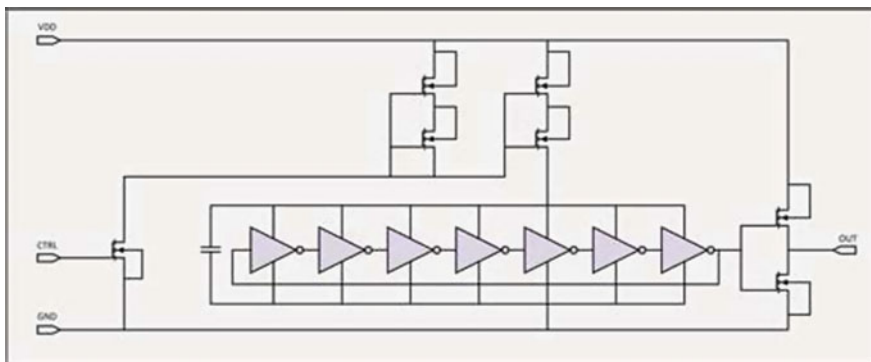


Fig. 7 Ring voltage-controlled oscillator

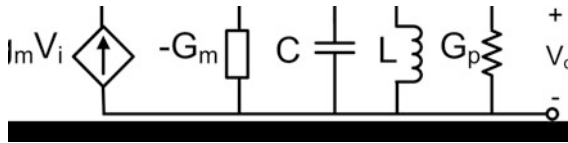


Fig. 8 Negative resistance model of synchronous oscillator

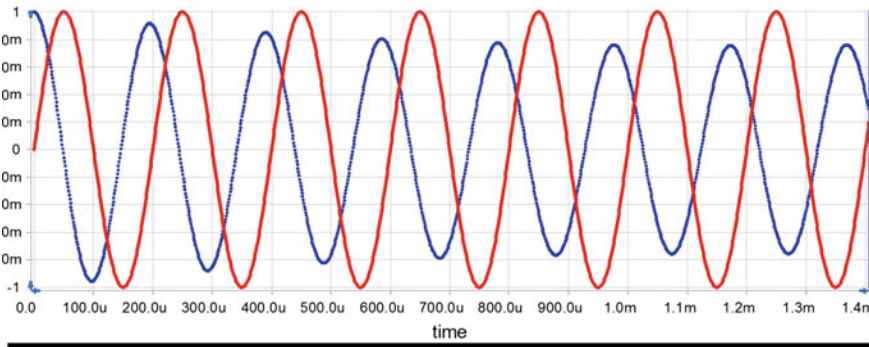


Fig. 9 Unsynchronized initially

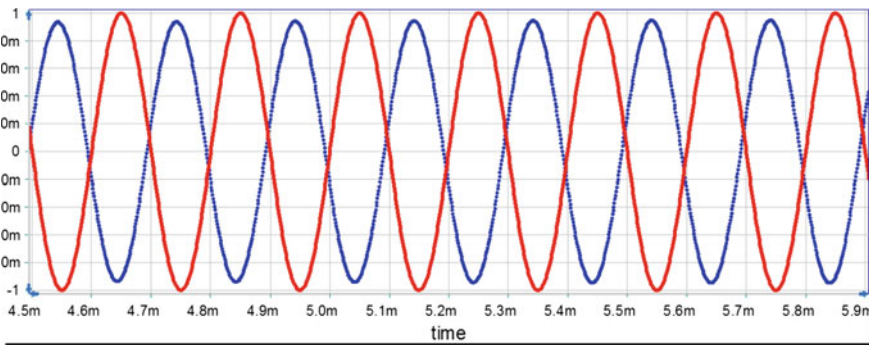


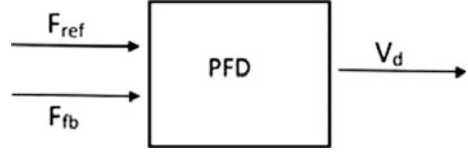
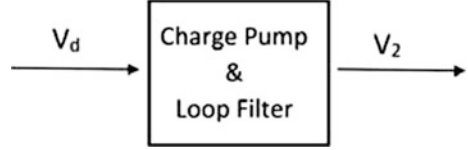
Fig. 10 Synchronized after many cycles

4 Modeling of Basic PLL

Different parameters of PLL like stability, lock-in range, loop bandwidth can be analyzed in phase domain.

D. Phase model of PLL

The PLL consists of three main functional blocks as shown in Fig. 1. The phase parameter and transfer function of PFD (Fig. 11), Charge pump and Loop filter (Fig. 12) and VCO are stated below.

Fig. 11 Phase and frequency detector**Fig. 12** Charge pump and LPF

Phase detector:

$$[F_{\text{ref}}(s) - F_{\text{fb}}(s)]K_d = V_d(s) \quad (1)$$

$$H_{\text{lpf}}(s) = \frac{v_2(s)}{v_d(s)} = \frac{1}{cs} \quad (2)$$

VCO:

The loop filter will produce the control voltage which is fed into VCO. The output frequency gets altered according to the control voltage, so the transfer function of VCO is given as

$$H_{\text{vco}}(s) = \frac{F_{\text{out}}(s)}{v_2(s)} = \frac{k_v}{s} \quad (3)$$

5 Conclusion

This paper presented a different analysis of various techniques to design the PLL blocks. From the different methods to design phase and frequency detector, digital pulse amplifier is the best method since it produces less dead zone. Charge pump and loop filter can be done by bilinear transformation of RC loop filter. The best VCO is coherent-based phase synchronous oscillator with improved coherency, lock-in range with less phase noise. If the entire best block can be put together in the DPLL with various constraints such as lock-in time, power consumption, acquisition time, tuning range can be evaluated and compared with existing DPLL.

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