

# System Verilog Assertions

## LAB Material

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Lab 2 ...

overlapping and  
non-overlapping  
implication operator ...

# LAB 2 : Overlap and non-overlap operators

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## LAB Overview

*This example is simply to high light how property behaves with an overlapping implication operator and with a non-overlapping implication operator. It also helps you understand how piplelined threads of a property work*

## LAB Objectives

1. *You will learn how an overlapping vs. non-overlapping implication operator works.*
2. *You will also learn how multiple pipelined threads work through a property.*

## LAB Design Under Test (DUT)

*There is no DUT as such in this example. Only a simple property coded with overlapping and non-overlapping operator.*

# LAB 2 : Overlap and non-overlap operators

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## LAB: Database

### FILES:

1. *test\_overlap\_nonoverlap.sv* :: A simple example showing how to model a property with overlap and non-overlap implication operator.
2. *LAB\_QUESTIONS* :: This file has questions that you will answer as pointed out below in compile/simulate section.

## LAB: How to compile/simulate - step by step instructions

1. `% cd <myDir>/SVA_LAB/LAB2`
2. `% run_overlap`  
This will create *test\_overlap.log*
  - Study *test\_overlap.log*
  - Answer the questions embedded in the file *./LAB\_QUESTIONS* for *+define+overlap*
3. `% run_nonoverlap`  
This will create *test\_nonoverlap.log*
  - Study *test\_nonoverlap.log*
  - Answer the questions embedded in the file *./LAB\_QUESTIONS* for *+define+nonoverlap*