

Preface

When an engineer in a London Post Office got tired of sorting hundreds of tangled cables between their connectors, he filed a patent named “Improvements in or Connected with Electric Cables and the Jointing of the Same” in 1903—probably without foreseeing the broad implications of his “flat foil conductors laminated to an insulating board”. Thus was born the *printed circuit board (PCB)*, which became an engineering success. The first boards required extreme manufacturing skills—electronic devices were fixed between springs and electrically connected by rivets on Pertinax. Copper-laminated insulating layers were introduced in 1936, leading the way to reliable, mass-produced printed circuit boards. These boards enabled the manufacture of affordable electronic devices, such as radios, which have become indispensable items in everyone’s home ever since.

The invention of miniature vacuum tubes in 1942 started the first generation of modern electronics. The earliest large-scale computing device, the Electronic Numerical Integrator and Computer (ENIAC), contained an impressive 20,000 vacuum tubes.

In 1948, the invention of the transistor kickstarted the second generation of computing devices. These transistors proved to be smaller, cooler and much more reliable than their predecessor vacuum tubes, enabling truly portable electronic gadgets, such as small transistor radios.

The 1960s saw the dawn of the third generation of electronics, ushered in by the development of *integrated circuits (ICs)*. Together with semiconductor memories, they enabled increasingly complex and miniaturized system designs. Subsequently, we witnessed the first microprocessor in 1971, followed soon thereafter by a host of technical breakthroughs whose impact remains evident today. In 1973, Motorola developed the first prototype mobile phone, in 1976 Apple Computer introduced the *Apple I*, and in 1981 IBM introduced the *IBM PC*. These developments foreshadowed the *iPhones* and *iPads* that became ubiquitous at the turn of the twenty-first century, followed by intelligent, cloud-based electronics that complement, facilitate, and enhance our lives today. These days, even the cheapest smartphone contains more transistors than there are stars in the Milky Way!

This spectacular success in the art of engineering relies on a crucial step: transforming an abstract, yet increasingly complex circuit description into a detailed geometric layout that can subsequently be manufactured “for real” and without flaws. This step, referred to as *layout design*—or *physical design*, as it is also known in the industry and which is the term we use in this book—is the final stage in every electronic circuit design flow. All of the instructions necessary for fabricating PCBs and ICs must be generated in this step. Essentially, all components in the abstract circuit description, consisting of the device symbols and the wire connections between them, are translated into formats that describe geometric objects, such as footprints and drilling holes (for PCBs) or mask layout patterns comprising billions of rectangular shapes (for ICs). These blueprints are then used during fabrication to “magically create” the physical electrical network on the surface of a silicon chip in the case of an IC—which performs exactly the same functions as envisioned in the initial circuit description when electrons are sent through the system. Without this physical design stage, we would not have even the simplest radios, let alone laptops, smartphones or the myriad of electronic devices we take for granted nowadays.

Physical design was once a fairly straightforward process. Starting with a netlist that describes the logical circuit components and interconnections, a technology file, and a device library, a circuit designer would use floorplanning to determine where different circuit parts should be placed, and then the cells and devices would be arranged and connected in the so-called place and route step. Any circuit and timing problems would be solved by iteratively improving the layout locally.

Times have changed; if previous generations of circuit designs represented complexity analogous to towns and villages, current-generation designs cover entire countries. For example, if the wires in one of today’s ICs, such as found in a smartphone, were to be laid out with regular street sizes, the area of the resulting chips would stretch over the continental U.S. and Canada combined, covered entirely with streets shoulder-to-shoulder! Hence, today’s multi-billion transistor circuits and heterogeneous stacks of printed circuit boards require a far more complex physical design flow. Circuit descriptions are *partitioned* first in order to break down complexity and to allow parallel design. Once we have arranged the contents and interfaces of the partitions during *floorplanning*, these blocks can be handled independently. *Placement* of devices is the first step, followed by *routing* their connections. *Physical verification* checks and enforces timing and other constraints, and multiple measures are applied in a *post layout process* to ensure manufacturability of the IC and PCB layout.

The field of physical/layout design has grown well beyond the point where a single individual can handle everything. Constraints to be considered during layout generation have become extremely complex. The stakes are high: one missed reliability check can render a multi-million-dollar design useless. The fabrication facility to produce a single technology node can easily cost over a billion dollars. Research papers describe solutions to a myriad of these problems; their sheer volume, however, renders it impossible for engineers to keep pace with the latest developments.

Given the high stakes and the incredible complexity, there is a pressing need to temporarily step back from these rapid developments and to consider the *fundamentals* of this extremely broad and complex design stage. Students need to learn and understand the basics behind today's complicated layout steps—the “why” and “how”, not just the “what”. Engineers and professionals alike need to refresh their knowledge and broaden their scope as new technologies compete for application. With Moore's law and thus, continuous down-scaling being replaced by novel and heterogeneous technologies, new physical design methodologies enter the field. To successfully master these challenges requires sound knowledge of physical design's basic methods, constraints, interfaces and design steps. This is where this book comes in.

After a thorough grounding in general electronic design in Chap. 1, we introduce the basic technology know-how in Chap. 2. This knowledge lays the foundation for understanding the multiple constraints and requirements that make physical design such a complicated process today. Chapter 3 looks at layout generation “from the outside”—what are its interfaces, how and why do we need design rules and external libraries? Chapter 4 introduces physical design as a complete end-to-end process with its various methodologies and models. Chapter 5 then dives into the individual steps involved in generating a layout, including its multifarious verification methodologies. Chapter 6 introduces the reader to the unique layout techniques needed for analog design, before Chap. 7 elaborates on the increasingly critical topic of improving the reliability of generated layouts.

This book is the result of many years of teaching layout design, combined with industrial experience gained by both authors before entering academia. Chapters 1–7 are well structured for teaching a two-semester class of layout/physical design. For use in a one-semester class, Chap. 1 (introduction) and Chap. 2 (technology) can be assigned for self-study, with instruction starting with Chap. 3 (interfaces), followed by design methodologies (Chap. 4) and design steps (Chap. 5). Alternatively, Chap. 4 can also be used as an effective starting point, followed by the detailed design steps of Chap. 5, intermittently extended with material from the respective interfaces, design rules and libraries presented in Chap. 3. All figures of the book are available for download at www.springer.com/9783030392833.

A book of such extensive scope and depth requires the support of many. The authors wish to express their warm appreciation and thanks to all who have helped produce this publication. We would like to mention in particular Martin Forrester for his key role in writing a proper English version of our manuscript. Special thanks go to Dr. Mike Alexander who greatly assisted in the preparation of the English text. His knowledge on the subject matter of this book has been appreciated. We thank Dr. Andreas Krinke, Kerstin Langner, Dr. Daniel Marolt, Dr. Frank Reifegerste, Matthias Schweikardt, Dr. Matthias Thiele, Yannick Uhlmann, and Tobias Wolfer for their many contributions. Our warm appreciation is also due to Petra Jantzen at Springer for being very supportive and going beyond her call of duty to help out with our requests.

Rapid progress will continue apace in layout design in the years to come, perhaps by some of the readers of this humble book. The authors are always grateful for any comments or ideas for the future development of the topic, and wish you good luck in your careers.

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