WHAT'S ON IN THE EDIF TEST ARE(N)A?

by

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A B S T R A C T

The paper outlines the status quo of the EDIF test activities. A great deal of technical issues could be settled, action points in the field of functional test are closed and a solid proposal has been worked out. The past has seen a major shift of emphasis in the methodology towards the "EDIF Test Extension". To avoid getting entangled in syntactic constructs, the primary task of the TSC Test is and will be to develop a coherent and consistent information model for testing. The line of development towards such a semantic model is studied closely. Three steps to a standard are presented: from conceptual via information modelling to syntactic representation. Each step is illustrated by state-of-the-art examples.

1 FOR THOSE WHO HAVEN'T HEARD YET ...

The development of the EDIF Test Extension is a joint effort between the American and European sections of the EDIF TSC Test. The groups work together very closely using all means of electronic communication at hand, such as fax, e-mail and telephone conferences. Furthermore, several common workshops were held abroad. The TSC is optimistic that work will be up to schedule and a thoroughly worked-out proposal ready in the course of 1991.

1.1 ... What It Is All About: Bridging The Gap Between Design & Test

The CAx scenario of today places design and test engineers in a predicament: on the one hand, highly sophisticated design and verification tools (CAD/CAE) and automatic test equipment (ATE) are readily at their disposal. In principle, they are free to choose services and equipment best suited for a particular task from a growing number of suppliers. On the other hand, however, the variety of feasible choices is strongly narrowed when it comes to exchanging design and test-oriented information. That is when engineers encounter the well known problem of interfacing design to test.

While numerous test-oriented interchange formats have been developed over the past decade, none of them has turned out to be a suitable candidate for an industry standard because of one or more of the following drawbacks.

- Narrow scope

  Not all aspects of test are adequately addressed by the same format, e.g. the description of both event-oriented time linear and tester-oriented cyclic waveforms. Furthermore, the scope of transfer is limited to the area of test neglecting other disciplines of designing and verifying electronic products.

- Proprietary constraints

  Many formats are owned or controlled by individual CAE and ATE companies. As a consequence, access and proliferation are limited by licensing. In addition, formats are generally centered on peculiarities of test equipment, whereas from a test engineer's point of view they should be exclusively defined from the perspective of the device under test. This orientation towards individual testers leads to incompatibility. The focus should be set on principles of testing rather than on aspects of software and hardware implementation.

- Lack of an underlying semantic model

  The majority of present formats misses the capacity to meet future demands of integrating design & test. Among other things, they fail to take into account DFT techniques (design for testability) like Boundary Scan and LSSD for printed circuit boards and integrated circuits respectively. This is due to an apparent lack of a clear information model from which the format's syntax should have been derived.

Examples of existing standards for test are described in [1,2,3]. A profound comparison is given in [4,5]. Most of the data and control channels among simulators, test pattern generators and testers have to be bidirectional (stimuli, expected and physical responses, not just ones and zeroes). Fig. 1.1 illustrates how the data network in a heterogenous design & test environment can be disentangled. Carried to the extreme, the order of magnitude of transformers and formatters needed would grow to the square of the number of communicating units. In the long run, only a common interchange format for all facets of design & test data will drastically diminish investment in format converting. The public interchange format EDIF [6,7] has successfully overcome most of the drawbacks outlined above in the fields of mask artwork, netlists and schematics. Being a well established industry standard, it has the potential to achieve similar importance in the area of test where current means of description are fairly limited [8].

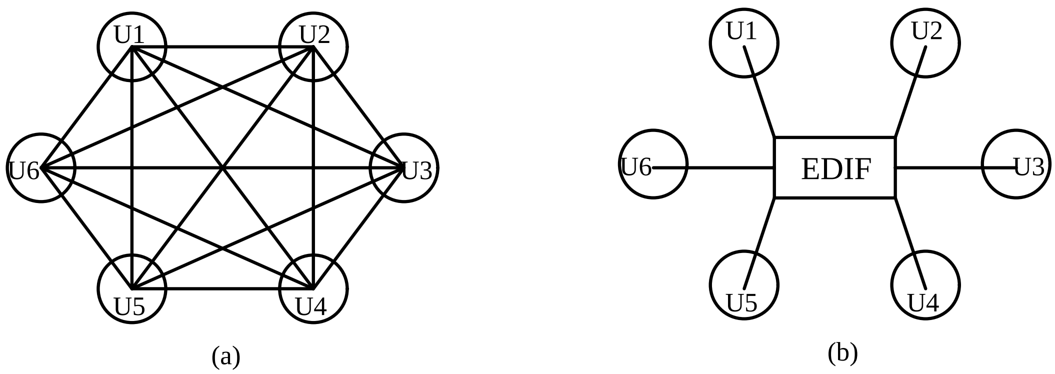

Fig. 1.1: Reducing the number of transformers and formatters from quadratic (a) to linear (b).

1.2 ... What The EDIF Test People Have Been Working On

As resources are limited, the members of the EDIF TSC Test decided to set the focus of work on the transfer of test information. The problem of data mismatch between simulation and test is tackled by the concept of *tester-oriented cyclic waveforms*. The notion of tester-oriented does not stand for any peculiarities of specific test equipment in the marketplace. It is in contrast with *event-oriented time linear waveforms* as common logic simulators produce them. Support for the latter concept will be an issue in the following-up phase.

Currently, work on several topics related to the transfer of test information has matured to a degree that preliminary proposals can be provided:

- General information model

  A textual as well as an innovative graphic description have been developed identifying the basic semantic entities and their interrelationships. (The development process towards a test information model is subject of the following chapter.) The model will serve as a basis for further discussion between the American and European working groups. In its final version, it will represent the information content of the EDIF Test Extension.

- Top level

  The TSC has concluded definition of the top entity (test plan) in the information model. The test flow, i.e. the execution order of test sequences, has been extended.

- Conceptual model

Consensus on a model of test has been reached. The model serves as a conceptual framework. It is the result of reducing the variety of test concepts to a common denominator.

- Pattern-oriented description

  The signal representation lies at the heart of the information model. Essentially, signals are described in a block-oriented framework consisting of four two-dimensional sub-blocks. A row represents a complete cyclic signal waveform. Columns reference the ports which the signals are applied to (driven ports) or measured at (sensed ports). The individual arrays carry information about logic values, timing (frames like NRZ, RC, SBC, etc.), cycle duration and references to electrical levels, e.g. CMOS and TTL. Thus, all signal characteristics may, at least theoretically, change on the fly. Fig. 1.2 gives an example. Note well: the block structure does not predetermine any syntactic constructs.

  Agreement on several aspects of pattern description could be reached: among other things, frames, pattern annotation, logic values, array compaction and block concept.

- Scaling mechanism

  It is now up to the TC to decide on the final scaling mechanism. It will be based either on a straightforward percentage solution or on the descriptive means of EDIF level 1 (variables and expressions).

- Events

  Though debatable, events are only considered in connection with simulator-oriented data.

- Report

  Measured values can be both compared to expected values and logged in a log-book (report device) for later off-line use. The report mechanism is triggered by referencing the individual measurements of interest.

- Support for DFT techniques

  Boundary Scan and LSSD are, of course, important issues and will be adequately reflected in the model. The work in the field of DFT techniques has good prospects to flourish. On the one hand, the TSC can profit from the active membership of one of its own members in JTAG. On the other, the European section can take advantage of great expertise in design for testability from both academia and industry.

- Data sheet

  A test specific extension to the usual data sheet for electronic devices has been worked out identifying the methods, parameters and environmental conditions under which the test is to be performed.

cycle	logic values			frames			cycle duration	electrical levels		
	A	B	C	A	B	C	all ports	A	B	C
1	H	L	H	RZ	RZ	SBC	100	CMOS_I	CMOS_I	CMOS_I
2	L	L	H	NRZ	RZ	SBC	100	CMOS_I	CMOS_I	CMOS_I
3	H	L	L	NRZ	RZ	SBC	100	CMOS_I	CMOS_I	CMOS_I
4	L	L	L	NRZ	RZ	SBC	130	CMOS_I	CMOS_I	CMOS_I
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮

Fig. 1.2: Block-oriented representation of test patterns

1.3 ... What They Will Be Working On

Besides improving and refining the current proposals for general aspects of test information, future work will concentrate on advanced topics hardly covered by existing interchange formats. This promises to be a wide and challenging area where great efforts have to be made. Among other things, the emphasis will be set on:

- Fault dictionary
- Guided probe
- Tester description
- Specification of tolerances
- Parametric test
- Environmental test
- Analogue test

1.4 ... How They Will Reach Their Aims

It was at the Third European EDIF Forum '89 in Bonn where the new line of development towards future versions was first made public to the EDIF community. Frans Meys presented some ideas about conceptual modelling and the necessity for it [9]. It was about that time the new directive of the Technical Committee had reached its subcommittees saying that, without an underlying conceptual model, future proposals for technical extensions to EDIF would not be accepted anymore.

To the members of the TSC Test, this was nothing out of the blue as they had already taken to heart the rationale behind the TC's directive in the past. From the beginning, a systematic approach was followed to manage the immense bulk of test data. In a multi-corporate effort, a requirements analysis resulting from a close study of existing standards [10] and self-experienced unsatisfied needs [11] was set up first. To come to a consensus on the components which constitute a test, a generalized conceptual model of a device under test (DUT) was developed. This model now serves as a basis of discussion for test-related aspects and helps to identify the problem areas not covered by present test formats [12].

Thus, for the TSC Test it is not a question of just following a directive without seeing reason for it. It is a continuation and in some respects a reworking of the systematic approach by other means, namely information modelling. This will be studied closely in the following chapter.

2 THE ART OF MODELLING OR HOW TO GET TO GRIPS WITH INFORMATION

The relatively young interchange format EDIF is now facing the same old story of form and content, matter and manner, syntax versus semantics — the question of **how** information is formatted and transferred and **what** entities of information are actually to be transmitted. The "syntax crisis" of EDIF has become obvious by the ever growing volumes of *Queries and Answers* — the laborious attempt to clarify the (user's) misunderstandings of syntactic constructs. The existence of the crisis is further indicated by the fact that a whole technical session of the Fourth European EDIF Forum is devoted to the theme of information modelling. The Technical Committee is aware of the problems arising from the pure syntax-orientation of EDIF and it is determined to contain the flood of further constructs to a minimum. As a consequence, any proposals for modifications and extensions to the current version have to be based on a solid information model to be described formally with the help of the information modelling language Express [13].

Against this background, the European EDIF TSC Information Modelling Working Group (IMG) was launched at the end of 1989 in Manchester. Its prime objective is to develop a general information model of the underlying concepts of EDIF — a model "from which the EDIF syntax could have been derived" [14,15]. As was said before, the TSC Test does not consider this to be a new way of thinking in the EDIF community. A successful management of the bulk of test data does not allow the traditional syntax-oriented approach. From the beginning, it was evident that prior to any syntactic representation one has to get to grips with the information content of test-oriented concepts. In this context, it is interesting to follow the TSC's special way of approaching the art of modelling.

2.1 The Time Before

Previous versions of the so-called "Blue Book" of the Everest Project [16] — there are several personal unions between the EDIF TSC Test and the Everest Working Group on Standards — illustrate the time before **systematic** information modelling was high up on the agenda. To avoid getting lost in a jungle of syntactic constructs, the test people helped themselves with informal textual descriptions and rudimentary graphic representations of test concepts. Their textual approach to documentation — a description of all the entities in the graph of the data model given by terms of *definition*, *synonyms* and *rationale* — was pioneering in the sense, that it served as a pattern for the final structure of the data dictionary proposed by the EDIF Information Modelling Group. In addition, the necessity for a graphic representation of data models was first felt by the TSC Test and communicated to the IMG (again, through personal union between the European working groups of the TSC IMG and the TSC Test). It stimulated further research into graphic notations.

The previously used "balloon diagram" functioned as a vehicle of communication between the American and European sections. Though not being formalized and very expressive, the graphic notation of the balloon diagram helped a lot to structure and clarify the vast amount of test data. Admittedly, this model was nearer to aspects of implementation rather than to a representation of the information content. The justification for this leaning to implementation, now regarded as a breach of rules in information modelling, is twofold: on the one hand, efficiency of data structures for test is a key issue with respect to usability and acceptance of a standard. Thus, in the area of test, aspects of implementation must always be taken into account. On the other hand, it takes quite an effort to change from the traditional way of procedural thinking as professional programmers are used to it to the descriptive, non-procedural way of information modelling. This can be compared to the predicament of object-oriented programming languages and database technologies which face a similar "semantic gap" to get the message of object orientation across. The comparison seems to suggest itself as it is beyond doubt that information modelling is mainly influenced by object-oriented concepts of encapsulation, classes, instantiation and inheritance.

To sum up, the members of the EDIF TSC Test are well prepared for the new systematic approach towards information modelling.

2.2 The Time Now

Learning the art of modelling is a question of learning new skills. The first steps are taken. The data model of the past has been thoroughly reworked and a solid nucleus of a test information model extracted. The TSC has dedicated itself to a universal systematic approach to the final proposal for a test standard. The approach taken is analysed in the following.

2.2.1 Three Steps To A Standard For Test

In the past, the conventional approach to a standard followed a prolonged and non-systematic line of development:

(1) Most standards have their origin in an internal agreement of an influential or innovative company on interfaces and data transfer formats. As a consequence, they are company dependent and confidential.

(2) Provided there is a broad need for a close cooperation among several companies, for example CAD and ATE suppliers, the agreement is taken further to a de-facto industry standard. In this case, the existence of such a standard will create a demand for adequate converters to other standards.

(3) As several corporate agreements come up simultaneously following steps (1) and (2), there will finally be a pool of de-facto standards further prompting the demand for converting software.

(4) To formally establish a widespread de-facto standard in industry, it is carried to national and international standardization bodies, like ANSI, ISO, DIN, etc. Having passed the standardization procedure, the originally internal company agreement turns to be a de-jure industry standard.

It is evident, that this line of standardization will lead to serious drawbacks as outlined in the previous chapter. The development of EDIF has partly followed the same pattern, except that from the beginning a **group of companies** have worked together to combine the best features of existing interchange formats to a universal one.

The common characteristic of most standards which resulted from this conventional approach is their orientation to syntactic constructs without being embedded in a semantic framework. The negative experiences of the conventional standardization process have made the EDIF TSC Test take a **strictly systematic approach:** from conceptual via information modelling to syntactic representation.

The advantages of this systematic approach can be summed up as follows:

- It helps to concentrate on the semantic entities which really represent the area of interest and that are not just syntactic or physical carriers of information.
- It frees oneself from "thinking in syntactic constructs".
- Sources of misunderstanding, like semantic contradictions, omissions and weak points, can easily be identified.
- It facilitates team communication.

- The question of syntactic representation can be postponed to the final step. Indeed, numerous different syntactic structures can be derived from the same information model. The mapping of the model to a format is a straightforward task.
- Given a semantic model, an evaluation of different formats can be performed on the objective basis of information content.

2.2.1.1 Step One: The Conceptual Model

The objective of conceptual modelling is to describe the scope and functionality of an area of interest and to identify the semantic entities involved. In general, the model's notation is arbitrary. The means of formal description are only a matter of convenience: graphic notations, e.g. block diagrams, graphs and tables, or textual documents like data dictionaries and glossaries. The learning curve of conceptual modelling is not easy to take, but it is worth the effort as it is of fundamental importance for the subsequent determination of the information content. Coherence and consistency of the information model depend essentially on the conceptual framework.

This was due to the area of testing where a consensus on the components constituting a test could hardly be reached. After long sessions of brainstorming and clarifying debates, the EDIF TSC Test has finally agreed on a basic model (Fig. 2.1) first presented in [12]. It serves as a paradigm for the variety of possible tests.

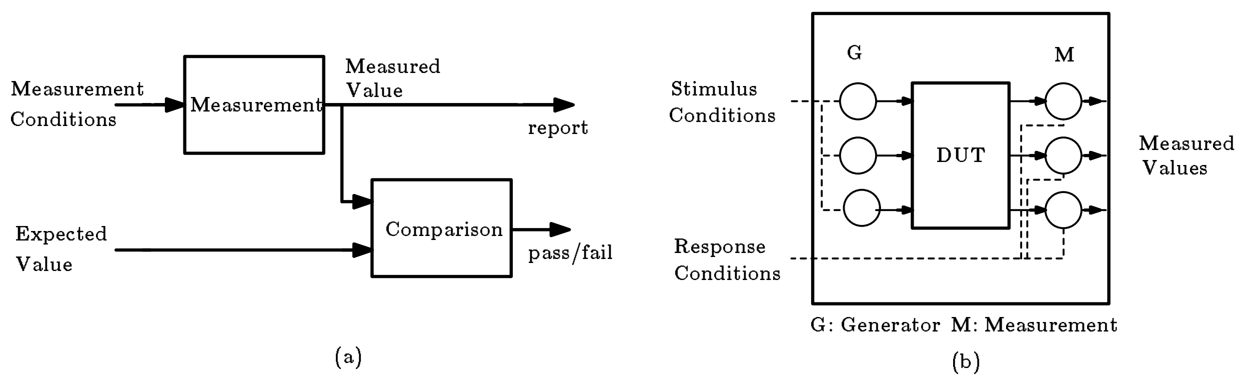

Fig. 2.1: A conceptual model for testing (a) and its partial refinement (b)

Two prime operations can be identified in any test procedure: measurement and comparison. Though, in digital systems these distinct operations are usually implemented in hardware and thus not visible to the user individually. The conditions under which a measurement is to be performed are of two kinds. Stimulus conditions are given by electrical and environmental signals and must be applied to the DUT (analogue or digital electrical quantities, temperature, humidity, etc.). They stimulate the device and cause it to change its electrical state. Response conditions, applied to measurement instruments, determine when and how the responses of the DUT are to be measured, e.g. strobe point, strobe window, output loading. The measurement operation, as a whole, supplies a parameter value of the device under test. The comparator decides whether this measured value is up to expectation and produces a boolean result accordingly. The measured value may be additionally logged in a report unit for further fault analysis.

2.2.1.2 Step Two: The Information Model

The next step of semantic refinement leads to the information model. It implements the corresponding conceptual model in terms of entities and relationships. Entities constitute semantically distinguishable objects like signals, ports and measurement. Hierarchic relationships among entities are described by supertype/subtype trees. However, information modelling should be carefully distinguished from database modelling, for example, the entity-relationship model in the context of relational databases, and from data structures of programming languages like records, arrays and lists. The distinction lies in the degree of closeness to physical implementation (relational tables, hardware addressing techniques, etc.). An information model — in its purest form — does not reflect aspects of software and hardware implementation. The only matter of interest is the information content within a given conceptual context.

Contrary to the arbitrary notation of conceptual models, there is a clear directive from the Technical Committee to use the formal information modelling language Express [13] as a textual means of description. Express sets the focus on the definition of information classes, called *entity types*, which constitute the area of interest. Entity types are defined in terms of attributes which, in turn, are represented by other entity types. Entities are considered to be independent, but constraints can be given to effect dependency. This is done by *rules* in the global context of a *schema* (schemata partition the area of interest) or by *where*-clauses in the local scope of an entity type. A closer look on the methodology of Express is taken in [14,15]. Fig. 2.2 gives an extract from the current Express description of the test information model.

```
ENTITY test_plan;
  dut          : DUT_description;
  logicValues  : OPTIONAL SET [1:#] OF logic_value;
  frames       : OPTIONAL SET [1:#] OF frame;
  levels       : OPTIONAL SET [1:#] OF level_mapping;
  blocks       : OPTIONAL SET [1:#] OF block;
  signals      : OPTIONAL SET [1:#] OF signal;
  tests        : OPTIONAL SET [1:#] OF test;
  flow         : test_flow;
  faultDic     : OPTIONAL fault_dictionary;
END_ENTITY;
```

Fig. 2.2: Partial Express description of the top level of the EDIF Test Extension

The language can be read by humans and parsed by computers. The formal description offers the possibility of using programs to check up on semantic consistency. At present, however, only syntax checkers are available. Furthermore, besides a pure textual description, Express offers a proposal for a graphic notation, called Express-G, as a subset of its language. The graphic constructs are partly oriented to IDEF 1X [17], a general description methodology. Graphic generators are currently under development to create a graphic representation from an Express file. Fig. 2.3 and 2.4 illustrate the use of Express-G in the context of test.

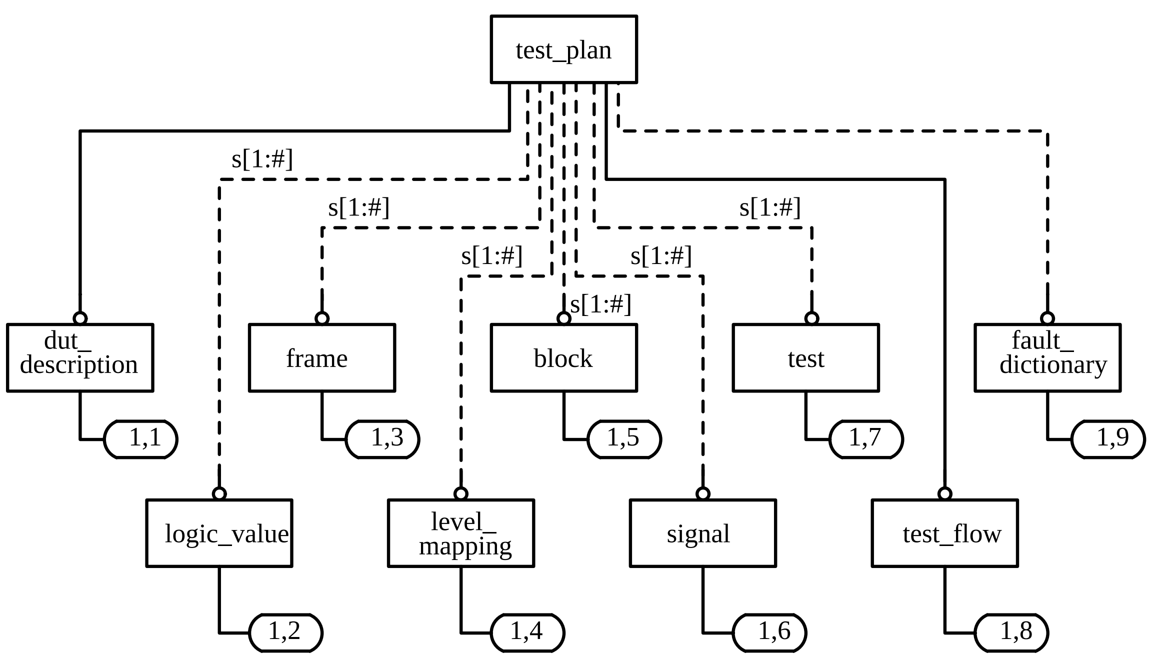

Fig. 2.3: Express-G representation of top level

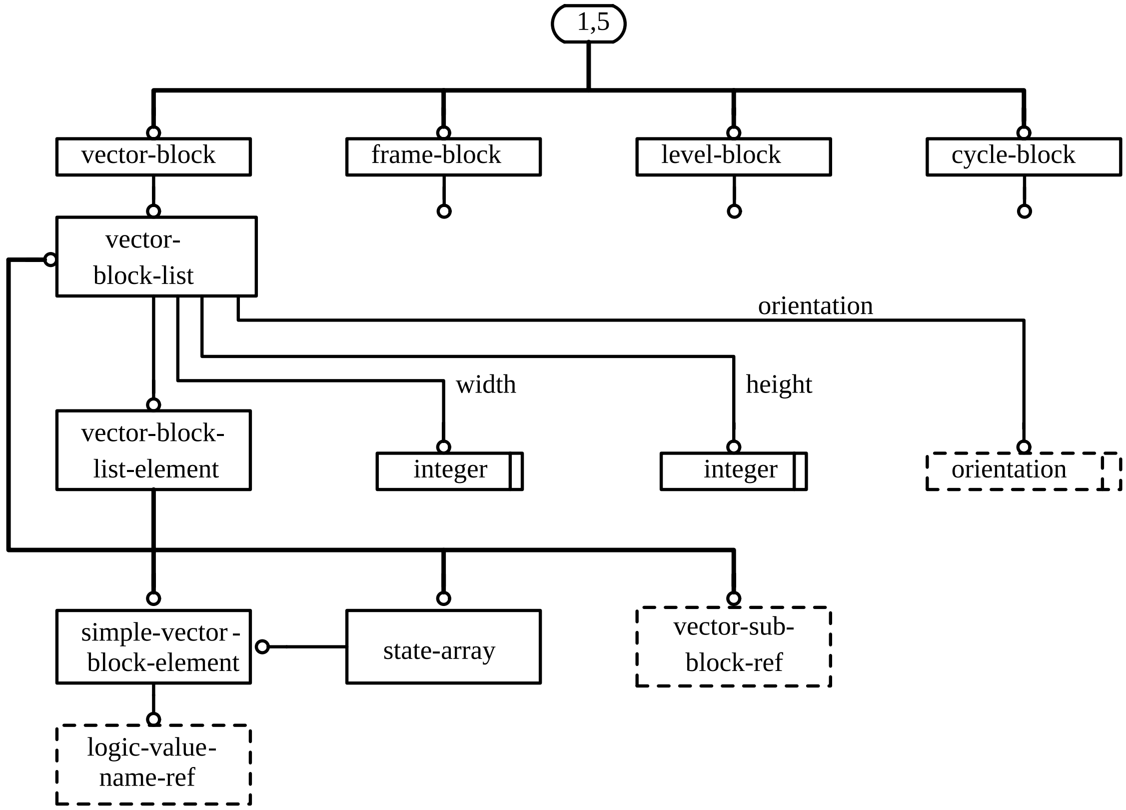

Fig. 2.4: Express-G representation of the block concept

As a third means of documentation, data dictionaries are written by extracting annotated text and structural information from the Express description. The data dictionary contains two main sections, one for the description of schemata, the other for entity types. Each entity type is listed by name. The entity context, definition and constraints are given. The data dictionary is more than just a catalogue of items. It incorporates a glossary and the rationale for every entity type and schema. Fig. 2.5 illustrates the structure of the Express data dictionary which resulted from close cooperation between the TSCs of Test and Information Modelling.

Schema Name:
    superschema of: *(all subsequent nested schemata)*
    subschema of: *(at least: universe, otherwise the whole schema path)*
    schemata assumed: *(all references — "bridges" — to other schemata for scope control)*
    assumed by schemata:
Schema Description: *(general description of the area of interest)*
    Enclosing Entities: *(list of entity names)*
Rationale: *(why is the area of interest enclosed as given? — justification of the containing structure chosen — peculiarities of the model)*

Entity Name: *(strictly speaking, the following refers to entity types and not to instances of them as the term "entity" might suggest)*
Schema Context: *(schema path)*
Entity Context: *(location within supertype/subtype-trees)*
    supertype of:
    subtype of:
    sibling subtypes:
Entity Description: *(description of the entity's attributes — explicit and derived — and their constraints)*
    Entity Synonyms:
    Attributes:
        explicit:

derived:
Entity referred to in: *(back references)*
functions:
procedures:
rules:
entities: *("mapped from")*
Example: *(an illustrative entity instance)*
Rationale: *(the "overall why" — peculiarities of the model, limitations of the expressive power of Express, contradictions, etc.)*
See Also: *(forward references to other entity types and schemata)*

Fig. 2.5: The structure of the Express data dictionary

2.2.1.3 Step Three: The Syntactic Representation: Make Your Choice

The last step to a standard leaves freedom to choose. It is a decisive feature of information modelling that the final syntactic representation results from *one-to-many*-mapping. Thus, numerous different syntactic structures can be derived from the same source. Generally speaking, this mapping is a straightforward task and applicable to any given syntax definition. Fig. 2.6 shows the enveloping structure of the EDIF Test Extension.

```
(testPlan ...                  * begin of test program
  (dutDescription ...)         * description of the device under test
  (logicValue                  * definition of logic values
  .
  .
  )
  (frame                       * definition of tester waveforms
  .
  .
  )
  (levelMapping                * how logic values are assigned to electrical levels
  .
  .
  )
  (block ...                   * definition of block structure
    (vectorBlock ...           * logic patterns
      (vectorBlockList ...)
    )
    (frameBlock ...)           * timing
    (levelBlock ...)           * electrical levels
    (cycleBlock ...)           * cycle duration
  )
  (quadTable                   * definition of signals
  .
  .
  )
  (test                        * definition of first test
  .
  .
  )
  (testFlow ...)               * execution order of test sequences
  (faultDictionary ...)
)                              * end of test program
```

Fig. 2.6: Syntactic representation of top level (first draft)

2.3 The Time Ahead

Applying Express to the area of test — both textually and graphically — has initially been a European discipline. Meanwhile, the Express policy has been fully adopted by both sections of the EDIF TSC Test. As a first result, the general information model for testing and some partial refinements of it can be presented. The model clearly indicates the direction how future activities will be formally embedded in a conceptual framework.

Further research into test-related topics, as outlined in the previous chapter, will be exclusively guided by the methodology of information modelling.

SUMMING-UP

A status report of the EDIF Test Extension was given and future activities were outlined. It was demonstrated that the new era of information modelling — now closing in on the EDIF community — had not taken the TSC Test by surprise. The subcommittee's work had been devoted to conceptual modelling from the beginning. However, the TSC decided to adopt a **strictly systematic approach** towards drafting the final proposal. As a consequence, the information model for testing will be documented by innovative powerful means of description: Express information modelling language, graphic notation of Express-G and automatically produced data dictionary.

ACKNOWLEDGEMENTS

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PS: Membership of the TSC Test is open to any test enthusiast. In case of further questions, feel free to contact Michael G. Wahl, co-chair, at the address above.

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