Part II
Quantum point contacts

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The discovery of the quantized conductance in ballistic quantum point contacts (QPCs) has both motivated as well as enabled a large number of subsequent experiments in the field of mesoscopic transport in low-dimensional systems. It is the intention of this review both to introduce the general reader to this active field of current research, as well as to provide an accurate summary of the development of the field to date.

2 Overview of systems

The electronic properties of metallic point contacts have always attracted considerable interest since their non-linear properties yield significant information about the electron-phonon interaction in such systems [80J]. Such point contact spectroscopy in metallic point contacts requires devices with dimensions comparable to the mean free path of the electrons, and is therefore limited to relatively pure metals. It is only comparatively recently that it has become technologically possible to fabricate point contacts whose lateral dimensions are not only smaller than the mean free path of the electrons but also comparable with the Fermi wavelength λ_F of the system. Such quantum point contacts were first fabricated in semiconductor systems with Fermi wavelengths of the order of 40 nm [88vW1, 88W1] and their conductance was found to be quantized in units of $2e^2/h$. This fundamental result is the quantum-mechanical analogue of the Sharvin resistance for classical point contacts [65S] where the conductance scales linearly with the product $k_F A$, where A is the cross-section of the point contact. Interestingly, in the transition regime between tunneling and a metallic point contact in scanning tunneling microscope (STM) studies [87G] a step in the conductance was observed even earlier. The magnitude of this step corresponded to a change in resistance of the order of 10 kΩ ($h/2e^2 = 12.8\,\text{k}\Omega$) and was subsequently associated with the formation of a quantum point contact [88F]. More recently metallic quantum point contacts with lateral dimensions comparable with the size of a few metallic atoms have been systematically fabricated and investigated [93A, 93K2]. Conductance steps have also been observed in such metallic quantum point contacts, however, the interpretation of these experiments remains the subject of much debate and we shall concentrate here on the physical properties of the semiconductor devices where the data have been well explained.

A quantum point contact consists essentially of a short, narrow constriction connecting two conducting reservoirs, as illustrated in the micrograph of Fig. 10. The dimensionality of the reservoirs, while certainly of relevance for the transport properties, is usually determined by the utility of fabrication and is, for the overwhelming majority of experiments to date, defined by some two-dimensional electron system. Both silicon based systems as well as III-V heterostructure materials have been successfully used in the fabrication of such devices, although the excellent low-temperature electron mobility of the latter has meant that many of the fundamental investigations have been performed using these systems.

The fabrication of the quantum point contact itself invariably involves some form of high-resolution lithography; as mentioned above, the lateral extent of the contact perpendicular to the direction of the current must be of the order of the Fermi wavelength and the contact itself considerably shorter than the electronic mean free path. The Fermi wavelength in semiconductor

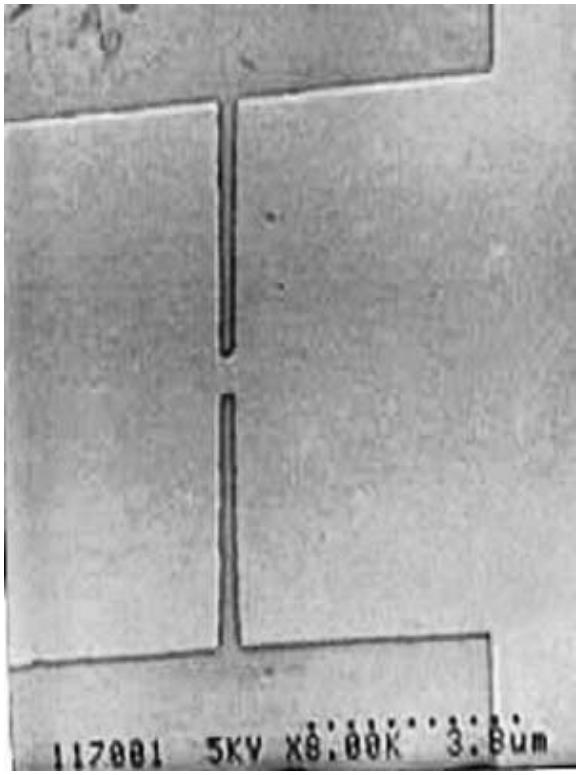

Fig. 10: An electron micrograph showing the lithographically defined gate electrodes which are used to tune the ballistic quantum point contact. The source and drain contacts are located in the extended two-dimensional reservoirs (left and right), while the gate electrodes are contacted above and below the visible portion of the micrograph.

systems is typically of the order of 50 nm, and undoubtedly electron-beam lithography has been the technology most often employed in the fabrication of such devices although other techniques, such as atomic force lithography and focussed ion beams, have been successfully exploited.

2.1 Si-based systems

Silicon based systems can be subdivided into essentially two categories: those defined in the two-dimensional electron gas (2DEG) formed in the inversion layer of a Si-MOSFET, and those systems based upon Si/SiGe heterostructures. The former invariably require the fabrication of patterned gate electrodes for the definition of a suitably structured inversion layer, while the latter employ the gate electrodes to deplete the underlying 2DEG. For the MOSFET devices the simplest possibility consists of a single structured gate defined above the oxide layer. This strategy has been successfully implemented using both heavily-doped polycrystalline Silicon [92T1], where a long silicon inversion wire with additional, mesoscopic voltage probes separated by 1 μm was defined, as well as with metallic electrodes [95T2] appropriately patterned to form a narrow constriction between source and drain contacts. A more flexible approach lies in the fabrication of a stacked-gate geometry [86W, 90G1]; a lower patterned electrode defines the device geometry while an upper electrode, separated by an additional oxide layer controls the electron density as illustrated schematically in Fig. 11.

This geometry was initially exploited in experiments on multiple one-dimensional (1D) wires [86W, 90G1] which despite showing evidence of one-dimensionality lacked the clear signature of a quantized 1D conductance. A more recent proposal for the fabrication of a QPC in a Si-nanostructure is based upon the anisotropic etchant properties of KOH [97N]. A lithographically defined channel is employed as an etch mask for (110) Si. The narrow channel thus defined develops pronounced {111} planes due to the slow etch rate of these planes. A wedge shaped channel forms whose width is determined by the etched depth. The resulting channel can be subsequently oxidized and gated; the QPC thus formed showed clear evidence of conductance plateaux, albeit

at conductance values significantly smaller than the multiples of $8e^2/h$ expected for the valley degeneracy ($g_v = 4$) in this structure.

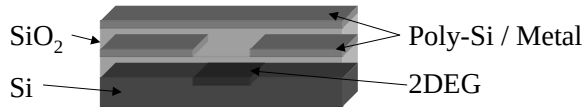

Fig. 11: The stacked-gate geometry employed in the realization of a Si-based QPC device is schematically illustrated.

All of the above devices suffer to a greater or lesser extent from the low electronic mobility, and hence short mean free path, of silicon systems. The ability to grow lattice matched $Si/Si_{0.7}Ge_{0.3}$heterostructures and the consequent improvement of the material properties has led to significant interest in this material system and its application to nanostructure physics. The fabrication of a QPC in this system is essentially similar to that required for AlGaAs/GaAs heterostructures although the definition of high-quality Schottky gate electrodes is more difficult. Typical low-temperature mean free paths are of the order a few microns and many of the phenomena associated with ballistic transport in QPCs have been observed, albeit not with the quality of AlGaAs/GaAs heterostructures. Interestingly, devices fabricated in Si/SiGe show an additional valley degeneracy ($g_v = 2$ for the commonly used crystal orientation) which leads to the observation of a conductance quantized in units of $4e^2/h$ [95T3].

2.2 AlGaAs/GaAs heterostructures

AlGaAs/GaAs heterostructures remain the system of choice for the majority of experiments on ballistic QPCs. Both the excellent low-temperature elastic scattering lengths, in excess of 10 μm, together with the comparative simplicity of the associated fabrication technology have contributed to this development. The essential geometry of a heterostructure based QPC is illustrated schematically in Fig. 12; modulation doping of the AlGaAs layer leads to the formation of a 2DEG in the GaAs substrate at the heterointerface. The application of a negative bias to the so-called split-gate electrodes depletes the underlying 2DEG and thus defines the geometry of the constriction. Independent control of the electron density is not possible.

Fig. 12: The split-gate geometry extensively used for the fabrication of heterostructure based QPC devices is schematically illustrated.

An improvement of the device tunability has been realised using a back-gated device [92H1]; in this device the underlying GaAs substrate has been intentionally doped during the MBE growth and can be contacted separately. Variation of the back-gate voltage allows independent control of the carrier density, while the QPC geometry is determined solely by the front, split-gate electrode configuration. A further limitation of the heterostructure-based QPC as discussed above lies in the device size attainable. While the fabrication technologies employed generally have a resolution limit of the order of 10 nm, the dimensions of the QPC device itself are determined by the separation between the gate electrodes and the underlying 2DEG. The inevitable, and indeed desirable, lateral depletion leads to a smoothing of any device features smaller than the distance between gate and 2DEG. In typical modulation doped structures the presence of an insulating GaAs cap-layer and the AlGaAs spacer-layer lead to surface-2DEG separations of about 70 nm. Optimization of the MBE growth can however significantly reduce these dimensions and surface-2DEG separations as small as 30 nm have been achieved [92S1]. Indeed, the resultant conductance quantization not only showed quantization energies greatly enhanced compared with standard devices, but also showed pronounced conductance features at temperatures up to 40 K.

2.3 Other III-V and metallic systems

Other III-V heterostructure material systems have also been successfully employed in the fabrication of QPC devices; in particular InAs-AlSb [93K1], GaAs/InGaAs/AlGaAs [93M1] and also InGaAs/InP heterostructures [96T1]. These studies have been motivated partly by the reduced effective mass of these systems which leads to larger quantization energies and hence, in theory, to more pronounced conductance plateaux visible at higher temperatures. This expectation has been partially confirmed, however the electron mobility of these III-V systems has yet to approach that achieved in AlGaAs/GaAs systems. Another important reason for the experimental investigation of these alternative material systems lies in the possible integration of semiconducting and superconducting systems. The reduction of the Schottky-barrier height at the semiconductor-superconductor interface plays a decisive role and it has been shown that a high indium content is highly desirable in this context. In such superconducting QPCs the normal ohmic contacts are replaced with superconducting electrodes (e.g. Nb) [95T1]; the resulting devices show additional quantized features associated with the superconducting electrodes, for example the existence of a quantized critical current.

As mentioned above, conductance quantization has also been observed in metallic quantum point contacts. A variety of techniques have been exploited to produce such metallic systems; in particular scanning tunneling microscopes [93A, 93P, 94O] as well as mechanically controlled break-junctions [93K2] have been successfully used in the investigation of conductance quantization.

2.4 Preparation and structuring

The definition of the active region of a QPC device necessarily requires some form of high-resolution lithography. As mentioned above electron-beam lithography is certainly the most widely exploited technique which has been employed for this purpose. The advantages of an excellent resolution ($< 10\,\mathrm{nm}$) combined with the flexibility of the subsequent processing steps offer unsurpassed opportunities. The standard technique uses a positive resist (such as PMMA) which after exposure and development serves as a mask for the evaporation of the metallic electrodes. Using this strategy the active device region remains unexposed and only the regions immediately underlying the metallic electrodes, which during device operation are depleted, receive a significant electron dose. With Silicon devices such as those which use the patterned electrode to create an inversion layer [92T1, 95T2] the active device region is exposed during fabrication. Alternative strategies which exploit the high resolution of electron-beam lithography are based upon a subsequent etch step as, for example, discussed above for the selective etchant KOH in Si [97N]. Another etchant technique relies upon the deep mesa etch of an insulating trench between the QPC channel and surrounding 2DEG regions [90N]; these regions then serve as in-plane gates for the tuning of the channel width. This device is a derivative of the in-plane gate transistor fabricated using focussed ion beam technology [90W1] where the ion beam was used to selectively damage the 2DEG. The original focussed ion beam experiments [89H1] employed high energy Gallium ions to define a highly resistive p-type region which served to define the conducting constriction. The lack of tunability in this structure meant that only indirect evidence for conductance quantization could be found during continuous weak illumination with a low energy ($2\,\mathrm{eV}$) light source. The focussed ion beam (FIB) in-plane gate device overcomes this weakness through the definition of conducting gate regions. However, despite several advantages such as the field configuration expected in this device, the device characteristics are rarely as clean as those observed in split-gate devices.

QPCs have also been fabricated using conventional optical contact lithography [91G]. Despite the use of contact exposure for the critical optical step, feature sizes smaller than $600\,\mathrm{nm}$ have not been realised and indeed the characteristics of these samples, regardless of the high-quality of the original material, are more indicative of a diffusive sample than a ballistic channel.

More recently scanning probe microscopes have also been employed for QPC fabrication [97H1]. A previously evaporated titanium layer can be selectively oxidised via the technique of local an-

odic oxidation. The patterned titanium structure then serves to define appropriately shaped gate electrodes. The resolution of the scanning probe technique is comparable to that attainable using electron beam lithography and the quality of the device characteristics is also correspondingly good.

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