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Wideband Amplifiers

Part 3:

Wideband Amplifier Stages With Semiconductor Devices

The only way to find the limits of what is possible
is by pushing towards the impossible!
Arthur C. Clarke

Back To Basics

This part deals with some elementary amplifier configurations which can serve as building blocks of multi-stage amplifiers described in Part 4 and 5, together with the inductive peaking circuits described in Part 2.

Today two schools of thought prevail amongst amplifier designers: the first one (to which most of the more experienced generation belongs) says that cheap operational amplifiers can never fulfill the conflicting requirements of good wideband design; the other (mostly the fresh forces) says that the analog IC production technology advances so fast that, by the time needed to design a good wideband amplifier, the new opamps on the market will render it obsolete.

Both of them are right, of course!

An important point, however, is that very few amplifier designers have a silicon chip manufacturing facility next door. Those who have, often discover that component size reduction solves half of the problems, whilst packing the components close together produces a nearly equal number of new problems.

Another important point is that computer simulation tells you only a part of what will be going on in the actual circuit. Not because there would be anything wrong with the computer, its program or the circuit modeling method used, but because designers, however experienced they are, can not take everything into account right from the start; and, in order to be able to complete the simulation in the foreseeable future, many things are left out intentionally.

A third important point is that by being satisfied with the performance offered by *LEGO*-tronics (playing with general purpose building blocks, as we call it — and we really do not mean anything bad by that!), one intentionally limits oneself to a performance which, in most cases, is an order of magnitude below of what is achievable by the current ‘state of the art’ technology. Not to speak of there being only a limited amount of experience to be gained by playing just with the outside of those nice little black boxes.

A wise electronics engineer always takes some time to build a discrete model of the circuit (the most critical part, at least) in order to evaluate the influence of strays and parasitics and find a way of improving it. Even if the circuit will eventually be put on a silicon chip those strays will be scaled down, but will not disappear.

That is why we think that it is important to go back to basics.

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3.0 Introduction: *A Farewell to Exact Calculations*

The inductive peaking circuits discussed in Part 2 should be applied to some amplifier stages in order to have any sense. Today the amplifiers are made almost exclusively using semiconductor devices (**bipolar junction transistors — BJTs** and **field effect transistors — FETs**). The number of books describing semiconductor amplifiers is enormous [e.g., Ref. 3.7, 3.12, 3.13, 3.14, 3.15], whilst books discussing wideband amplifiers in necessary depth are quite rare.

Wideband amplifiers with BJTs and FETs are found in a great diversity of electronic products, in measuring instruments and oscilloscopes in particular. They require a different design approach from the 'classical' low frequency amplifier circuits, where the inter-electrode and stray capacitances are less important. In order to improve the wideband performance many special circuits were invented [e.g., Ref. 3.1, Ch.8 and 3.34, Ch.7] and to discuss thoroughly all of them in a book like this would not be possible for several reasons. Here we shall analyze only some basic circuits (the common emitter and the common base amplifiers) and some of the most used wideband circuits (e.g., the differential cascode, the common source follower, and the f_T doubler configurations; later in Part 5 we shall meet several more complex circuits).

In the first section we analyze the common emitter amplifier. Since the base pole ω_h (set by the base spread resistance r_b and the total input capacitance $C_\pi + C_M$), represents the most prevalent bandwidth limit in the transconductance equation, we discuss how to reduce the input capacitance. In this type of amplifier, as well as in all other types that we intend to discuss, the analysis becomes extremely complicated if all the parameters are considered. Since it is our intention to acquire a clear picture of the basic facts, an analysis with all the minute details would needlessly fog the view. The market is still waiting (probably in vain) for a transistor with $\pm 1\,\%$ tolerances in electrical parameters. Also, it is very difficult to specify the stray inductances and capacitances of the wiring with comparable precision. Therefore we shall simplify our expressions and neglect all the parameters which have either little influence or which must be solved numerically for a specific case. After the basic picture is acquired, the reader who wants to make a more precise analysis, can use a computer with a suitable program such as SPICE [Ref. 3.28], PSpice [Ref. 3.29], or MicroCAP [Ref. 3.30], to name a few. Be warned, however, that the result will be as good as allowed by the models of semiconductor devices and, of course, it will be influenced by the user's ability to correctly model the stray components which depend on layout and which are not explicitly shown either in the initial circuit schematic diagram or included in any semiconductor device model.

The nature of the HF impedance in the emitter circuit changes drastically if we look at it from the base, and vice versa. Since it is useful to know the possible transformations from base to emitter circuit and back, we discuss all the transformations of resistive, capacitive, and inductive impedances. Next we analyze the common base circuit. The cascode circuit, which is effectively a combination of a common emitter and a common base configuration, is often used in wideband amplifiers, so it deserves a thorough analysis, too. The same is valid for the differential cascode amplifier. We also discuss the emitter peaking in a cascode amplifier. The invention of the f_T doubler has made possible a bandwidth extension of almost twofold within a single stage and we

discuss it next. This is followed by an analysis of the JFET source follower, which is commonly used as the input stage of oscilloscopes and other measuring instruments. Such a stage can have the input impedance **negative** at high frequencies when the JFET source is loaded by a capacitor (which is always the case), and we show how to compensate this very undesirable property.

In Part 2 we have analyzed the T-coil peaking circuit with a purely capacitive tap to ground impedance. However, if the T-coil circuit is used for a transistor interstage coupling, the tap to ground impedance ceases to be purely capacitive. This fact requires a new analysis, which we deal with in the last section.

Probably, the reader will ask how accurately we need to model the active devices in our circuits to obtain a satisfying approximation. In 1954, *Ebers* and *Moll* [Ref. 3.9] had already described a relatively simple nonlinear model, which, over the years, was improved by the same authors, and by *Gummel* and *Poon* [Ref. 3.10] in 1970. Modern computer programs for circuit simulation allow the user to trade simulation speed for accuracy by selecting models with different levels of complexity (e.g., an older version of MicroCAP [Ref. 3.30] had 3 EM and 2 GP models for the BJT, the most complex GP2 using a total of 51 parameters). To simplify the circuit analysis we shall use the linearized high frequency EM2 model, explained in Sec. 3.1.

All these models look so simple and perform so well, that it seems as if anyone could have created them. Nothing could be farther from the truth. It takes lots of classical physics (*Boltzmann*'s transport theory, *Gauss*' theorem, *Poisson*'s equation, the charge current mean density integral calculus, the complicated p–n junction boundary conditions, *Maxwell*'s equations, ...), as well as quantum physics (*Fermi* levels, *Schrödinger*'s equation, the *Pauli* principle, charge generation, injection, recombination and photon–electron and phonon–electron scattering phenomena, to name just a few important topics) to be judiciously applied in order to find well defined special cases and clever approximations that would, within limits, provide a model simple enough for everyday use. Of course, if pushed too far the model fails, and there is no other way to the solution but to rework the physics neglected. In our analysis we shall try not to go that far.

It cannot be overstressed that in our analysis we are dealing with **models** of semiconductor devices! As *Philip Darrington*, former Wireless World editor, put it in one of his editorials, *"the map is not the territory"*, just as the schematic diagram is not the circuit. As in any branch of science, we build a (theoretical) model, analyze it, and then compare with the real thing; if it fits, we have had a good nose there, or perhaps we have simply been lucky; if it does not fit we go back to the drawing board.

In the macroscopic world, from which all our experience arises, most models are quite simple, since the size ratio of objects, which can still be perceived directly with our senses, to the atomic size, where some odd phenomena begin to show up, is some 6 orders of magnitude; thus the world appears to us to be smooth and continuous. However, in the world of ever shrinking semiconductor devices we are getting ever closer to the quantum phenomena (e.g., the dynamic range of our amplifiers is limited by thermal noise, which is ultimately a quantum effect). But long before we approach the quantum level we should stay alert: even if we forget that the oscilloscope probe loads our circuit with a shunt capacitance of some 10–20 pF and a serial inductance of about 70–150 nH of the ground lead, the circuit will not forget, and sometimes not forgive, either!

3.1 Common Emitter Amplifier

Fig. 3.1.1a shows a common emitter amplifier (the name reflects that the emitter is the common reference for both input and output signals), whilst Fig. 3.1.1b represents its small signal equivalent circuit (the EM2 model, see [Ref. 3.4 and 3.9]). If a signal source amplitude is much smaller than the base bias voltage, resulting in an output signal small enough compared to the supply voltage, we can assume that all the equivalent circuit components are linear (not changing with the signal). However, when the transistor has to handle large signals, the equivalent model becomes rather complicated and the analysis is usually carried out by a suitable computer program.

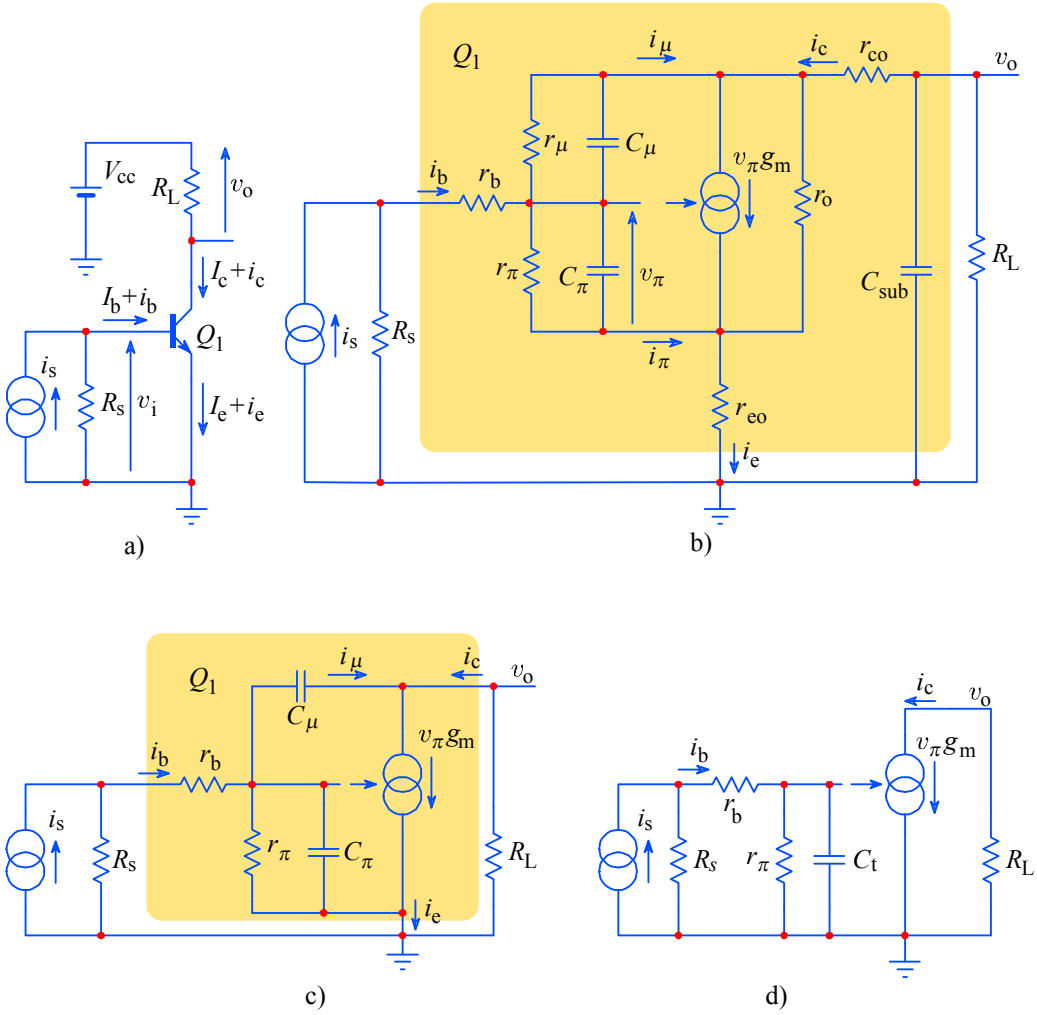

Fig. 3.1.1: The common emitter amplifier: a) circuit schematic diagram – the current and voltage vectors are drawn for the NPN type of transistor; b) high frequency small signal equivalent circuit; the components included in the Q_1 model are explained in the text; c) simplified equivalent circuit; d) an oversimplified circuit where $C_t = C_\pi + AC_\mu = \text{constant}$.

During the first steps of circuit design we can usually neglect the nonlinear effects and obtain a satisfactory performance description by using a first order approximation of the transistor model, Fig. 3.1.1c. Some of the circuit parameters can even be estimated by an oversimplified model of Fig. 3.1.1d. By assuming a certain

operating point OP, set by the DC bias conditions, we can explain the meaning of the model components. On the basis of these explanations it will become clear why and when we may neglect some of them, thus simplifying the model and its analysis.

g_m transistor mutual conductance in *siemens* [S = 1/Ω]: $g_m = \dfrac{i_c}{v_\pi} \approx 1/r_e$

where i_c is the instantaneous collector current;

v_π is the voltage across r_π (see below);

and r_e is the dynamic emitter resistance: $r_e = \dfrac{V_T}{I_e}$ [Ω] (*ohm*);

I_e is the d.c. emitter current [A] (*ampere*);

V_T is the p-n junction 'thermal' voltage $= \dfrac{k_B\, T}{q}$ [V] (*volt*);

where q is the electron charge $= 1.602 \cdot 10^{-19}$ [C] (*coulomb* = [As]);

T is the absolute temperature [K] (*kelvin*);

k_B is the Boltzmann constant $= 1.38 \cdot 10^{-23}$ [J/K] (*joule/kelvin*) (= [VAs/K]).

r_o equivalent collector–emitter output resistance, representing the variation of the collector–emitter potential due to collector signal current at a specified operating point (its value is nearly always much greater than the load):

$$r_o = \frac{v_{ce}}{i_c} = \frac{d\,V_{ce}}{d\,I_c}\bigg|_{OP} = \frac{V_A + V_{ce}}{I_c}$$

where V_A is the *Early* voltage (see Fig. 3.4.11);

In wideband amplifiers: $r_o \gg R_L$

r_μ collector to base resistance, representing the variation of the collector to base potential due to base signal current at some specified DC operating point condition OP(V_{cc}, I_b); in wideband amplifiers its value is always much larger than the source resistance or the base spread resistance:

$$r_\mu = \frac{v_{cb}}{i_b} = \frac{d\,V_{cb}}{d\,I_b}\bigg|_{OP} = \frac{V_A + V_{ce}}{I_b}$$

$$r_\mu \gg R_s + r_b$$

r_π base to emitter input resistance (forward biased BE junction), representing the variation of the base to emitter potential owed to the base signal current at a specified operating point:

$$r_\pi = \frac{v_\pi}{i_b} = \frac{d\,V_{be}}{d\,I_b}\bigg|_{OP} = \beta\,\frac{V_T}{I_c} = \frac{\beta}{g_m} \approx \beta\, r_e$$

r_b base spread resistance (resistance between the base terminal and the base–emitter junction); value range: $10\,\Omega < r_b < 200\,\Omega$.

r_{co} presumably constant collector resistance of internal bonding and external lead; approximate value $< 1\,\Omega$.

r_{eo} presumably constant emitter resistance of internal bonding and external lead; approximate value $< 1\,\Omega$.

C_μ collector–base (reverse biased) junction capacitance; usually the value is small ($< 10\,\text{pF}$); however, in the common emitter circuit it is effectively amplified by the voltage gain (the *Miller* effect, see Eq. 3.1.9).

C_π base–emitter junction effective capacitance; depends on DC bias:

$$C_\pi = g_m\,\tau_T - C_\mu$$

where τ_T is the characteristic time constant, derived from the 'transition' frequency, f_T, the frequency at which $\beta(f_T) = 1$ (see below):

$$\tau_T = \frac{1}{\omega_T} = \frac{1}{2\pi f_T}$$

C_{sub} collector to substrate capacitance; must be accounted for only in integrated circuits; in discrete devices it can be neglected.

β the transistor current gain, the collector to base current ratio; the gain frequency dependence is modeled by the characteristic time constant τ_T:

$$\beta = \frac{i_c}{i_b} = \beta_0\,\frac{1}{1 + \beta_0\, s\,\tau_T} \qquad \text{where:} \qquad \beta_0 = \frac{I_c}{I_b}$$

It is important to realize that some of those resistances are only 'equivalent resistances', or 'incremental resistances', which can be represented by a tangent to the voltage–current relation curvature at a particular bias point, and as such they are highly nonlinear for large signals. Also, the capacitances are only in part a consequence of the actual p–n junction geometry; they are dominantly volumes in the semiconductor material in which there are energy gaps capable of charge trapping, storing and releasing. In turn the gap energy is voltage dependent, so the effective capacitances are also voltage dependent and therefore also nonlinear.

With bias conditions encountered in wideband amplifier applications, the collector to base resistance r_μ and the collector to emitter resistance r_o are several orders of magnitude larger than the source resistance R_s and the load resistance R_L. In order to simplify the analysis we shall neglect r_μ and r_o; that is why they have not been drawn in Fig. 3.1.1c.

Likewise the DC power supply voltages are also not drawn, because their sources (should!) represent a short circuit for the signal, so we have simply tied the loading resistor and the bias voltages to the ground. Remember that it is the duty of the circuit designer — that is you, yourself! — to provide good power supply bypassing by both adding appropriate capacitors and using wide and short, low resistance, low inductance PCB traces.

The resistors r_{co} and r_{eo} represent the external leads and internal wires, and since their value is usually less than $1\,\Omega$, they are also neglected.

In general we can assume that small signal transistors work at an internal junction temperature of 300 K (27 °C or 80 °F, roughly the 'room temperature' increased by a few degrees owing to some small power dissipation caused by DC bias). Output

transistors work at higher temperatures, depending on the output signal amplitude, the load and the power efficiency of the amplifying stage.

It is interesting to note that $k_B T/q$ has the dimension of voltage (J=VAs, C=As and K cancels) and it has been named the junction 'thermal' voltage, its value $V_T = k_B\,T/q = 26\,\text{mV}$ at $T = 300\,\text{K}$. By assuming that the collector current I_c is almost equal to the emitter current I_e (actually $\times\,\beta/(\beta+1)$), we obtain a well known relation for the effective emitter resistance:

$$r_e = \frac{V_T}{I_e} = \frac{26\,\text{mV}}{I_e} \approx \frac{26\,\text{mV}}{I_c} \tag{3.1.1}$$

The collector to base capacitance C_μ depends on the collector to base voltage V_{cb}. In normal operating conditions (CB junction reverse biased), the corresponding relation [Ref. 3.4, 3.20] is:

$$C_\mu(V_{cb}) = \frac{C_{\mu 0}}{\left[1 + \frac{V_{cb}}{V_{jc}}\right]^{m_c}} \tag{3.1.2}$$

This equation is valid under the assumption that there is no charge in the collector to base depletion layer. The meaning of the symbols are:

$C_{\mu 0}$ = junction capacitance [F] (*farad*) (when $V_{cb} = 0$ V)

V_{cb} = collector to base voltage [V] (*volts*)

V_{jc} = collector to base barrier potential $\simeq$ 0.6–0.8 V for silicon transistors

m_c = collector voltage potential gradient factor
(0.5 for abrupt junctions and 0.33 for graded junctions)

Obviously, C_μ decreases inversely with collector voltage. For small signals (amplifier input stage) V_{cb} does not change very much, so we can assume C_μ to be constant, or, in other words, 'linear'. However, in middle stage and output transistors, V_{cb} changes considerably. As already mentioned, in such cases the computer aided circuit simulation is mandatory (after the initial linearized approximation has been found acceptable). Fortunately most transistor manufacturers provide the diagrams showing the dependence of C_μ from V_{cb}. The reader can find a very good review for 25 of the most commonly used transistors in [Ref. 3.21, p. 556].

The input base emitter capacitance C_π strongly depends on the emitter current, respectively, on the transconductance g_m. Since we can not directly access the internal base junction to measure C_π and C_μ separately, we calculate C_π from the total equivalent input capacitance C_t (see Fig. 3.1.1d), from which we first subtract C_μ:

$$C_\pi = C_t - C_\mu = g_m\,\tau_T - C_\mu = \frac{1}{2\pi f_T\,r_e} - C_\mu \tag{3.1.3}$$

where f_T is the frequency at which the (frequency dependent) current amplification factor $\beta = i_c/i_b$ is reduced to 1. Because C_μ is usually small compared to C_t we can simplify Eq. 3.1.3 to obtain:

$$C_\pi \approx \frac{1}{2\,\pi f_T\, r_e} \tag{3.1.4}$$

The product $r_e\, C_\pi$ is called the *transistor time constant* $\tau_T = 1/\omega_T$, where $\omega_T = 2\,\pi\, f_T$. The value $s_1 = -\omega_T = -1/(r_e C_\pi)$ represents the dominant pole of the amplifier and thus it is the main bandwidth limiting factor. In our further discussions we shall find the way to drastically reduce the influence of C_π, at the expense of the amplification factor.

The next problem is to calculate the input impedance. Here we must consider the *Miller effect* [Ref. 3.7, 3.12] owed to capacitance C_μ (in practice, there is also a CB leads stray capacitance, parallel to the junction capacitance, that has to be taken into account). Therefore we first calculate the input admittance looking right into the internal $r_b C_\mu$ junction in Fig. 3.1.1c. The current i_μ flowing through C_μ is:

$$i_\mu = (v_\pi - v_o)\, C_\mu\, s \tag{3.1.5}$$

where v_π is the voltage across r_π. The output voltage is[1]:

$$v_o = -\, i_c R_L = -\, g_m\, v_\pi\, R_L \tag{3.1.6}$$

By inserting Eq. 3.1.6 into Eq. 3.1.5, we obtain:

$$i_\mu = (1 + g_m\, R_L)\, s\, C_\mu\, v_\pi \tag{3.1.7}$$

and from this the junction input admittance:

$$\frac{i_\mu}{v_\pi} = (1 + g_m\, R_L)\, C_\mu\, s \tag{3.1.8}$$

From this equation it follows that the junction input impedance, owed to capacitance C_μ, is a capacitance with the value:

$$C_M = (1\ + g_m\, R_L)\, C_\mu = (1 + A_v)\, C_\mu \tag{3.1.9}$$

where $g_m\, R_L = A_v = v_o/v_i$, the voltage gain.

The capacitance C_M is called the *Miller capacitance*, after the *Miller effect* — bandwidth reduction with increasing voltage gain (the Miller effect is probably named after *John Milton Miller*, [Ref. 3.36]).

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[1] Note the negative sign in Eq. 3.1.6: actually, the output voltage is $v_o = V_{cc} - i_c R_L$. However, since we have agreed to replace the supply voltage with a short circuit, we are left with the negative part only.

When the voltage gain is large the effect of C_μ (and, respectively, C_M) becomes prevalent. However, there are ways of reducing the effect of $A_\mathrm{v}\,C_\mu$ (by lowering the voltage gain or by using other circuit configurations); we discuss it in later sections.

The complete input impedance that the signal source would see at the base is:

$$Z_\mathrm{b} = r_\mathrm{b} + \frac{1}{\dfrac{1}{r_\pi} + sC_\pi + sC_\mathrm{M}} = r_\mathrm{b} + \frac{r_\pi}{1 + s(C_\pi + C_\mathrm{M})\,r_\pi} \qquad (3.1.10)$$

3.1.1 Calculation of voltage amplification (based on Fig. 3.1.1d)

On the basis of the analysis made so far, we come to the conclusion that the two capacitances C_π and C_μ (effectively C_M) are connected in parallel in the base circuit. We can simply add them together and consider their sum to be C_t. This has been drawn in Fig. 3.1.1d. This equivalent circuit is appropriate for the calculation of both input impedance and the transimpedance. But since we have removed any connection between the output and input (where C_μ is effective), this circuit **is not suitable** for the calculation of output impedance. Therefore when calculating the voltage gain we must also consider the pole $s_2 \simeq -1/R_\mathrm{L}C_\mu$ on the collector side, according to Fig. 3.1.1c (in general, some collector to ground stray capacitance must be added to C_μ, but for the time being, we shall write only C_μ).

According to Fig. 3.1.1d, thus neglecting the pole s_2, but including the source impedance R_s, we have:

$$\frac{v_\mathrm{i} - v_\pi}{R_\mathrm{s} + r_\mathrm{b}} = v_\pi\left(\frac{1}{r_\pi} + s\,C_\mathrm{t}\right) \qquad (3.1.11)$$

From this we can express v_π as:

$$v_\pi = v_\mathrm{i}\frac{r_\pi}{r_\pi + R_\mathrm{s} + r_\mathrm{b} + s\,C_\mathrm{t}\,r_\pi(R_\mathrm{s} + r_\mathrm{b})} \qquad (3.1.12)$$

The output voltage is:

$$v_\mathrm{o} = -\,g_\mathrm{m}\,v_\pi\,R_\mathrm{L} = -\,g_\mathrm{m}\,R_\mathrm{L}\frac{r_\pi}{r_\pi + R_\mathrm{s} + r_\mathrm{b} + s\,C_\mathrm{t}\,r_\pi(R_\mathrm{s} + r_\mathrm{b})}\,v_\mathrm{i} \qquad (3.1.13)$$

and the voltage amplification is:

$$A_\mathrm{v} = \frac{v_\mathrm{o}}{v_\mathrm{i}} = -\,g_\mathrm{m}\,R_\mathrm{L}\frac{r_\pi}{r_\pi + R_\mathrm{s} + r_\mathrm{b} + s\,C_\mathrm{t}\,r_\pi(R_\mathrm{s} + r_\mathrm{b})} \qquad (3.1.14)$$

We would like to separate the frequency dependent part of A_v from the frequency independent part, in a normalized form, as:

$$A_\mathrm{v}(s) = A_0\,\frac{-\,s_1}{s - s_1} \qquad (3.1.15)$$

where A_0 is the DC gain and s_1 is the system's pole.

To achieve this separation we first divide both the numerator and the denominator of Eq. 3.1.14 by $C_t\, r_\pi (R_s + r_b)$:

$$A_v = -\, g_m\, R_L \frac{-\,\dfrac{r_\pi}{C_t\, r_\pi (R_s + r_b)}}{s - \left(-\,\dfrac{r_\pi + R_s + r_b}{C_t\, r_\pi (R_s + r_b)}\right)} \tag{3.1.16}$$

To make the two ratios equal we must multiply the numerator by $(r_\pi + R_s + r_b)/r_\pi$ and then multiply the whole by the reciprocal:

$$A_v = -\, g_m\, R_L \frac{-\,\dfrac{r_\pi}{C_t\, r_\pi (R_s + r_b)} \cdot \dfrac{r_\pi + R_s + r_b}{r_\pi}}{s - \left(-\,\dfrac{r_\pi + R_s + r_b}{C_t\, r_\pi (R_s + r_b)}\right)} \cdot \frac{r_\pi}{r_\pi + R_s + r_b} \tag{3.1.17}$$

We rearrange this to obtain:

$$A_v = -\,\frac{g_m\, R_L\, r_\pi}{r_\pi + R_s + r_b} \cdot \frac{-\,\dfrac{r_\pi + R_s + r_b}{C_t\, r_\pi (R_s + r_b)}}{s - \left(-\,\dfrac{r_\pi + R_s + r_b}{C_t\, r_\pi (R_s + r_b)}\right)} \tag{3.1.18}$$

and by comparing this with Eq. 3.1.15 the DC gain is:

$$A_0 = -\,\frac{g_m\, R_L\, r_\pi}{r_\pi + R_s + r_b} \tag{3.1.19}$$

and the pole s_1 is:

$$s_1 = -\,\frac{R_s + r_b + r_\pi}{(R_s + r_b)\, r_\pi\, C_t} \tag{3.1.20}$$

Since s_1 is a simple real pole it is equal to the system's upper half power frequency:

$$\begin{aligned} \omega_h = |s_1| &= \frac{R_s + r_b + r_\pi}{(R_s + r_b)\, r_\pi} \cdot \frac{1}{C_t} \\ &= \left(\frac{1}{R_s + r_b} + \frac{1}{r_\pi}\right) \cdot \frac{1}{C_\pi + (1 + g_m\, R_L)\, C_\mu} \end{aligned} \tag{3.1.21}$$

and it can be seen that it is **inversely proportional to all the components**: R_s, r_b, r_π, C_π, C_μ, g_m, and R_L.

If $R_s + r_b \ll r_\pi$ and if R_L is very small the approximate value of the pole is:

$$|s_1| \approx \frac{1}{r_\pi\, C_\pi} = \frac{1}{\beta_0} \cdot \frac{g_m}{C_\pi} = \frac{\omega_T}{\beta_0} \tag{3.1.22}$$

where $\beta_0 = I_c / I_b$, the DC current amplification factor.

Before more sophisticated circuits were invented, the common emitter amplifier was used extensively (with many amplifier designers having hard times and probably cursing both C_π and C_μ). In 1956 *G. Bruun* [Ref. 3.22] thoroughly analyzed this type of amplifier with the added shunt–series inductive peaking circuit. In view of modern wideband amplifier circuits, this reference is only of historical value today. Nevertheless, the common emitter stage represents a good starting point for the discussion of more efficient wideband amplifier circuits.

3.2 Transistor as an Impedance Converter

In the previous section we have realized that the amplification factor is frequency dependent, decreasing with frequency above some upper frequency limit (asymptotically to $-20\,\mathrm{dB}/10f$, just like a first-order low pass system). This can help us to derive different impedance transformations from the emitter to the base circuit and back [Ref. 3.1, 3.2]. Knowing the possible transformations is extremely useful in the wideband amplifier design. We are going to show how the nature of the impedance changes with these transformations. A capacitive impedance may become inductive and positive impedances may occasionally become negative!

3.2.1 Common base small signal transistor model

As we explained in Sec. 3.1, if the voltage gain is not too high the base emitter capacitance C_π is the dominant cause of the frequency response rolling off at high frequencies. By considering this we can make a simplified small signal high frequency transistor model, as shown in Fig. 3.2.1, for the common base configuration, where i_c, i_e and i_b are the collector-, emitter-, and base-current respectively. For this figure the DC current amplification factor is:

$$\alpha_0 = \frac{I_\mathrm{c}}{I_\mathrm{e}} \tag{3.2.1}$$

Initially we have written $g_\mathrm{m} \approx 1/r_\mathrm{e}$. A better expression for mutual conductance is:

$$g_\mathrm{m} = \frac{\alpha_0}{r_\mathrm{e}} = \frac{\beta_0}{(1+\beta_0)\,r_\mathrm{e}} \tag{3.2.2}$$

where β_0 is the common emitter DC current amplification factor. If $\beta_0 \gg 1$ then $\alpha_0 \simeq 1$, so the collector current I_c is almost equal to the emitter current I_e, and $g_\mathrm{m} \simeq 1/r_\mathrm{e}$. This simplification is often used in practice.

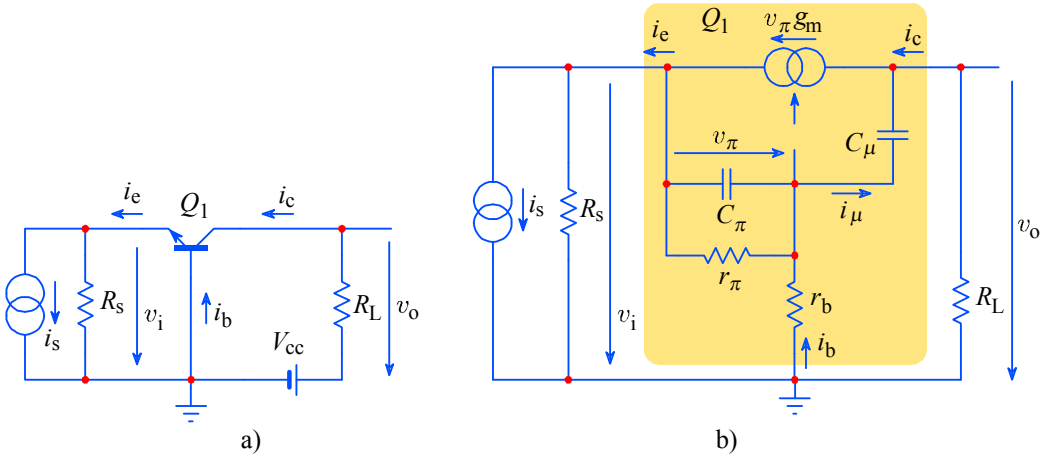

Fig. 3.2.1: The common base amplifier: a) circuit schematic diagram; b) high frequency small signal equivalent circuit.

For the moment let us assume that the base resistance $r_b = 0$ and consider the low frequency relations. The input resistance is:

$$r_\pi = \frac{v_\pi}{i_b} \tag{3.2.3}$$

where v_π is the base to emitter voltage. Since the emitter current is:

$$i_e = i_b + i_c = i_b + \beta_0\, i_b = i_b\,(1 + \beta_0) \tag{3.2.4}$$

then the base current is:

$$i_b = \frac{i_e}{1 + \beta_0} \tag{3.2.5}$$

and consequently:

$$r_\pi = \frac{v_\pi\,(1 + \beta_0)}{i_e} = r_e\,(1 + \beta_0) \approx \beta_0\, r_e \tag{3.2.6}$$

The last simplification is valid if $\beta_0 \gg 1$. To obtain the input impedance at high frequencies the parallel connection of C_π must be taken into account:

$$Z_b = \frac{(1 + \beta_0)\, r_e}{1 + (1 + \beta_0)\, s\, C_\pi\, r_e} \tag{3.2.7}$$

The base current is:

$$i_b = \frac{v_\pi}{Z_b} = v_\pi\, \frac{1 + (1 + \beta_0)\, s\, C_\pi\, r_e}{(1 + \beta_0)\, r_e} \tag{3.2.8}$$

Therefore v_π is:

$$v_\pi = i_b\, \frac{(1 + \beta_0)\, r_e}{1 + (1 + \beta_0)\, s\, C_\pi\, r_e} \tag{3.2.9}$$

Consequently, the collector current is:

$$i_c = g_m\, v_\pi = \frac{\beta_0}{1 + \beta_0} \cdot \frac{1}{r_e}\, v_\pi = \frac{\alpha_0}{r_e}\, v_\pi \tag{3.2.10}$$

If we put Eq. 3.2.9 into Eq. 3.2.10 we obtain:

$$\begin{aligned} i_c &= i_b\, \frac{\beta_0}{1 + \beta_0} \cdot \frac{1}{r_e} \cdot \frac{(1 + \beta_0)\, r_e}{1 + s\,(1 + \beta_0)\, r_e\, C_\pi} \\ &= i_b\, \frac{1}{\dfrac{1}{\beta_0} + s \left(\dfrac{\beta_0 + 1}{\beta_0} \right) r_e\, C_\pi} \\ &\approx i_b\, \frac{1}{\dfrac{1}{\beta_0} + s\, \tau_T} = i_b\, \beta(s) \end{aligned} \tag{3.2.11}$$

In the very last expression we assumed that $\beta_0 \gg 1$ and $\tau_T = r_e\, C_\pi = 1/\omega_T$, where $\omega_T = 2\pi f_T$ is the angular frequency at which the current amplification factor β decreases to unity. The parameter τ_T, and consequently ω_T, depend on the internal configuration and structure of the transistor. Fig. 3.2.2 shows the frequency dependence of β and the equivalent current generator.

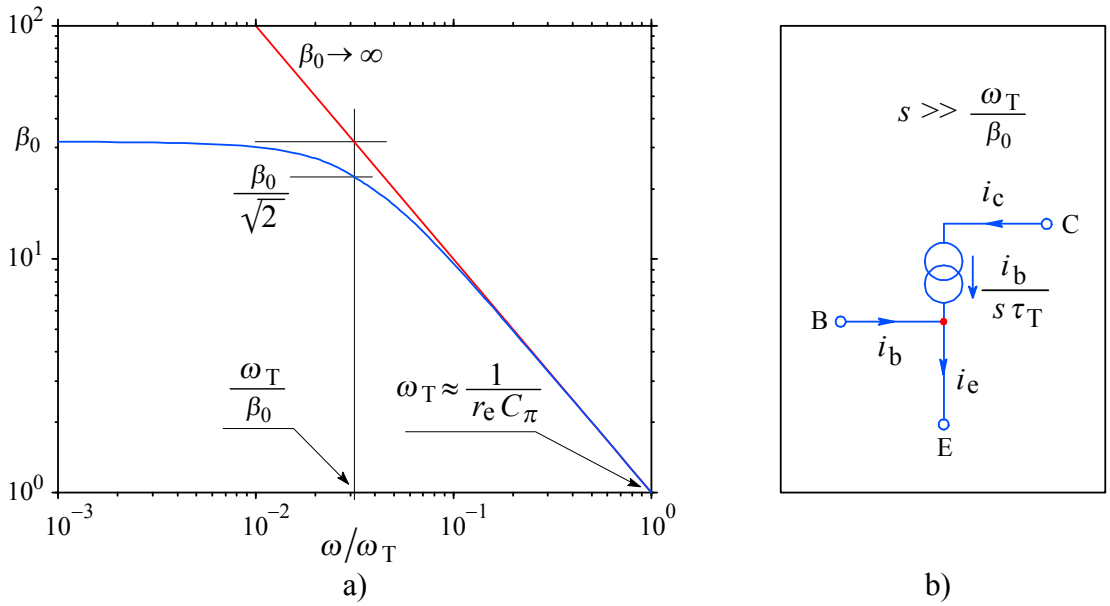

Fig. 3.2.2: a) The transistor gain as a function of frequency, modeled by the Eq. 3.2.11; b) the equivalent HF current generator.

In order to correlate Fig. 3.2.2 with Eq. 3.2.11 we rewrite it as:

$$\frac{i_c}{i_b} \approx \beta_0 \frac{-\frac{\omega_T}{\beta_0}}{s - \left(-\frac{\omega_T}{\beta_0}\right)} = \beta_0 \frac{-s_1}{s - s_1} \tag{3.2.12}$$

where s_1 is the pole at $-\omega_T/\beta_0$. This relation will become useful later, when we shall apply one of the peaking circuits (from Part 2) to the amplifier. At very high frequencies, or if $\beta_0 \gg 1$, the term $s\,\tau_T$ prevails. In this case, from Eq. 3.2.11:

$$\frac{i_c}{i_b} = \beta(s) \approx \frac{1}{s\,\tau_T} = \frac{1}{j\,\omega\,r_e\,C_\pi} \tag{3.2.13}$$

Obviously β is decreasing with frequency. By definition, at $\omega = \omega_T$ the current ratio $i_c/i_b = 1$; then the capacitance C_π can be found as:

$$C_\pi \approx \frac{1}{\omega_T\,r_e} \tag{3.2.14}$$

This simplified relation represents the $-20\,\mathrm{dB}/10f$ asymptote in Fig. 3.2.2a.

3.2.2 The conversion of impedances

We can use the result of Eq. 3.2.11 to transform the transistor internal (and the added external) impedances from the emitter to the base circuitry, and vice versa. Suppose we have the impedance Z_e in the emitter circuit, as displayed in Fig. 3.2.3a, and we are interested in the corresponding base impedance Z_b:

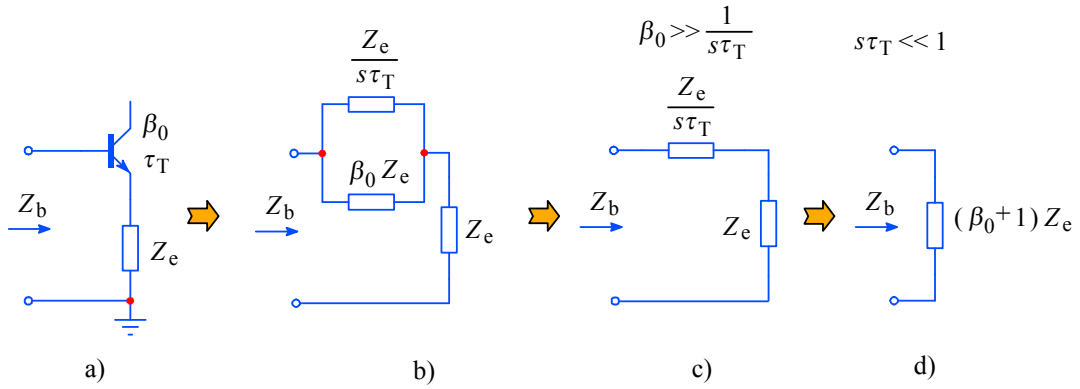

Fig. 3.2.3: Emitter to base impedance conversion: a) schematic; b) equivalent circuit; c) simplified for high β_0; d) simplified for low frequencies.

We know that:

$$Z_b = \beta(s)\, Z_e + Z_e = \left[\, \beta(s) + 1 \,\right] Z_e \tag{3.2.15}$$

If we insert $\beta(s)$ according to Eq. 3.2.11, we obtain:

$$Z_b = \frac{Z_e}{\dfrac{1}{\beta_0} + s\,\tau_T} + Z_e \tag{3.2.16}$$

The admittance of the first part of this equation is:

$$Y = \frac{\dfrac{1}{\beta_0} + s\,\tau_T}{Z_e} = \frac{1}{\beta_0\, Z_e} + \frac{s\,\tau_T}{Z_e} \tag{3.2.17}$$

and this represents a parallel connection of impedances $\beta_0\, Z_e$ and $Z_e/s\,\tau_T$. By adding the series impedance Z_e, as in Eq. 3.2.16, we obtain the equivalent circuit of Fig. 3.2.3b. At medium frequencies and with a high value of β_0 we can assume that $1/\beta_0 \ll s\,\tau_T$, so we can delete the impedance $\beta_0 Z_e$ and simplify the circuit, as in Fig. 3.2.3c. On the other hand, at low frequencies, where $s\,\tau_T \ll 1$, we can neglect the $Z_e/s\,\tau_T$ component and get a very basic equivalent circuit, displayed in Fig. 3.2.3d.

Eq. 3.2.11 is equally useful when we want to transform the impedance from the base into the emitter circuit as shown in Fig. 3.2.4a. In this case we have:

$$Z_e = \frac{Z_b}{\beta(s) + 1} \tag{3.2.18}$$

Again we calculate the admittance, which is:

$$Y_e = \frac{\beta(s)+1}{Z_b} = [\beta(s)+1]\,Y_b = \beta(s)\,Y_b + Y_b \tag{3.2.19}$$

The first part of this admittance is:

$$Y = \frac{\beta(s)}{Z_b} = \frac{Y_b}{\frac{1}{\beta_0} + s\,\tau_T} = \frac{1}{Z_b} \cdot \frac{1}{\frac{1}{\beta_0} + s\,\tau_T} \tag{3.2.20}$$

and the impedance is:

$$Z = \frac{Z_b}{\beta_0} + s\,\tau_T\,Z_b \tag{3.2.21}$$

Thus the transformed impedance Z_e is composed of three elements: the series connection of Z_b/β_0 and $s\,\tau_T\,Z_b$, in parallel with the impedance Z_b.

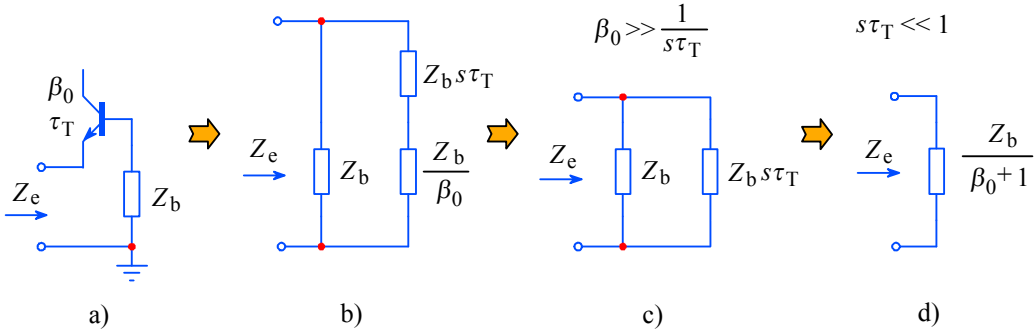

Fig. 3.2.4: Base to emitter impedance conversion: a) schematic; b) equivalent circuit; c) simplified for high β_0 or for $f \simeq f_T$; d) simplified for low frequencies.

The equivalent emitter impedance is shown in Fig. 3.2.4b.

As in the previous example, for some specific conditions the circuit can be simplified. At medium frequencies and a high β_0, we can assume $\beta_0 \gg 1/s\,\tau_T$ and therefore neglect the impedance Z_b/β_0, as in Fig. 3.2.4c. At low frequencies, where $s\,\tau_T \ll 1$, the impedance $Z_b/(\beta_0+1)$ prevails and we can neglect the parallel impedance Z_b, as in Fig. 3.2.4d.

3.2.3 Examples of impedance transformations

The most interesting examples of impedance transformations are the emitter to base transformation of a capacitive emitter impedance and the base to emitter transformation of an inductive base impedance.

In the first case we have $Z_e = 1/s\,C$, where C is the emitter to ground capacitance.

To obtain the base impedance we apply Eq. 3.2.5:

$$Z_\mathrm{b} = \frac{\beta(s)+1}{s\,C} = \left[\frac{1}{\dfrac{1}{\beta_0}+s\,\tau_\mathrm{T}}+1\right]\frac{1}{s\,C} = \frac{\dfrac{1}{\beta_0}+s\,\tau_\mathrm{T}+1}{\left(\dfrac{1}{\beta_0}+s\,\tau_\mathrm{T}\right)s\,C}$$

$$= \frac{s\,\tau_\mathrm{T}+\left(1+\dfrac{1}{\beta_0}\right)}{s^2\tau_\mathrm{T}\,C+\dfrac{s\,C}{\beta_0}} \qquad (3.2.22)$$

The inverse of Z_b is the admittance:

$$Y_\mathrm{b} = \frac{s^2\tau_\mathrm{T}\,C+\dfrac{s\,C}{\beta_0}}{s\,\tau_\mathrm{T}+\left(1+\dfrac{1}{\beta_0}\right)} \qquad (3.2.23)$$

Let us synthesize this expression by a simple continued fraction expansion [Ref. 3.27]:

$$\frac{s^2\tau_\mathrm{T}\,C+\dfrac{s\,C}{\beta_0}}{s\,\tau_\mathrm{T}+\left(1+\dfrac{1}{\beta_0}\right)} = s\,C - \frac{s\,C}{s\,\tau_\mathrm{T}+\left(1+\dfrac{1}{\beta_0}\right)} \qquad (3.2.24)$$

The fraction on the right is a negative admittance with the corresponding impedance:

$$Z'_\mathrm{b} = -\frac{s\,\tau_\mathrm{T}+\left(1+\dfrac{1}{\beta_0}\right)}{s\,C} = -\frac{\tau_\mathrm{T}}{C} - \frac{1+\dfrac{1}{\beta_0}}{s\,C} \qquad (3.2.25)$$

It is evident that this impedance is a series connection of a negative resistance:

$$R_\mathrm{n} = -\frac{\tau_\mathrm{T}}{C} = -r_\mathrm{e}\,\frac{C_\pi}{C} \qquad (3.2.26)$$

and a negative capacitance:

$$C_\mathrm{n} = -\frac{C}{1+\dfrac{1}{\beta_0}} = -\frac{\beta_0}{1+\beta_0}\,C = -\alpha_0\,C \qquad (3.2.27)$$

By adding the positive parallel capacitance C, as required by Eq. 3.2.24, we obtain the equivalent circuit which is shown in Fig. 3.2.5. Since we deal with an active circuit (transistor) it is quite normal to encounter negative impedances. The complete base admittance is then:

$$Y_\mathrm{b} = s\,C - \frac{1}{\dfrac{\tau_\mathrm{T}}{C}+\dfrac{1}{s\,\alpha_0\,C}} \qquad (3.2.28)$$

By rearranging this expression and substituting $s = j\omega$ we can separate the real and imaginary parts, obtaining:

$$Y_\mathrm{b} = \Re\{Y_\mathrm{b}\} + j\Im\{Y_\mathrm{b}\} = G_\mathrm{b} + j\omega C_\mathrm{b}$$

$$= -\frac{\frac{\tau_\mathrm{T}}{C}}{\tau_\mathrm{T}^2 + \frac{1}{\omega^2\alpha_0^2}} - j\omega C\,\frac{\tau_\mathrm{T}^2 - \frac{\alpha_0 - 1}{\omega^2\alpha_0^2}}{\tau_\mathrm{T}^2 + \frac{1}{\omega^2\alpha_0^2}} \tag{3.2.29}$$

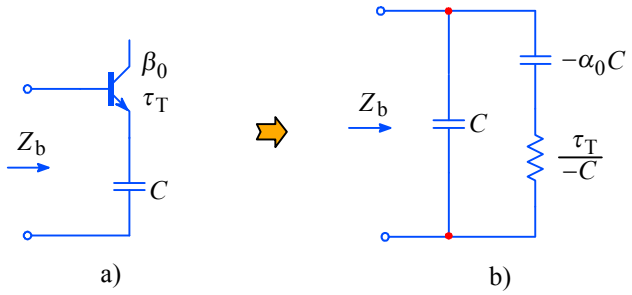

Fig. 3.2.5: A capacitive emitter load is reflected into the base (junction) with **negative** components.

The negative input (base) conductance G_b can cause ringing on steep signals or even continuous oscillations if the signal source impedance has an emphasized inductive component. We shall thoroughly discuss this effect and its compensation later, when we shall analyze the emitter–follower (i.e., common collector) and the JFET source–follower amplifiers.

Now let us derive the emitter impedance Z_e in the case in which the base impedance is inductive ($s\,L$). Here we apply Eq. 3.2.18:

$$Z_\mathrm{e} = \frac{s\,L}{\beta(s)+1} = \frac{s\,L}{\frac{1}{\frac{1}{\beta_0} + s\,\tau_\mathrm{T}} + 1} = \tag{3.2.30}$$

$$= \frac{s\,L\left(\frac{1}{\beta_0} + s\,\tau_\mathrm{T}\right)}{1 + \frac{1}{\beta_0} + s\,\tau_\mathrm{T}} = \frac{s^2 L\,\tau_\mathrm{T} + \frac{s\,L}{\beta_0}}{s\,\tau_\mathrm{T} + \left(1 + \frac{1}{\beta_0}\right)} \tag{3.2.31}$$

By continued fraction expansion we obtain:

$$\frac{s^2 L\,\tau_\mathrm{T} + \frac{s\,L}{\beta_0}}{s\,\tau_\mathrm{T} + \left(1 + \frac{1}{\beta_0}\right)} = s\,L - \frac{s\,L}{s\,\tau_\mathrm{T} + \left(1 + \frac{1}{\beta_0}\right)} \tag{3.2.32}$$

The negative part of the result can be inverted to obtain the admittance:

$$Y'_\mathrm{e} = -\frac{s\,\tau_\mathrm{T} + \left(1 + \frac{1}{\beta_0}\right)}{s\,L} = -\frac{\tau_\mathrm{T}}{L} - \frac{1 + \frac{1}{\beta_0}}{s\,L} \tag{3.2.33}$$

This means we have two parallel impedances. The first one is a **negative** resistance:

$$R_x = -\frac{L}{\tau_T} \tag{3.2.34}$$

and the second one is a **negative** inductance:

$$L_x = -\frac{L}{1+\frac{1}{\beta_0}} = -\frac{\beta_0}{1+\beta_0} L = -\alpha_0 L \tag{3.2.35}$$

As required by Eq. 3.2.32, we must add the inductance L in series, thus arriving at the equivalent emitter impedance shown in the figure below:

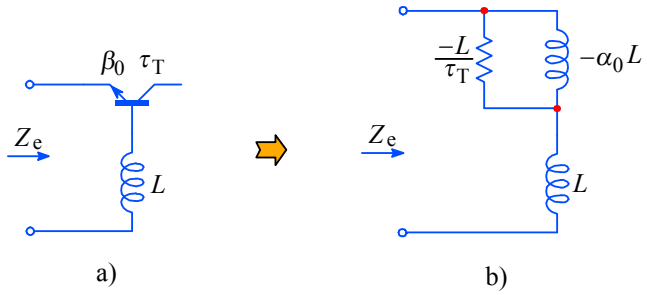

Fig. 3.2.6: The inductive source is reflected into the emitter with **negative** components.

We have just analyzed an important aspect of a common base amplifier, with an inductance (i.e., long lead) between the base and ground. The negative resistance, as given by Eq. 3.2.34, may become the reason for ringing or oscillations if the driving circuit seen by the emitter has a capacitive character. We shall discuss this problem more thoroughly when we shall analyze the cascode circuit.

In a way similar to those used for deriving the previous two results, we can transform other impedance types from emitter to base, and vice versa. The Table 3.2.1 displays the six possible variations and the reader is encouraged to derive the remaining four, which we have not discussed.

Note that all the three transformations for the common base circuit in the table apply to the base–emitter **junction** to ground only. In order to obtain the correct base **terminal** to ground impedance the transistor base spread resistance r_b must be added in series to the circuits shown in the table.

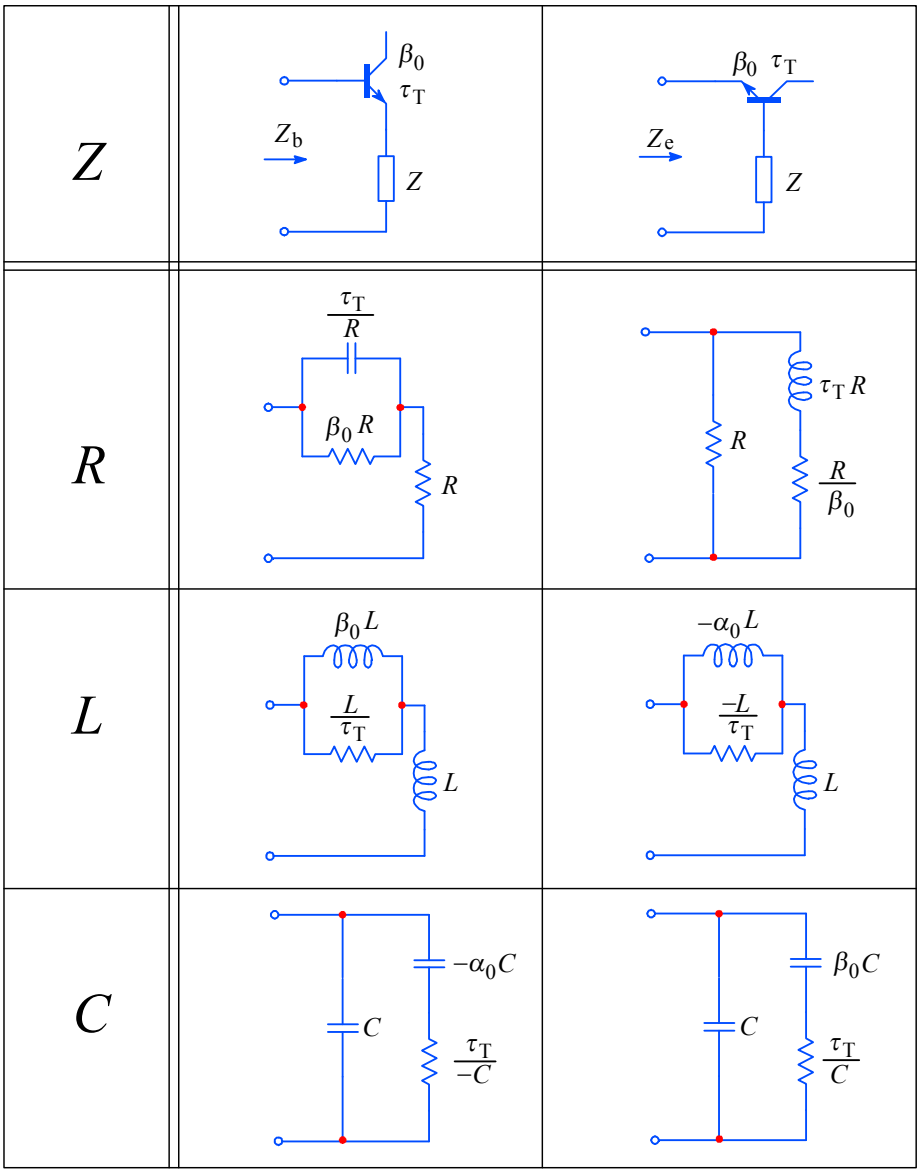

Table 3.2.1: The Table of impedance conversions [Ref. 3.8].

3.2.4 Transformation of combined impedances

The Table 3.2.1 can also help us in transforming impedances consisting of two or more components.

Example 1:

Suppose we have a parallel $R_b C_b$ combination in the base circuit, as shown in Fig. 3.2.7a. What is the emitter impedance Z_e if the common base transistor has a current amplification factor β_0 and the time constant τ_T ($= 1/\omega_T$)?

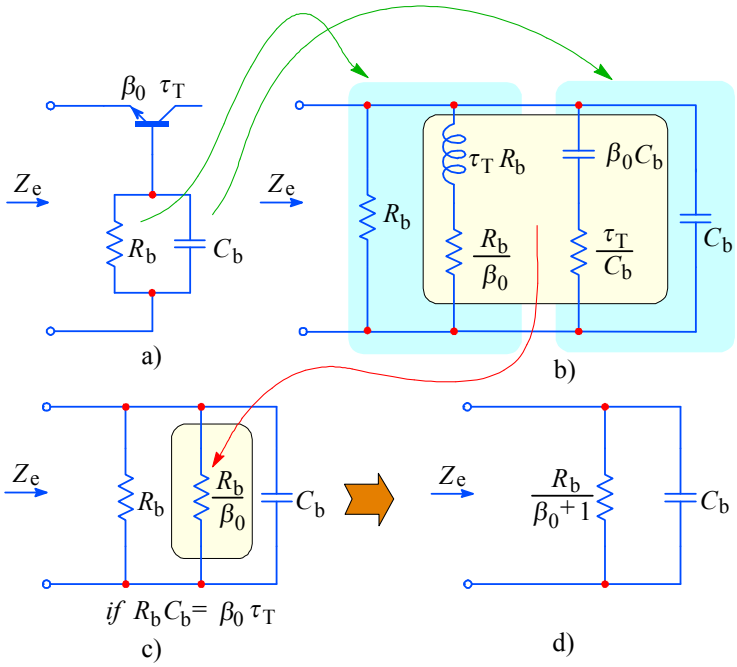

Fig. 3.2.7: Base to emitter RC network transformation: a) schematic; b) equivalent circuit; c) if $R_b C_b = \beta_0 \tau_T$ the middle components form a resistance; d) final equivalent circuit.

From the Table 3.2.1 we first transform the resistance R_b from base to emitter and obtain what is shown on the left half of Fig. 3.2.7b. Then we transform the capacitance C_b and obtain the right half of Fig. 3.2.7b. If we want the transformed network to have the smallest possible influence in the emitter circuit, we can apply the principle of constant resistance network (L and C cancel each other when $RC = L/R$, [Ref. 3.27]). To do so let us focus on both middle branches of the transformed network, where we select such values of R_b and C_b that:

$$\sqrt{\frac{R_b\,\tau_T}{C_b\,\beta_0}} = \frac{R_b}{\beta_0} \tag{3.2.36}$$

which is resolved as:

$$R_b\,C_b = \tau_T\,\beta_0 \tag{3.2.37}$$

With such values of R_b and C_b the middle two branches obtain the form of a resistor with the value R_b/β_0, as shown in Fig. 3.2.7c, which allows us to further simplify the complete circuit to that in Fig. 3.2.7d.

To acquire a feeling for practical values, let us make a numerical example. Our transistor has:

$$\beta_0 = 80 \qquad f_T = 600\,\text{MHz} \qquad R_b = 47\,\Omega$$

where R_b is the external base resistance, as in Fig. 3.2.7.

What should be the value of the capacitance C_b, connected in parallel with R_b, which would fulfill the requirement expressed by Eq. 3.2.36?

We start by calculating the transistor time constant:

$$\tau_T = \frac{1}{\omega_T} = \frac{1}{2\,\pi\,f_T} = \frac{1}{2\,\pi\cdot 600\cdot 10^6} = 265\,\text{ps} \tag{3.2.38}$$

Then we calculate the capacitance by using Eq. 3.2.37:

$$C_b = \frac{\tau_T\,\beta_0}{R_b} = \frac{265\cdot 10^{-12}\cdot 80}{47} = 451\,\text{pF} \tag{3.2.39}$$

The equivalent parallel resistance, R_q, according to Fig. 3.2.7d, is:

$$R_q = \frac{R_b}{1+\beta_0} = \frac{47}{1+80} = 0.58\,\Omega \tag{3.2.40}$$

The time constant of the equivalent circuit, τ_q, is:

$$\tau_q = R_q\,C_b = 0.56\cdot 451\cdot 10^{-12} = 261.58\,\text{ps} \tag{3.2.41}$$

whilst the base time constant is:

$$\tau_b = R_b\,C_b = 47\cdot 451\cdot 10^{-12} = 21.197\,\text{ns} \tag{3.2.42}$$

and the ratio of time constants is:

$$\frac{\tau_b}{\tau_q} = \beta_0 + 1 \tag{3.2.43}$$

We shall consider these results in the design of the common base amplifier and of the cascode amplifier.

Example 2:

By using the same principles as we have used above, we shall take another example, which is also very important for the wideband amplifier design. We shall transform a parallel combination R_eC_e, as shown in Fig. 3.2.8a, from emitter to base. With the data from Table 3.2.1, we can draw the transformed base network separately for R_e and C_e and then connect them in parallel. This is shown in Fig. 3.2.8b. Now we

focus only on the middle part of the circuit, which is drawn in Fig. 3.2.8c. If we select such values of $R_e C_e$ that:

$$R_e C_e = \tau_T \tag{3.2.44}$$

and if we consider that $\alpha_0 \approx 1$, then the admittance Y of the middle part of the circuit becomes zero, because in this case:

$$R_e = -\frac{\tau_T}{C_e} \tag{3.2.45}$$

and:

$$\frac{\tau_T}{R_e} = -\alpha_0 C_e \approx -C_e \tag{3.2.46}$$

and the parallel connection of a positive and an equal negative admittance gives zero admittance:

$$Y = \frac{1}{R_e + \dfrac{1}{s\dfrac{\tau_T}{R_e}}} + \frac{1}{-\dfrac{\tau_T}{C_e} - \dfrac{1}{s C_e}} = 0 \Bigg|_{R_e C_e = \tau_T} \tag{3.2.47}$$

A zero admittance is an infinite impedance. So in this case the only components that remain are the parallel connection of C_e and $(\beta_0 + 1)R_e$, as in Fig. 3.2.9d.

Note that this transformation was carried out by taking the **internal base junction** as the viewing point. The actual input impedance at the external base terminal will be equal to the parallel RC combination of Fig. 3.2.8d to which the series connected base spread resistance r_b must be added.

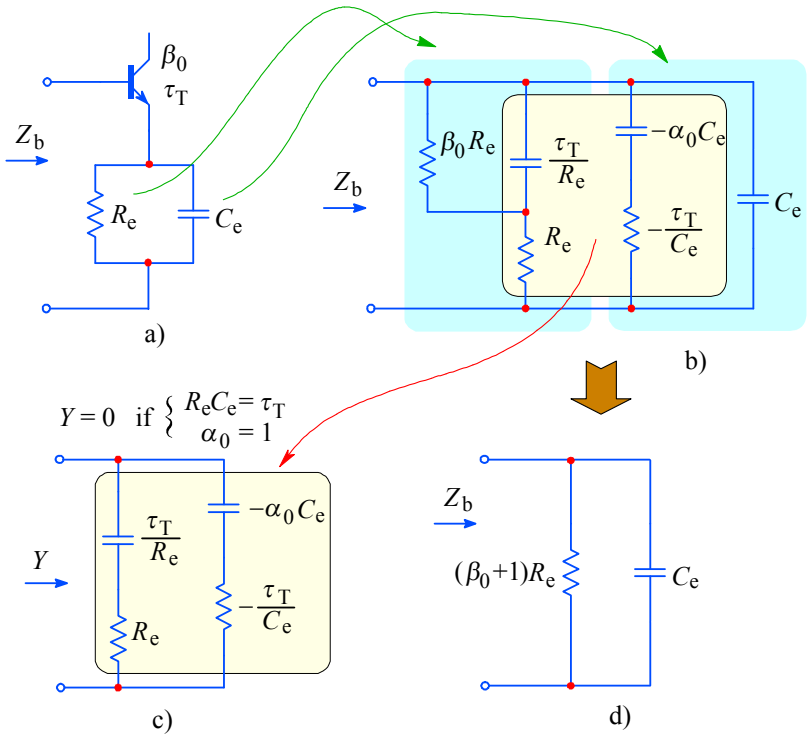

Fig. 3.2.8: Transformation of the emitter RC network as seen from the base: a) schematic; b) equivalent circuit; c) if $RC = \tau_T$ and $\alpha_0 = 1$, the sum of the middle frame component's admittances is zero; d) final equivalent circuit.

The transformation in Fig. 3.2.8 allows us to trade the gain of a common emitter circuit for the reduced input capacitance. Instead of C_π (large) with the emitter grounded, the input capacitance is now equal to the capacitance C_e (small) which we have inserted in the emitter circuit. Of course, we still have to add the base to collector capacitance C_μ or Miller capacitance C_M. As we shall see in the Sec. 3.4, where we shall discuss the cascode amplifier, the gain is reduced in proportion to R_L/R_e. Since in a wideband amplifier stage we almost never exceed the voltage gain of ten, we can always apply the above transformation.

For a numerical example let us use the same transistor as before ($\beta_0 = 80$, $f_T = 600\,\text{MHz}$). According to Eq. 3.2.38 the corresponding τ_T is 265 ps. Let us say that on the basis of the desired current gain of the common-emitter stage we select an emitter resistor $R_e = 100\,\Omega$. What is the value of the parallel emitter capacitance C_e which would give the input impedance according to Fig. 3.2.8d?

Since $R_e\,C_e = \tau_T = 265\,\text{ps}$, it follows that:

$$C_e = \frac{\tau_T}{R_e} = \frac{256 \cdot 10^{-12}}{100} = 2.65\,\text{pF} \quad \text{only!} \tag{3.2.48}$$

If the stage has an emitter current $I_e = 10\,\text{mA}$, then:

$$r_e = \frac{26\,\text{mV}}{10\,\text{mA}} = 2.6\,\Omega \tag{3.2.49}$$

Without the R_eC_e network in the emitter, the base to emitter capacitance C_π would define the bandwidth and its estimated value would be (Eq. 3.1.4):

$$C_\pi = \frac{1}{2\,\pi\,r_e\,f_T} = \frac{1}{2\,\pi\,\cdot 2.6 \cdot 600 \cdot 10^6} = 102\ \text{pF} \tag{3.2.50}$$

By introducing the $R_e\,C_e$ network in the emitter circuit, we have reduced the base to emitter capacitance, seen by the input current, by $102/2.65 = 38.5$ times! Of course, to our 2.65 pF we must add in parallel the capacitance $C_M = C_\mu\,(1 + A_v)$ and the base spread resistance r_b in series with this network to obtain a more accurate input impedance. Since now the collector to base capacitance C_μ has become significant, especially because it is 'magnified' $(1 + A_v)$ times, we must look for some methods to reduce its effect as much as possible. We shall discus this in the following sections.

Owing to R_e the input resistance is increased to:

$$R_i \simeq (1 + \beta_0)\,R_e = (1 + 80)\,100 = 8100\,\Omega \tag{3.2.51}$$

Here, too, we have neglected the base resistance r_b; it must be added to the value above to obtain a more accurate figure.

In Fig. 3.2.9a the transistor stage with R_eC_e is shown again and in Fig. 3.2.9b is its small signal equivalent input circuit.

In wideband amplifiers we usually make the emitter network with $C_e \leq 20\,\text{pF}$. In order to match $R_e\,C_e = \tau_T$ the capacitor C_e is often made adjustable, because τ_T in commercially available transistors have rather large tolerances.

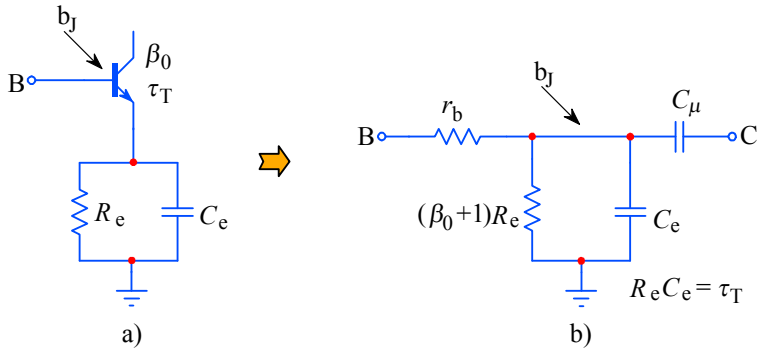

Fig. 3.2.9: R_eC_e network transformation: a) schematic; b) equivalent circuit. The symbol b_J represents the internal base junction.

With an appropriate R_L in the collector (not shown in Fig. 3.2.9) we might now calculate the (decreased) voltage amplification A_v owed to the R_eC_e network in the emitter circuit of the common emitter stage and consider the decreased value of the Miller capacitance C_M. Since we shall not use exactly such amplifier configuration we leave this as an exercise to the reader.

But for the application in the cascode amplifier, which we are going to discuss in Sec. 3.4, it is important to know the transconductance i_o/v_i of the amplifier with the R_eC_e network. The corresponding circuit is drawn again in Fig. 3.2.10a and Fig. 3.2.10b shows the equivalent small signal circuit.

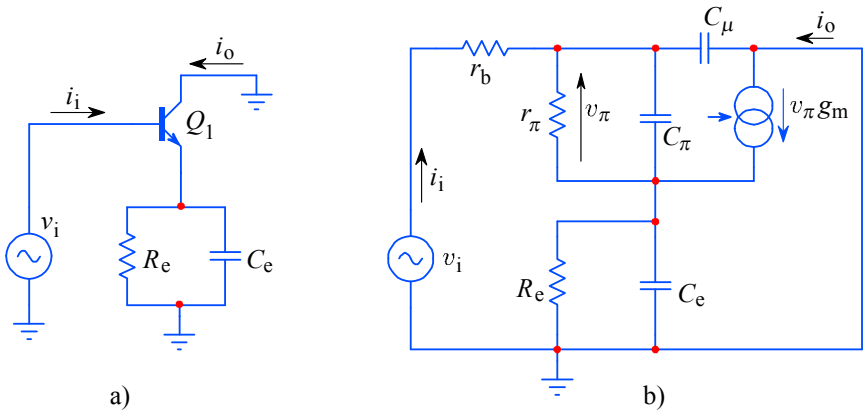

Fig. 3.2.10: Common collector amplifier: a) schematic; b) equivalent small signal circuit.

If we neglect the resistance r_b and the capacitance C_μ the following relation is valid for the remaining circuit:

$$v_i = i_i\,(z_\pi + Z_e) + i_o\,Z_e \tag{3.2.52}$$

where:

$$i_o = g_m\,v_\pi \qquad \text{and} \qquad v_\pi = i_i\,z_\pi$$

therefore:

$$i_o = g_m\,i_i\,z_\pi \tag{3.2.53}$$

The impedances z_π and Z_e are:

$$z_\pi = \frac{r_\pi}{1 + s\,C_\pi\,r_\pi} \qquad \text{and} \qquad Z_e = \frac{R_e}{1 + s\,C_e\,R_e} \tag{3.2.54}$$

We can rewrite Eq. 3.2.52 as:

$$v_i = i_i\,(z_\pi + Z_e + g_m\,z_\pi\,Z_e) \tag{3.2.55}$$

and the input current is:

$$i_i = \frac{v_i}{z_\pi + Z_e + g_m\,z_\pi\,Z_e} \tag{3.2.56}$$

The output current can be obtained by inserting Eq. 3.2.56 back into Eq. 3.2.53:

$$i_o = \frac{g_m\,z_\pi\,v_i}{z_\pi + Z_e + g_m\,z_\pi\,Z_e} \tag{3.2.57}$$

The transadmittance is:

$$\frac{i_o}{v_i} = \frac{g_m\,z_\pi}{z_\pi + Z_e + g_m\,z_\pi\,Z_e} \tag{3.2.58}$$

We can divide the numerator and denominator by $g_m\,z_\pi\,Z_e$:

$$\frac{i_o}{v_i} = \frac{1}{Z_e} \cdot \frac{1}{\dfrac{1}{g_m\,Z_e} + \dfrac{1}{g_m\,z_\pi} + 1} \tag{3.2.59}$$

Now we insert the expressions for z_π and Z_e from Eq. 3.2.54 and replace g_m by $1/r_e$:

$$\frac{i_o}{v_i} = \frac{1}{R_e} \cdot \frac{1 + s\,C_e R_e}{\dfrac{r_e}{R_e}(1 + s\,C_e R_e) + \dfrac{r_e}{r_\pi}(1 + s\,C_\pi r_\pi) + 1} \tag{3.2.60}$$

and with a slight rearrangement we obtain:

$$\frac{i_o}{v_i} = \frac{1}{R_e} \cdot \frac{1 + s\,C_e R_e}{\dfrac{r_e}{R_e} + \dfrac{r_e}{r_\pi} + 1 + s\,(C_e + C_\pi)\,r_e} \tag{3.2.61}$$

Because $(r_e/R_e) \ll 1$ and $(r_e/r_\pi) \ll 1$ we can neglect them, so:

$$\frac{i_o}{v_i} = \frac{1}{R_e} \cdot \frac{1 + s\,C_e R_e}{1 + s\,(C_e + C_\pi)\,r_e} \tag{3.2.62}$$

This equation can be simplified if we 'tune' the emitter network so that:

$$\begin{aligned} & C_e R_e = (C_e + C_\pi)\,r_e \\ \Rightarrow \quad & C_e(R_e - r_e) = C_\pi\,r_e \\ \Rightarrow \quad & C_e R_e \approx C_\pi\,r_e \end{aligned} \tag{3.2.63}$$

The transadmittance can thus be expressed simply as:

$$\boxed{\frac{i_\mathrm{o}}{v_\mathrm{i}} = \frac{1}{R_\mathrm{e}}} \tag{3.2.64}$$

Here we must not forget that at the beginning of our analysis we have neglected the resistance r_b, which, together with the transformed input capacitance C_e and the collector to base capacitance C_μ, makes a pole at:

$$s_1 = -1/(C_\mathrm{e} + C_\mu)\, r_\mathrm{b} \tag{3.2.65}$$

The magnitude of s_1 is equal to the upper half power frequency: $|s_1| = \omega_\mathrm{h}$. This pole makes the stage frequency dependent in spite of Eq. 3.2.64. We have also neglected the input resistance $\beta_0 R_\mathrm{e}$, but, since it is much larger than r_b, we shall not consider its influence (with it, the bandwidth would increase slightly). By introducing the pole s_1 back into Eq. 3.2.64, we obtain a more accurate expression for the transadmittance:

$$\boxed{\frac{i_\mathrm{o}}{v_\mathrm{i}} = \frac{1}{R_\mathrm{e}} \cdot \frac{-\dfrac{1}{(C_\mathrm{e} + C_\mu)\, r_\mathrm{b}}}{s - \left[-\dfrac{1}{(C_\mathrm{e} + C_\mu)\, r_\mathrm{b}}\right]}} \tag{3.2.66}$$

3.3 Common-Base Amplifier

In the previous sections we have realized that the collector to base capacitance C_μ has a very undesirable effect on the stage bandwidth (Miller effect). But in the common base configuration the base is effectively grounded and any current through C_μ is fed to the ground, not affecting the base current (actually, owing to the physical construction of the CB junction C_μ is spread across the whole base resistance r_b, so part of that current would nevertheless reach the base, which we shall analyze later).

The common base circuit is drawn in Fig. 3.3.1a and its small signal equivalent circuit in Fig. 3.3.1b. In wideband amplifiers the loading resistor R_L is much smaller than the collector to base resistance r_μ, so we shall neglect the later. In order to make the expressions still simpler, at the beginning of our analysis we shall also not take into account the base resistance r_b. However, we shall have to include r_b later, when we shall discuss the input impedance.

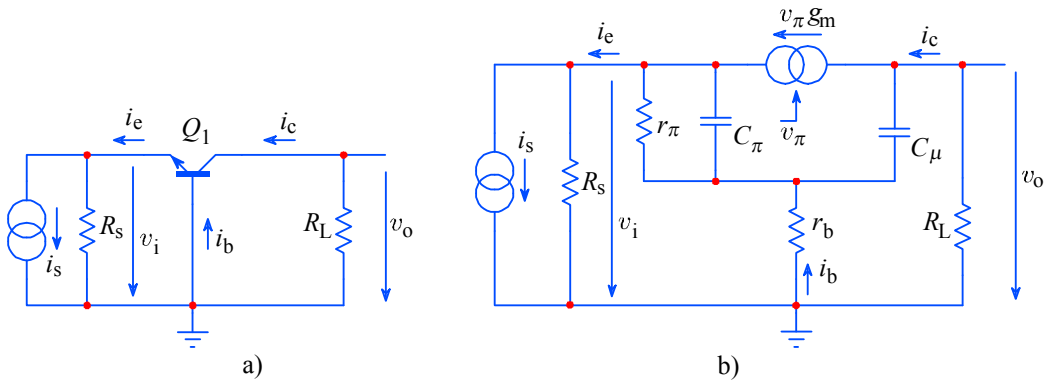

Fig. 3.3.1: Common base amplifier: a) schematic; b) equivalent small signal model.

The main characteristics of the common base stage are a very low input impedance, a very high output impedance, the current amplification factor $\alpha_0 \approx 1$, and, with the correct value of the loading resistor R_L, the possibility of achieving higher bandwidths. The last property is owed to a near elimination of the Miller effect, since C_μ is now grounded and does not affect the input A_v times. Thus C_μ is effectively in parallel with the loading resistor R_L and — because we can make the time constant $R_\mathrm{L} C_\mu$ relatively small — the bandwidth of the stage may be correspondingly large.

Another very useful property of the common base stage is that the collector to base breakdown voltage V_cbo is highest when the base is connected to ground and the higher reverse voltage reduces C_μ further (Eq. 3.1.2). Owing to all the listed properties the common base stage is used almost exclusively for wideband amplifier stages where large output signals are expected.

Following the current directions in Fig. 3.3.1, the input emitter current is:

$$i_\mathrm{e} = \frac{v_\pi}{z_\pi} + g_\mathrm{m}\, v_\pi \tag{3.3.1}$$

where:

$$z_\pi = \frac{r_\pi}{1 + s\, C_\pi\, r_\pi} \tag{3.3.2}$$

From these two equations it follows that:

$$i_e = v_\pi \left(g_m + \frac{1}{r_\pi} + s\,C_\pi \right) \tag{3.3.3}$$

The output collector current is:

$$i_c = g_m\, v_\pi \tag{3.3.4}$$

If we put Eq. 3.3.3 into Eq. 3.3.4 we obtain:

$$\frac{i_c}{i_e} = \frac{g_m}{g_m + \dfrac{1}{r_\pi} + s\,C_\pi} \approx \frac{g_m}{g_m + s\,C_\pi} = \frac{\alpha_0}{1 + s\,C_\pi\, r_e} \tag{3.3.5}$$

since $g_m \approx 1/r_e$ and $\alpha_0 = \beta_0/(\beta_0 + 1) \approx 1$. This equation has the pole at $-1/C_\pi\, r_e$, which lies extremely high in frequency, because r_e is normally very low. Since the output pole $-1/R_L C_\mu$, which we shall consider next, becomes prevalent we can neglect $s\,C_\pi r_e$ and assume that $i_c \approx i_e$. The output voltage is:

$$v_o = -\,i_c\, Z_L = -\,i_c\, \frac{R_L}{1 + s\,C_\mu\, R_L} \tag{3.3.6}$$

With the simplifications considered above we can write the expression for the transimpedance, which is:

$$\boxed{\frac{v_o}{i_e} \approx -\,\frac{R_L}{1 + s\,C_\mu\, R_L}} \tag{3.3.7}$$

Since the capacitance C_μ is in parallel with the loading resistor R_L, we can improve the performance by applying any of the inductive peaking circuits from Part 2. In practice we never consider only the 'pure' capacitance C_μ, because some stray capacitances are always present and must be taken into account. Also, if the transistor Q_1 is a part of an integrated circuit, we must consider the collector to substrate capacitance C_S. In such a case we use Eq. 3.1.2 with the exponent $m_c = 0.5$.

3.3.1 Input Impedance

We shall calculate the input impedance of the common base stage by taking into account the base resistance r_b, which — as we shall realize very soon — represents a very nasty obstacle in achieving a wide bandwidth. We shall make our derivation on the basis of Table 3.2.1, from which we have drawn Fig. 3.3.2. This figure represents the equivalent small signal input circuit owed to r_b.

The input admittance of the circuit in Fig. 3.3.2a is:

$$Y_e = \frac{1}{r_b} + \frac{1}{\dfrac{r_b}{\beta_0} + s\,\tau_T\, r_b} \tag{3.3.8}$$

Within the frequency range of interest the value r_b/β_0 in the second fraction is small and can be neglected. The simplified input admittance is thus:

$$Y_e \approx \frac{1}{r_b} + \frac{1}{s\,\tau_T\, r_b} \tag{3.3.9}$$

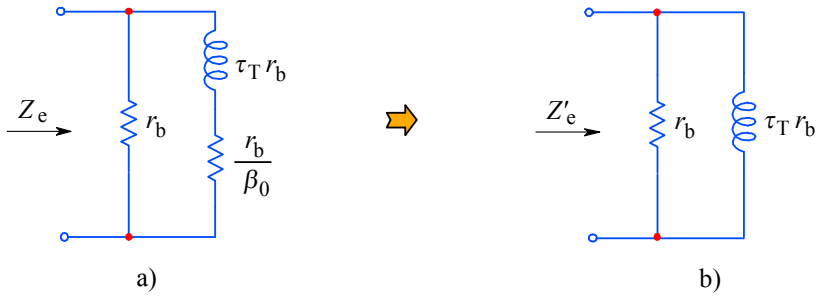

Fig. 3.3.2: Common base amplifier input impedance: a) r_b transformed to Z_e; b) within the frequency range of interest, r_b/β_0 can be neglected.

The real part represents a resistance:

$$\boxed{R_e \approx r_b} \tag{3.3.10}$$

and the imaginary part is an inductance:

$$\boxed{L_e \approx r_b \tau_T} \tag{3.3.11}$$

Normally, if the amplifier is built with discrete components, there is always some lead inductance L_s which must be added in series in order to obtain the total impedance.

In the next section, where we shall discuss the cascode amplifier, we shall find that the inductance L_e, together with the capacitance C_μ of the common emitter current driving stage, forms a parallel resonant circuit which may cause ringing in the amplification of steep signals. In most cases the resistance R_e is too large to damp the ringing effectively enough by itself, so additional circuitry will be required.

Eq. 3.3.10 and Eq. 3.3.11, respectively, disclose the fact that the annoying inductance L_e and the resistance R_e are directly proportional to the base spread resistance r_b. When using this type of amplifier for the output stages, where the amplitudes are large (e.g., in oscilloscopes), we must use more powerful transistors, mostly in TO5 case type. In this case the internal transistor connections are relatively long and its total active area is large, the corresponding r_b is large as well. In order to decrease R_e and L_e we must select transistors which have low r_b. To decrease base spread resistance as much as possible and also to decrease the *transition time* (the time needed by the current carriers to pass the base width), the firm RCA has developed (already in the late 1960s) the so called *overlay transistor*. A typical overlay transistor is the 2N3866. Such transistors are essentially integrated circuits, composed of many identical small transistors connected in parallel.

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3.4 Cascode Amplifier

If the common emitter amplifier of Fig. 3.2.1a is used as a driver of the common base amplifier of Fig. 3.3.1a, a *cascode amplifier* [Ref. 3.3, 3.7, 3.12] is obtained. The name *cascode* springs from the times when electronic tubes were the circuit building blocks. The anode of the first tube (the equivalent of the common emitter stage) was loaded by the **cathode** input of the second tube with a grounded grid (the equivalent of the common base stage). Both electronic tubes were therefore connected in **cascade**, hence the compound word **cascode**.

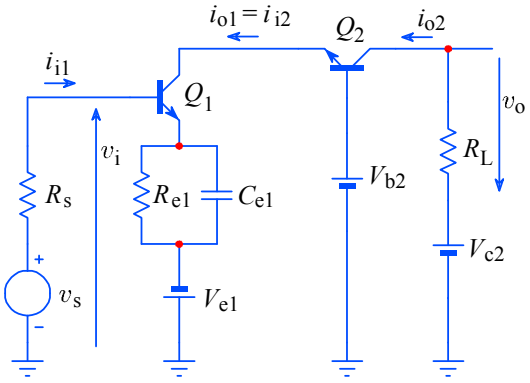

Fig. 3.4.1: Cascode amplifier schematic

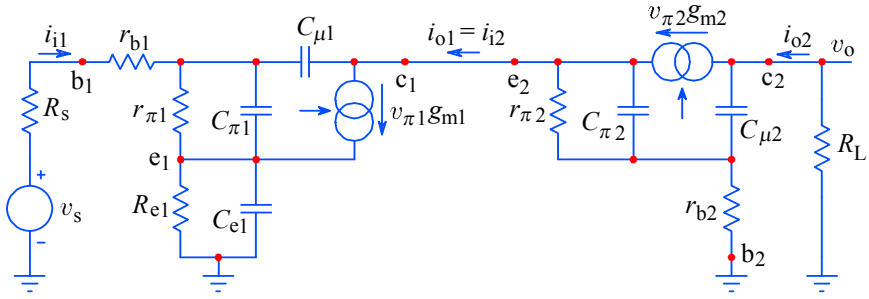

Fig. 3.4.2: Equivalent small signal model of a cascode amplifier. The components belonging to the common emitter circuit bear the index '1' and those of the common base circuit bear the index '2'.

3.4.1 Basic Analysis

A transistor cascode amplifier is drawn in Fig. 3.4.1 and Fig. 3.4.2 shows its small signal equivalent circuit. All the components that belong to transistor Q_1 bear the index '1' and all that belong to transistor Q_2 bear the index '2'.

For the emitter network of Q_1 we select the values such that $R_{e1}C_{e1} = \tau_{T1}$.

In order to simplify the initial analysis, we shall first neglect R_s, r_{b2}, and $C_{\mu 1}$. Later we shall reintroduce these elements one by one to get a closer approximation.

We have already derived the equations needed for each part of the combined circuit: for the common emitter stage we have Eq. 3.2.66 and for the common base we

have Eq. 3.3.7. We only need to multiply these two equations to get the voltage gain of our cascode amplifier:

$$A_\mathrm{v} = \frac{i_\mathrm{o1}}{v_\mathrm{i}} \cdot \frac{v_\mathrm{o}}{i_\mathrm{o1}} = \frac{v_\mathrm{o}}{v_\mathrm{i}} \approx \frac{1}{R_\mathrm{e1}} \cdot \frac{1}{1 + s\,C_\mathrm{e1}\,r_\mathrm{b1}} \cdot \left(- \frac{R_\mathrm{L}}{1 + s\,C_{\mu 2}\,R_\mathrm{L}} \right) \tag{3.4.1}$$

Here we have approximated $\alpha_{02} \approx 1$, and therefore $i_\mathrm{o2} = i_\mathrm{o1}$. The first fraction, multiplied by R_L from the third fraction, is the DC voltage amplification and the remainder represents the frequency dependence:

$$A_\mathrm{v} \approx - \frac{R_\mathrm{L}}{R_\mathrm{e1}} \cdot \frac{1}{(1 + s\,C_\mathrm{e1}\,r_\mathrm{b1})\,(1 + s\,C_{\mu 2}\,R_\mathrm{L})} \tag{3.4.2}$$

Obviously, the frequency dependence is a second-order function. There are two poles: the pole at the input is $-1/\,C_\mathrm{e1} r_\mathrm{b1} = -1/\tau_\mathrm{T1}$ whilst the pole $-1/C_{\mu 2}\,R_\mathrm{L} = -1/\tau_\mathrm{T2}$ is on the output side. As we shall see later, it is possible to apply the peaking technique on both sides.

In an ideal case the common base stage input (emitter) impedance is very low. Because of this low load the first stage voltage gain $A_\mathrm{v1} \ll 1$, so $C_{\mu 1}$ would not be amplified by it. And if we could neglect r_b2 the capacitance $C_{\mu 2}$ would appear in parallel to the loading resistor R_L, and therefore it would neither be multiplied by the second stage's voltage gain A_v2. Both $C_{\mu 1}$ and $C_{\mu 2}$ are relatively small, so it is obvious that the cascode amplifier has, potentially, a much greater bandwidth in comparison with a simple common emitter amplifier (for the same total voltage gain). The price we pay for this improvement is the additional transistor Q_2.

Of course, in practice things are not so simple, and in addition we should not neglect the inevitable stray capacitances. Those should be added to $C_{\mu 1}$ and $C_{\mu 2}$. Also, $(R_\mathrm{s} + r_\mathrm{b1})$ with $C_{\mu 1}$ will affect the behavior of Q_1 and r_b2 with $C_{\mu 2}$ will affect the behavior of Q_2, as we shall see in the following analysis.

3.4.2 Damping of the Q_2 Emitter

Owing to the base spread resistance r_b2 the Q_2 input (emitter) has an inductive component with the inductance $L_\mathrm{e2} = \tau_\mathrm{T2}\,r_\mathrm{b2}$ in parallel with r_b2, as already shown in Table 3.2.1 and also in Fig. 3.3.2. The equivalent input impedance of the transistor Q_2 was derived in Eq. 3.3.9 to Eq. 3.3.11.

As shown in the simplified circuit in Fig. 3.4.3, the inductance L_e2 and the collector to base capacitance $C_{\mu 1}$ of Q_1 form a series resonant circuit, damped by r_b2 in parallel with L_e2 (and a series emitter resistance r_b2/β_2, which is very small, so it was neglected). The other end of $C_{\mu 1}$ is connected to the base of Q_1, where we must consider the following two effects:

- at very high frequencies the input signal goes directly through r_b1 and $C_{\mu 1}$;
- at lower frequencies, the signal is inverted and amplified by Q_1 and the internal base junction can then be treated as the virtual ground.

In an actual cascode amplifier Q_2 operates at a much higher collector voltage than Q_1, and since the collector currents are nearly equal this means a higher power dissipation for Q_2. By using for Q_2 a transistor capable of higher power dissipation, we shall probably have to accept its higher r_{b2} as well. This increases the inductance L_{e2} and lowers the damping of the series resonance formed by $C_{\mu 1}$ and L_{e2}, resulting in a large peaking near the upper cut off frequency.

To prevent this from happening, an additional impedance Z_d, consisting of a resistor R_d in parallel with a capacitor C_d, is connected between the collector of Q_1 and the emitter of Q_2. If R_d is made equal to r_{b2}, then C_d can be chosen so, that it cancels L_{e2}; the result is a resistive input impedance of the Q_2 emitter: $Z_{e2} \approx r_{b2}$.

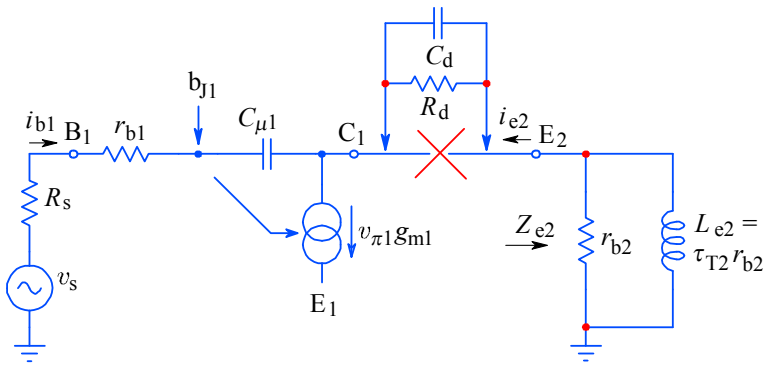

Fig. 3.4.3: Parasitic resonance damping of the cascode amplifier. Two current paths must be considered: at highest frequencies, for i_{b1}, $C_{\mu 1}$ represents a non-inverting cross-talk path; at lower frequencies, for i_{c1}, $C_{\mu 1}$ provides a negative feedback loop, thus it can be viewed as if being connected to a virtual ground (Q_1 base junction b_{J1}). The parasitic resonance, formed by $C_{\mu 1}$ and L_{e2} is only partially damped by r_{b2}; the required additional damping is provided by inserting R_d and C_d between Q_1 collector and Q_2 emitter.

So let us put:

$$R_d = r_{b2} = \sqrt{\frac{L_{e2}}{C_d}} \tag{3.4.3}$$

The value of C_d is then:

$$C_d = \frac{\tau_{T2}}{r_{b2}} = \frac{1}{2\pi f_{T2}\, r_{b2}} \tag{3.4.4}$$

To get a feeling for actual values let us have two equal transistors with parameters such as in the examples in Sec. 3.2.4 ($f_T = 600\,\text{MHz}$, $r_{b2} = 47\,\Omega$):

$$R_d = r_{b2} = 47\,\Omega \qquad C_d = \frac{1}{2\pi \cdot 600 \cdot 10^6 \cdot 47} = 5.6\,\text{pF} \tag{3.4.5}$$

The input impedance of the emitter circuit of transistor Q_2 now becomes:

$$Z_{e2} \approx r_{b2} \tag{3.4.6}$$

which is resistive at all frequencies (approximately so, because we have allowed ourselves a simplification). The corresponding equivalent circuit is shown in Fig. 3.4.4. The task of the impedance Z_d is actually twofold: it must damp the inductive input circuit of transistor Q_2, and as we shall see later, it can be a good choice for providing the thermal stabilization of the cascode stage.

Since we have introduced Z_d into the collector circuit of Q_1 we must now account for the Q_1 Miller capacitance:

$$C_\mathrm{M1} \approx C_{\mu 1}\left(1+\frac{Z_\mathrm{e2}}{Z_\mathrm{e1}}\right) = C_{\mu 1}\left(1+\frac{r_\mathrm{b2}}{R_\mathrm{e1}}\right) \tag{3.4.7}$$

where Z_e2 is the Q_2 compensated emitter input impedance and Z_e1 is the impedance of the emitter circuit of Q_1. With this consideration the gain, Eq. 3.4.2, becomes:

$$A_\mathrm{v} \approx -\frac{R_\mathrm{L}}{R_\mathrm{e1}} \cdot \frac{1}{\left[1+s\left(C_\mathrm{e1}+C_\mathrm{M1}\right)r_\mathrm{b1}\right]\left(1+s\,C_{\mu 2}\,R_\mathrm{L}\right)} \tag{3.4.8}$$

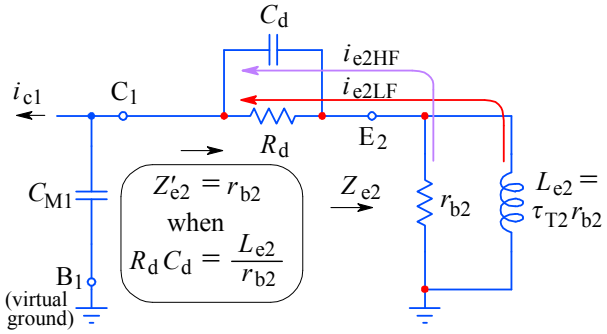

Fig. 3.4.4: With damping the simplified Q_2 input impedance becomes (approximately) resistive. Note the high and low frequency paths.

The collector to base capacitance of the transistor Q_1 allows very high frequency signals from the input bypassing this transistor and directly flowing into the emitter of transistor Q_2. Transistor Q_1 amplifies, inverts, and delays the low frequency signals. In contrast, all of what comes through $C_{\mu 1}$ is *non-delayed*, *non-amplified*, and *non-inverted*, causing a pre-shoot [Ref. 3.1] in the step response, as shown in Fig. 3.4.5. The Q_1 collector current, i_c1, is the sum of $i_{\mu 1}$ and $v_{\pi 1} g_\mathrm{m1}$. Note that both the pre-shoot owed to $i_{\mu 1}$ and the overshoot of $v_{\pi 1} g_\mathrm{m1}$ are reduced in v_c2 by the Q_2 pole $(1/C_{\mu 2} R_\mathrm{L})$.

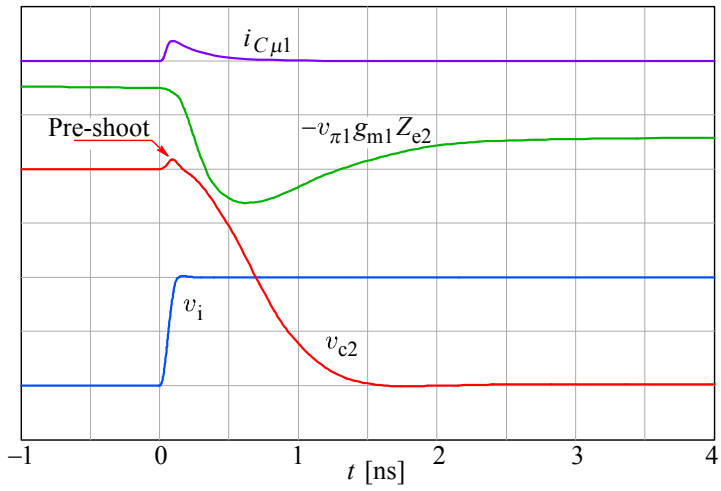

Fig. 3.4.5: The step response v_c2 has a pre-shoot owed to the signal cross-talk through $C_{\mu 1}$ (arbitrary vertical units, but corresponding to $A_\mathrm{v} = -2$).

So far we have excluded $C_{\mu 2}$ from our analysis. When included, its effect on bandwidth is severe, owing to the non-zero r_{b2} and the Miller effect. But it also affects the emitter input impedance of Q_2 since $C_{M2} = C_{\mu 2}(1 + A_v)$ appears in parallel to r_{b2} and is consequently transformed into the emitter in accordance with Table 3.2.1, in the same way as in Fig. 3.2.7. If A_v is relatively high the pronounced resonance owed to $C_{\mu 2}$ can cause long ringing, even if the bandwidth is lower than the resonant frequency.

The damping by $C_d R_d$ works only up to a certain frequency, because they add their own parasitic L and C, which we were trying to avoid in the firts place, and which also reduce the bandwidth. Instead, *John Addis* [Ref. 3.26] suggests an alternative approach by modifying the base impedance: the Q_2 base is connected to the bias voltage through a resistor R_A of up to a 100 Ω and grounded by a small capacitor $C_A \approx C_{\mu 2}$. In Fig. 3.4.6 we compare the voltage gain, the phase, and the group delay for the two cases: $R_A = 0$ and $R_A = 33\,\Omega$, respectively (the value of 33 Ω was optimized to the transistor model used in the simulation). The change in the Q_2 emitter impedance (b curves) is exposed by the lower drive stage current i_{c1} near the cut off frequency.

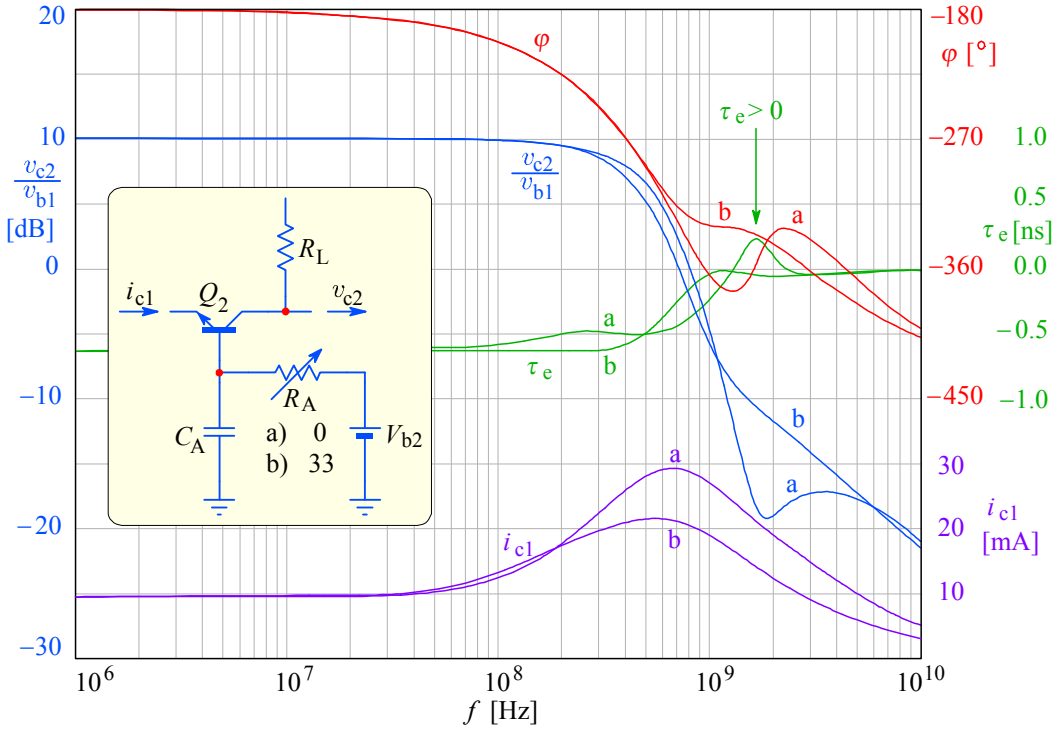

Fig. 3.4.6: The compensation method of Q_2 as suggested by John Addis. a) With $R_A = 0$, the frequency response has a notch at the resonance and a phase-reversed cross-talk, which makes the group delay τ_e positive, causing a potential instability. b) with $R_A = 33\,\Omega$ and $C_A = 3\,\text{pF}$ (the values suit the particular transistor model used for simulation) the frequency response slope is corrected to the $-6\,\text{dB}/2f$, the phase is smoothed and, although the bandwidth is reduced slightly, the group delay linearity is extended and the undesirable positive region is reduced to negative. The Q_2 emitter impedance is increased near cut off, as can be deduced from the lower i_{c1} peak.

To analyze this type of compensation of the Q_2 emitter impedance we must consider the equivalent circuit in Fig. 3.4.7. Here the capacitance $C_{\mu 2}$ is seen by the base as the Miller capacitance C_{M2} (remembering that $A_v = R_L/R_{e1}$):

$$C_{M2} = C_{\mu 2}(1 + A_v) \tag{3.4.9}$$

which appears in parallel with the base spread resistance r_{b2}.

The external compensation network, the parallel connection of R_A and C_A, is added in series and the total can then be transformed by the same rule as in Fig. 3.2.7. The base impedance is:

$$Z_{b2} = \frac{1}{\frac{1}{r_{b2}} + sC_{M2}} + \frac{1}{\frac{1}{R_A} + sC_A} \tag{3.4.10}$$

If $R_A \approx r_{b2}$ and $C_A \approx C_{\mu 2}$ then Z_{b2} becomes:

$$Z_{b2} = \frac{2R_A}{1 + sC_A R_A} = \frac{R_s}{1 + sC_s R_s} \tag{3.4.11}$$

which appears at the Q_2 emitter as a parallel connection of $R_s = 2R_A$ and $C_s = C_A/2$.

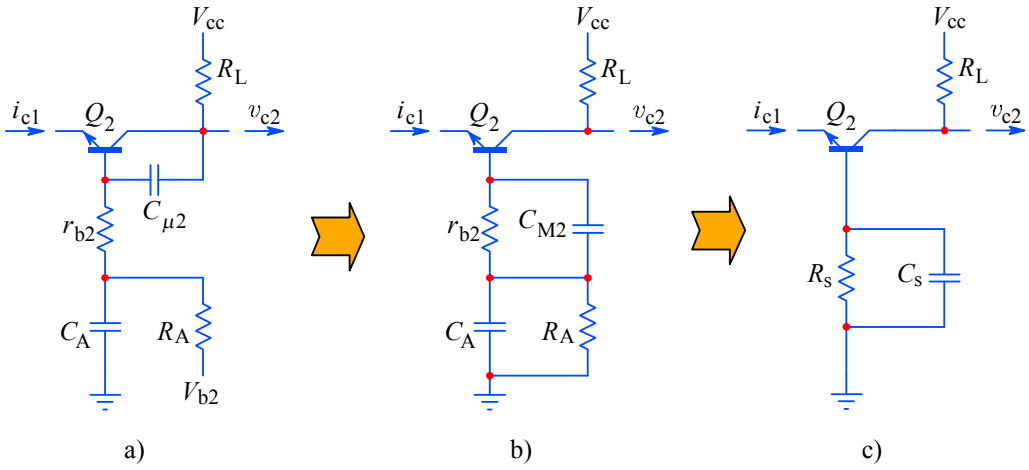

Fig. 3.4.7: The Q_2 emitter input impedance compensation by the added base network R_A and C_A (see also Fig. 3.2.7), making it capacitive at high frequencies. By altering the valuse slightly it can also be used to compensate the stray base inductance.

3.4.3 Thermal Compensation

Amplifier's thermal stability is preferably solved by using a differential configuration. However, in order to illustrate the potential problems, we discuss a single transistor stage. The well known relation for the transistor's base–emitter voltage is:

$$V_{be} = \frac{k_B T_j}{q_e} \ln\left(\frac{I_e}{I_s} + 1\right) \tag{3.4.12}$$

where T_j is the absolute temperature of the p-n junction, which causes the increase of V_{be} in a linear proportion. Unfortunately, the situation is complicated by the 'saturation current' $I_s \approx 10^{-14}$ A (for a typical silicon transistor at room temperature), which approximately doubles for every 8 K increase in temperature. The combined influence results in a V_{be} temperature coefficient of ≈ -2 mV/K (see Appendix 3.1 on the disk). All other terms are constants (as *James M. Bryant* of Analog Devices likes to joke, we can not change the Boltzmann constant k_B because *Ludwig Boltzmann* is already dead, and neither can we change the electron charge q_e because both *Charles Augustine de Coulomb* and *Joseph John Thompson* are dead, too!).

When we apply the bias and the supply voltage to a transistor, the power dissipated by the transistor depends on the collector current I_c and the voltage V_{ce} across the transistor:

$$P_D = I_c V_{ce} \tag{3.4.13}$$

If we know the ambient temperature T_a and the thermal resistance from junction to ambient $R_{\theta ja}$ [K/W] (*kelvin* per *watt*), we can calculate the junction temperature T_j:

$$T_j = T_a + R_{\theta ja} P_D \tag{3.4.14}$$

In a properly designed amplifier, a certain time after power-up an equilibrium is reached: all the heat generated by the transistor dissipates into the ambient and the transistor obtains a stable, but higher temperature.

If we now apply a voltage step to the base the collector current I_e increases, changing the power dissipation (depending on the chosen DC bias it can either increase or decrease). A little later, depending on the thermal capacitance of the transistor's case $C_{\theta c}$ and the thermal resistance $R_{\theta ja}$, a new temperature equilibrium is reached. As shown in Fig. 3.4.8, the change occurs gradually, depending on the transistor thermal time constant. But the supply voltage is shared between the transistor and the loading resistance, whilst the same current flows through both of them, therefore the choice of the DC bias point governs whether the transistor power dissipation will increase or decrease with the signal. This is known as the 'thermal distortion'.

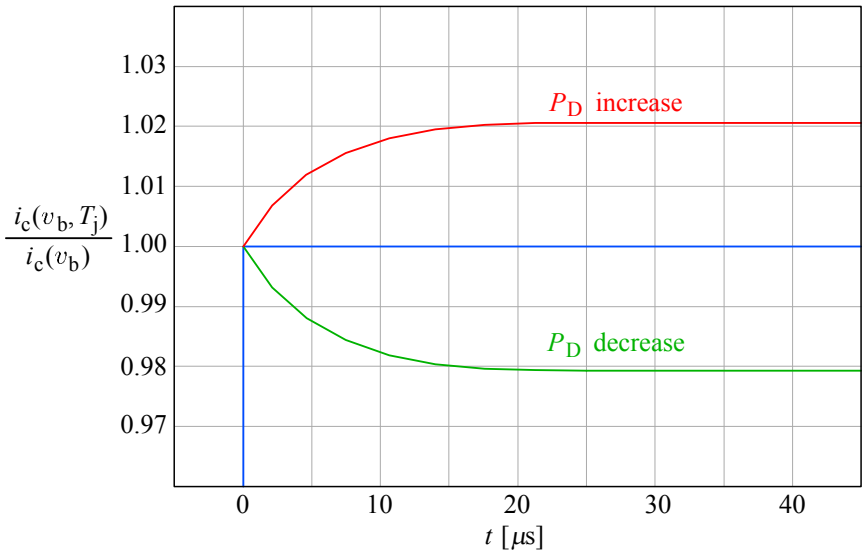

Fig. 3.4.8: The collector current step response is distorted by a long term thermal drift following the transient. Depending on the chosen DC bias point, the output can either increase or decrease relative to the ideal response. In addition to the junction thermal time constant, there can also be a slower one, owed to the transistor case temperature change.

Although the dynamic emitter resistance r_e is also temperature dependent (see Eq. 3.1.1), which affects the gain (see Eq. 3.2.61), in all wideband circuits we put (for bandwidth reasons!) a much larger external degeneration resistance R_e in series, reducing the gain temperature dependence. So in practice all thermal changes occur because of V_{be} and I_s.

In a multi-stage amplifier different transistors will have different operating points, thus different temperatures and temperature dependence. Also, they have different time constants, which cause longer and shorter drifts, and we can not expect all effects to cancel. Consequently even long oscillations in the step response can occur.

Before we look for the remedy for the problem of how to cancel, or at least how to substantially reduce the thermal distortion, let us take a look at Fig. 3.4.9, which shows a simple common emitter stage, and the way in which the power dissipation is shared between the load and the transistor as a function of the collector current. As usual, we use capital letters for the applied DC voltages, loading resistor, etc., and small letters for the instantaneous signal voltages and currents. The transistor's power dissipation is:

$$P_D = v_{ce}\, i_c = v_{ce}\,\frac{v_L}{R_L} = v_{ce}\,\frac{V_{cc} - v_{ce}}{R_L} = v_{ce}\,\frac{V_{cc}}{R_L} - \frac{v_{ce}^2}{R_L} \qquad (3.4.15)$$

Since v_{ce} cannot exceed V_{cc} if the collector load is purely resistive, the right-hand vertical axis is normalized to V_{cc}. The left-hand vertical axis is normalized to the maximum load power, which is simply $P_{Lmax} = V_{cc}^2/R_L$ (corresponding to $v_{ce} = 0$ and thus $P_D = 0$). The transistor's power dissipation, however, follows an inverse parabolic function with a maximum at $v_{ce} = V_{cc}/2$:

$$P_{Dmax} = \left(\frac{V_{cc}}{2}\right)^2 \frac{1}{R_L} = \frac{V_{cc}^2}{4\,R_L} \qquad (3.4.16)$$

This middle point is the optimum DC bias point for a transistor stage. If excited by small signals, the transistor power dissipation follows the parabola close to its broad and relatively flat top and thus it does not change very much. This means that the transistor's temperature does not change very much either.

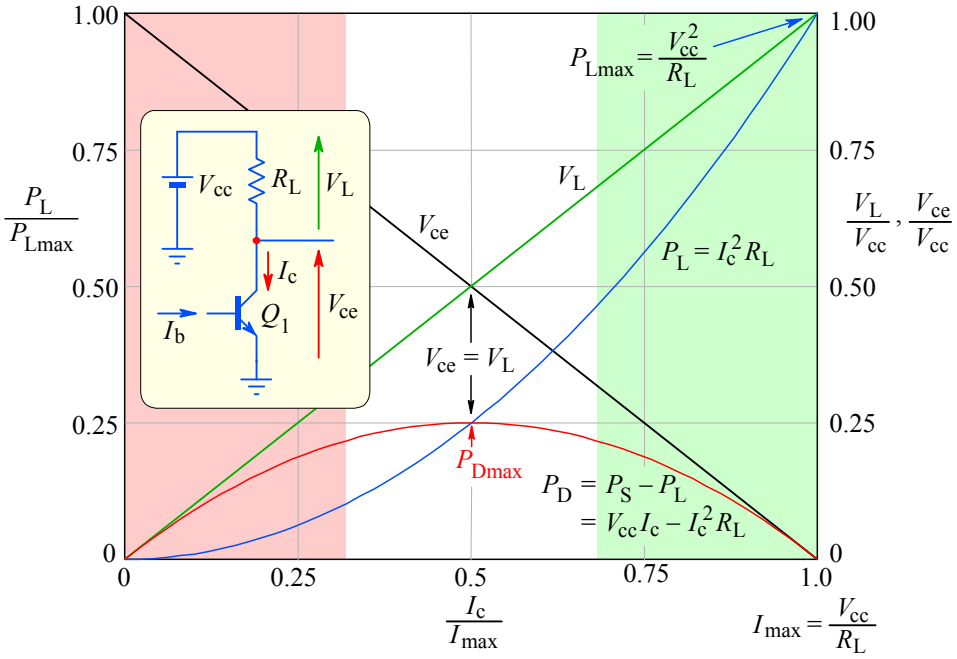

Fig. 3.4.9: The optimum bias point is when the voltage across the load is equal to the voltage across the transistor. This is optimal both in the sense of thermal stability, as well as in the available signal range sense.

If other design requirements force us to move the bias point far from the top of the parabola, the bias with $V_{ce} < V_{cc}/2$ (or $I_c > I_{max}/2$) is preferred, in contrast to the range $V_{ce} > V_{cc}/2$, because the latter situation is unstable. However, in wideband amplifiers we can hardly avoid it, because we want to have a low R_L, a high I_c and a high V_{cb} (to reduce C_μ) and all three conditions are required for high bandwidth.

The typical temperature coefficient of a base–emitter p–n junction voltage ($\approx 0.6\,V$) is approximately $-2\,mV/K$ for silicon transistors, so we can explain the instability in the following way:

When the circuit is powered up the transistor conducts a certain collector current, which heats the transistor, increasing the transistor base–emitter p–n junction temperature. If the base is biased from a voltage source (low impedance, which in wideband amplifiers is usually the case), the temperature increase will, owing to the negative temperature coefficient, decrease the base–emitter voltage. In turn, the base current increases and, consequently, both the emitter and the collector current increase, which further increases the dissipation and the junction temperature. The load voltage drop would also increase with current and therefore reduce the collector voltage, thus lowering the transistor power dissipation. But with a low R_L, the change in the drop of load voltage will be small, so the transistor power dissipation increase will be reduced only slightly.

The effect described is cumulative; it may even lead to a thermal runaway and the consequent destruction of the transistor if the top of the parabola exceeds the maximum permissible power dissipation of the transistor (which is often the case, since we want low R_L and high V_{cc} and I_e, as stated above). In a similar way, on the basis of the -2 mV/K temperature dependence of V_{be}, the reader can understand why the bias point for $V_{ce} < V_{cc}/2$ is thermally stable.

According to Eq. 3.4.16, to have the transistor thermally stable means having resistance R_L (or $R_L + R_e$) such that at the bias point the voltage drop across them is equal to $V_{cc}/2$. In general, this principle is successfully applied in differential amplifiers: when one transistor is excited so that its bias point is pushed to one side of the parabola the bias point of the other transistor is moved exactly to the same dissipation on the opposite side of the parabola. As a result the temperature becomes lower but equal in both transistors. Thus in the differential amplifier both transistors can always have similar temperatures, even if the temperature changes by the signal (provided that we remain within the linear range of excitation). Also, the thermal drift can be minimized by using current source biasing in the emitters of a differential amplifier, as well as using emitter degeneration resistors, which minimize variations in ΔV_{be}, even if transistor parameters vary considerably.

In our cascode circuit of Fig. 3.4.1 the transistor Q_1 already has an emitter resistor R_{e1} as dictated by the required current gain, and we do not want to change it. However, we can add a resistor, which we label R_θ, in the collector circuit of Q_1 to make $V_{ce1} \approx I_{c1}\,(R_{e1} + R_\theta) \approx V_{e2}/2$, where V_{e2} is the voltage at the emitter of the transistor Q_2. Suppose now that the emitter current is $I_{e1} \approx I_{c1} = 50\,mA$ and the Q_2 base voltage $V_{b2} = +15\,V$. Then the emitter voltage of transistor Q_2 is:

$$V_{e2} = V_{b2} - V_{be2} \approx 15 - 0.6 = 14.4\,V \qquad (3.4.17)$$

where V_{be2} is the base–emitter voltage (about $0.6\,V$ for a silicon transistor).

With $R_{e1} = 20\,\Omega$ the value of the thermal compensation resistor is:

$$R_\theta = \frac{V_{e2}/2 - I_{c1}\,R_{e1}}{I_{c1}} = \frac{14.4/2 - 0.05 \cdot 20}{0.05} = 124\,\Omega \qquad (3.4.18)$$

Such a resistor should be used instead of R_d as calculated before to achieve both the ringing suppression and the thermal compensation. But by inserting these $124\,\Omega$ instead of $R_d = 47\,\Omega$, the Miller capacitance C_M would increase to $27.8\,\text{pF}$, decreasing the amplifier bandwidth too much. Fortunately the compensating resistor R_θ needs to correct the behavior of the amplifier only at very low frequencies. So we can bridge that part of it which is not needed for the suppression of ringing by an appropriate capacitor; let us call it C_θ, as shown in Fig. 3.4.10. By doing so, we prevent an excessive increase of Miller capacitance.

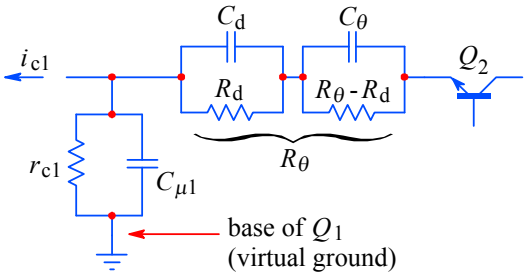

Fig. 3.4.10: The modified compensation network: R_dC_d provide the HF damping, whilst $R_\theta C_\theta$ provide thermal compensation.

The question is how to calculate the proper value of C_θ? The obvious way would be to calculate the thermal capacity of the transistor's die and case mass (and an eventual heat sink) and all the thermal resistances (junction to case, case to heath sink, heath sink to air), as is usually done for high power output stages.

Bruce Hofer [Ref.3.8] suggests the following — more elegant — procedure, based on Fig. 3.4.10. The two larger time constants in this figure must be equal:

$$(R_\theta - R_d)\,C_\theta = r_{c1}\,C_{M1} \qquad (3.4.19)$$

Here r_{c1} is the dynamic collector resistance of transistor Q_1, derived from Fig. 3.4.11 as $\Delta V_{ce}/\Delta I_c$. In this figure V_A is the *Early voltage*:

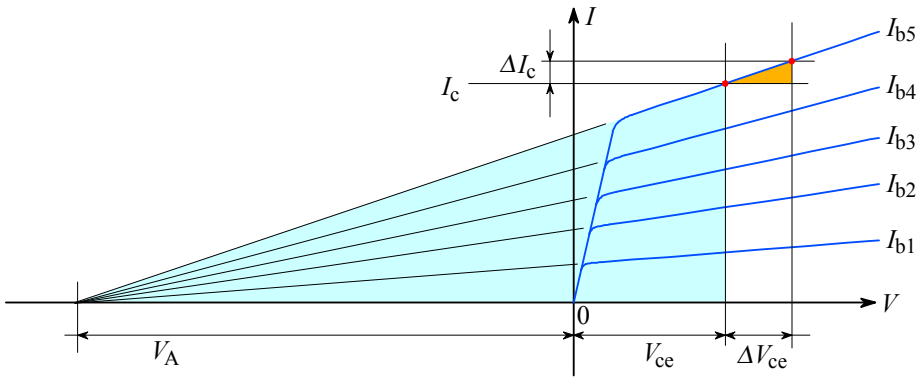

Fig. 3.4.11: The dynamic collector resistance r_{c1} is derived from the $I_c(V_{ce}, I_b)$ characteristic and the Early voltage V_A.

The meaning of the Early voltage can be derived from Fig. 3.4.11, where several curves of the collector current I_c vs. collector to emitter voltage V_{ce} are drawn, with base current I_b as the parameter. With increasing collector voltage the collector current increases even if the base current is kept constant. This is because the collector to base depleted area widens on the account of the (active) base width as the collector voltage increases. This in turn causes the diffusion gradient of the current carriers in the base to increase, hence the increased collector current.

By extending the lines of the collector current characteristics back, as shown in Fig. 3.4.11, all the lines intersect the abscissa at the same virtual voltage point V_A (negative for NPN transistors), called the *Early voltage* (after *J.M. Early*, [Ref. 3.11]). From the similarity of triangles we can derive the collector's dynamic resistance:

$$r_{c1} = \frac{\Delta V_{ce}}{\Delta I_c} = \frac{V_c - (-V_A)}{I_c} \tag{3.4.20}$$

Since the voltage gain of the common emitter stage is low, C_{M1} will be only slightly larger than $C_{\mu 1}$. If we now suppose that transistor Q_1 has an $r_{c1} = 0.5 \cdot 10^6\,\Omega$ and $C_{\mu 1} = 3\,\text{pF}$, the value of C_θ should be:

$$C_\theta = \frac{r_{c1}\, C_{M1}}{R_\theta - R_d} = \frac{0.5 \cdot 10^6 \cdot 3 \cdot 10^{-12}}{124 - 47} = 19.5\,\text{nF} \tag{3.4.21}$$

In practice, we can take the closest standard values, e.g., $C_\theta = 22\,\text{nF}$ and $R_\theta - R_d = 124 - 47 = 77\,\Omega \approx 75\,\Omega$. Since, in general, a wideband amplifier has several amplifying stages, each one having its own temperature and damping problems, these values can be varied substantially in order to achieve the desired performance. Thermal problems tend to be more pronounced towards the output stages where the signal amplitudes are high. Here experimentation should have the last word. Nevertheless, the values obtained in this way represent a good starting point.

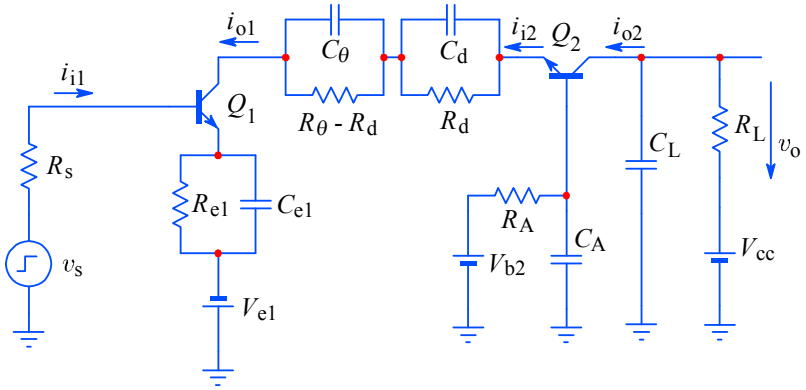

Fig. 3.4.12: The compensated cascode amplifier. If $R_A C_A$ compensation is used, $R_d C_d$ may become unnecessary. The main bandwidth limiting time-constants are now $(R_s + r_{b1})C_{e1}$ and $(C_{\mu 2} + C_L)R_L$.

In order to achieve a good thermal compensation, the same half-voltage principle (Fig. 3.4.9) can be applied to both Q_1 and Q_2, although this will rarely be possible. On the other hand, a cascode amplifier can always be implemented as a differential amplifier, simplifying the problem of thermal compensation and, as a bonus, doubling the gain. We shall see this later in Sec.3.7. There are, as we are going to see in following sections, still some points for possible improvement of the cascode amplifier.

All the discussion on thermal compensation in this section was based on the simple single stage cascode amplifier shown in Fig. 3.4.12.

It is however important to note that a multistage DC coupled amplifier must necessarily be built in a differential configuration. Then many of the effects described would be either compensated automatically or at least reduced significantly. Not all, unfortunately. Often the biggest problems will be caused by the first stage, since its output will be amplified by all the remaining gain of the chain. But the stages following it might also have their share, because of the increased signal amplitude. And the output stage is usually the one to drive the load, thus it is required to handle most of the power. It is therefore necessary to pay attention to thermals at each stage.

In addition, in an integrated circuit it is also necessary to check the adjacent circuits, such as current mirrors, constant current bias circuits and voltage references; they will all be affected by every thermal gradient across the chip. They will also tend to have their own particular thermal time constant, and changes in those can in turn affect the main signal chain. Consequently a complex system can be difficult to control and compensate properly.

Finally, in amplifiers employing DC feedback the thermal problems are usually reduced to only those of the first stage, but still the output stage could be prone to thermal runaway under heavy load.

Some of these problems will be mentioned again in discussions of differential circuit configurations in further sections and chapters.

3.5 Emitter Peaking in a Cascode Amplifier

Here we shall examine the possibility of improving the cascode amplifier bandwidth by applying the emitter peaking technique.

Let us return to the basic cascode amplifier of Fig. 3.4.1 and Fig. 3.4.2, but with a little modification: we shall assume a current signal source in parallel with the source resistance R_s. We shall also assume that there is an output capacitance in parallel with the load resistance R_L such that its value is $C_o = C_{\mu 2} + C_L$. To simplify the analysis we shall disregard the damping and thermal compensation described in the previous section. We shall basically follow the steps of Carl Battjes [Ref. 3.1], to show a different approach to the cascode amplifier design.

3.5.1 Basic Analysis

The transimpedance of the amplifier in Fig. 3.5.1 is:

$$\frac{v_o}{i_s} = \frac{i_{b1}}{i_s} \cdot \frac{i_{c1}}{i_{b1}} \cdot \frac{i_{c2}}{i_{c1}} \cdot \frac{v_o}{i_{c2}} \tag{3.5.1}$$

where:

$$\frac{i_{b1}}{i_s} = \frac{R_s}{R_s + Z_i} \qquad \text{and} \qquad \frac{i_{c1}}{i_{b1}} = \beta(s) = \frac{1}{\dfrac{1}{\beta_0} + s\,\tau_{T1}} \tag{3.5.2}$$

with Z_i being the input impedance looking into the base of transistor Q_1 and R_s the source resistance. At higher frequencies, when the input capacitance of transistor Q_1 prevails (see Eq. 3.2.12 and [Ref.3.1]), we have:

$$\frac{i_{c1}}{i_{b1}} \approx \frac{1}{s\,\tau_{T1}} \qquad \text{and} \qquad \tau_{T1} = \frac{1}{2\pi f_{T1}} \tag{3.5.3}$$

Further, for Q_2 we have:

$$\frac{i_{c2}}{i_{c1}} = \alpha_2 \approx 1 \qquad \text{and} \qquad \frac{v_o}{i_{c2}} = \frac{R_L}{1 + s\,R_L\,C_o} = \frac{R_L}{1 + s\,\tau_L} \tag{3.5.4}$$

where $\tau_L = R_L\,C_o$ and $C_o = C_{\mu 2} + C_L$.

We shall temporarily neglect the base spread resistance r_{b1} and calculate the input impedance Z_i at the base–emitter junction of Q_1 by Eq. 3.2.15:

$$Z_i = \big[\beta(s) + 1\big]\, Z_{e1} = \left(\frac{1}{s\,\tau_{T1}} + 1\right) Z_{e1} = \frac{1 + s\,\tau_{T1}}{s\,\tau_{T1}}\, Z_{e1} \tag{3.5.5}$$

The emitter peaking technique basically involves the introduction of a zero at $s_z = -\omega_R = -1/\tau_R$ in the emitter network of Q_1 to cancel the pole of the Q_2 collector load at $s_p = -\omega_L = -1/\tau_L$. For an efficient peaking τ_R must be lower than τ_L, but still above the time constant τ_{T1} of Q_1:

$$\tau_{T1} < \tau_R < \tau_L \tag{3.5.6}$$

The complete emitter circuit should look as in Fig. 3.5.1a, in which $\tau_R = RC$ and its HF impedance is:

$$Z_{e1} = \frac{R_{e1}\,(1 + s\,\tau_R)}{(1 + s\,\tau_{T1})\,(1 + s\,\tau_L)} = \frac{R_{e1}(1 + s\,\tau_R)}{s^2\,\tau_{T1}\tau_L + s\,(\tau_{T1} + \tau_L) + 1} \tag{3.5.7}$$

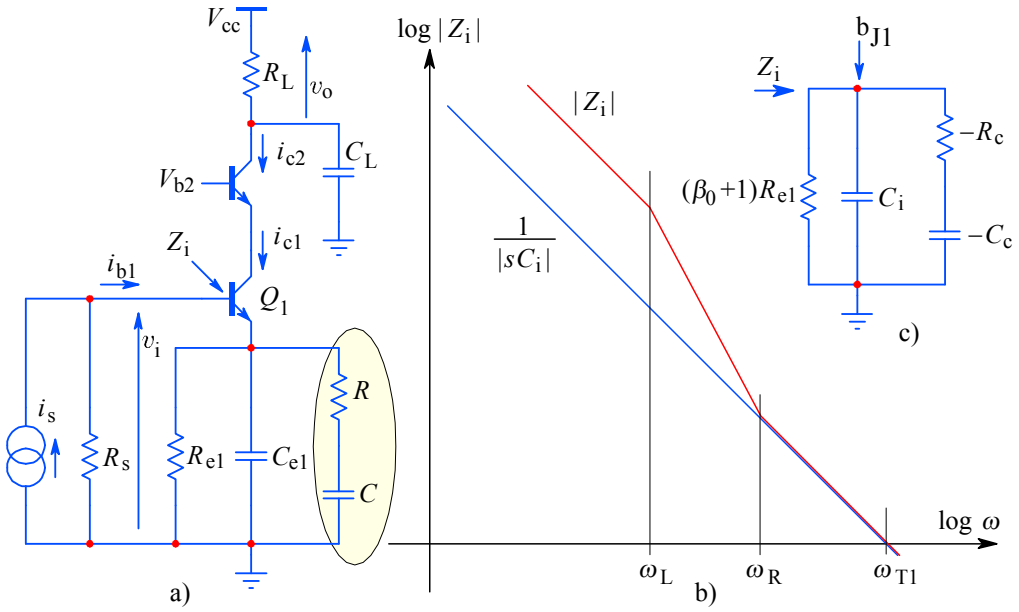

Fig. 3.5.1: Emitter peaking in cascode amplifiers. a) By adding a zero at $\omega_R = 1/RC$ to the emitter network of Q_1, we modify the input impedance Z_i at the base junction of Q_1; b) the frequency dependent asymptote plot of Z_i; c) the equivalent schematic has negative components, too. See the explanation in Sec. 3.5.2.

By introducing Eq. 3.5.7 back into Eq. 3.5.5 the input impedance can be expressed as:

$$Z_i = \frac{1 + s\,\tau_{T1}}{s\,\tau_{T1}} \cdot \frac{R_{e1}\,(1 + s\,\tau_R)}{(1 + s\,\tau_{T1})\,(1 + s\,\tau_L)} = \frac{R_{e1}\,(1 + s\,\tau_R)}{s\,\tau_{T1}(1 + s\,\tau_L)} \tag{3.5.8}$$

Now we put Eq. 3.5.2 and Eq. 3.5.8 into Eq. 3.5.1:

$$\frac{v_o}{i_s} = \frac{R_s\,R_L}{\left[R_s + \dfrac{R_{e1}\,(1 + s\,\tau_R)}{s\,\tau_{T1}(1 + s\,\tau_L)}\right] s\,\tau_{T1}(1 + s\tau_L)}$$

$$= \frac{R_s\,R_L}{s^2\,R_s\,\tau_{T1}\,\tau_L + s\,(R_s\,\tau_{T1} + R_{e1}\,\tau_R) + R_{e1}} \tag{3.5.9}$$

Next we put the denominator into the canonical form and equate it to zero:

$$s^2 + s\,\frac{R_s\,\tau_{T1} + R_{e1}\,\tau_R}{R_s\,\tau_{T1}\,\tau_L} + \frac{R_{e1}}{R_s\,\tau_{T1}\,\tau_L} = s^2 + a\,s + b = 0 \tag{3.5.10}$$

where we set the coefficients:

$$a = \frac{R_s\,\tau_{T1} + R_{e1}\,\tau_R}{R_s\,\tau_{T1}\,\tau_L} \quad \text{and} \quad b = \frac{R_{e1}}{R_s\,\tau_{T1}\,\tau_L} \tag{3.5.11}$$

The general solution of Eq. 3.5.10 is:

$$s_{1,2} = -\frac{a}{2} \pm \sqrt{\frac{a^2}{4} - b} \tag{3.5.12}$$

An efficient peaking must have complex poles, so the expression under the square root must be negative, therefore: $b > a^2/4$. We can then extract the negative sign as the imaginary unit and write Eq. 3.5.12 in the form:

$$s_{1,2} = -\frac{a}{2} \pm j\sqrt{b - \frac{a^2}{4}} \tag{3.5.13}$$

From Eq. 3.5.13 we can calculate the tangent section of the pole angle θ:

$$\tan\theta = \frac{\Im\{s_1\}}{\Re\{s_1\}} = \frac{\sqrt{b - \frac{a^2}{4}}}{\frac{a}{2}} = \sqrt{\frac{4\,b}{a^2} - 1} \tag{3.5.14}$$

It follows that:

$$1 + \tan^2\theta = \frac{4\,b}{a^2} \tag{3.5.15}$$

Now we insert the expressions from Eq. 3.5.11 for a and b and obtain:

$$1 + \tan^2\theta = \frac{4\,\frac{R_{e1}}{R_s\,\tau_{T1}\,\tau_L}}{\left(\frac{R_s\,\tau_{T1} + R_{e1}\,\tau_R}{R_s\,\tau_{T1}\,\tau_L}\right)^2} = \frac{4\,R_{e1}\,R_s\,\tau_{T1}\,\tau_L}{(R_s\,\tau_{T1} + R_{e1}\,\tau_R)^2} \tag{3.5.16}$$

By taking the square root the result is:

$$\sqrt{1 + \tan^2\theta} = \frac{2\sqrt{R_{e1}\,R_s\,\tau_{T1}\,\tau_L}}{R_s\,\tau_{T1} + R_{e1}\,\tau_R} \tag{3.5.17}$$

Finally we solve this for τ_R and obtain:

$$\boxed{\tau_R = R\,C = 2\sqrt{\frac{R_s\,\tau_{T1}\,\tau_L}{R_{e1}\left(1 + \tan^2\theta\right)}} - \frac{R_s\,\tau_{T1}}{R_{e1}}} \tag{3.5.18}$$

The admittance Y_{e1} of the emitter circuit in Fig. 3.5.1 is:

$$Y_{e1} = \frac{1}{R_{e1}} + s\,C_{e1} + \frac{1}{R + \frac{1}{s\,C}}$$

$$= \frac{s^2\,CR\,C_{e1}R_{e1} + s\left(CR + CR_{e1} + C_{e1}R_{e1}\right) + 1}{R_{e1}\left(1 + s\,CR\right)} \tag{3.5.19}$$

The emitter impedance Z_{e1} is the inverse value of Y_{e1} and it must be equal to Eq. 3.5.7:

$$Z_{e1} = \frac{R_{e1}\left(1 + s\,CR\right)}{s^2\,CR\,C_{e1}R_{e1} + s\left(CR + CR_{e1} + C_{e1}R_{e1}\right) + 1}$$

$$= \frac{R_{e1}\left(1 + s\,\tau_R\right)}{s^2\,\tau_{T1}\,\tau_L + s\left(\tau_{T1} + \tau_L\right) + 1} \tag{3.5.20}$$

The coefficients of s^2 and s respectively must be equal in both fractions, therefore:

$$CR\,C_{e1}R_{e1} = \tau_{T1}\,\tau_L \tag{3.5.21}$$

and:

$$CR + R_{e1}(C + C_{e1}) = \tau_{T1} + \tau_L \tag{3.5.22}$$

The value of R_{e1} is constrained by the DC current amplification R_L/R_{e1}. Thus we need the expressions for C, C_{e1}, and R. By using Eq. 3.5.18, 3.5.21, and 3.5.22 we obtain:

$$C_{e1} = \frac{\tau_{T1}\,\tau_L}{R_{e1}\,\tau_R} \tag{3.5.23}$$

and:

$$C = \frac{\tau_{T1} + \tau_L - \tau_R - \tau_{T1}\dfrac{\tau_L}{\tau_R}}{R_e} \tag{3.5.24}$$

where τ_R should be calculated by Eq. 3.5.18. Once the value of C is known we can easily calculate the value of the resistor $R = \tau_R/C$. Of course, τ_R is determined by the angle θ of the poles selected for the specified type of response.

Fig. 3.5.2a and 3.5.2b show the normalized pole loci in the complex plane. As seen already in examples in Part 1 and Part 2, to achieve the maximally flat envelope delay response (MFED), a single stage 2nd-order function must have the pole angle $\theta = \pm 150°$. The original circuit has two real poles s_{T1} and s_L, but when the emitter peaking zero s_R is brought close to s_L the poles form a complex conjugate pair.

The frequency response is altered as shown in Fig. 3.5.2c and the bandwidth is extended. The emitter current increase $i_{e1}(\omega)/I_{e1}$ owing to the introduced RC network has two break points: the lower is owed to $R_{e1}(C + C_{e1})$ and the upper is owed to RC. If the break point at ω_R is brought exactly over ω_L they cancel each other, and the final response is shaped by the break point ω_{T1} of the transistor and the second break point in the emitter peaking network, ω_C. The peaking can thus be adjusted by R and C.

Let us consider an example with these data: $f_{T1} = 2000\,\text{MHz}$, $R_s = 60\,\Omega$, $R_e = 20\,\Omega$, $C_o = 9\,\text{pF}$, $R_L = 390\,\Omega$. We want to make the amplifier with such an emitter peaking network which will suit the Bessel pole loci (MFED), where the pole angle $\theta = \pm 150°$. First we calculate both time constants:

$$\tau_{T1} = \frac{1}{2\pi f_{T1}} = \frac{1}{2\pi \cdot 2000 \cdot 10^6} = 79.58\,\text{ps} \tag{3.5.25}$$

and:

$$\tau_L = R_L\,C_o = 390 \cdot 9 \cdot 10^{-12} = 3.51\,\text{ns} \tag{3.5.26}$$

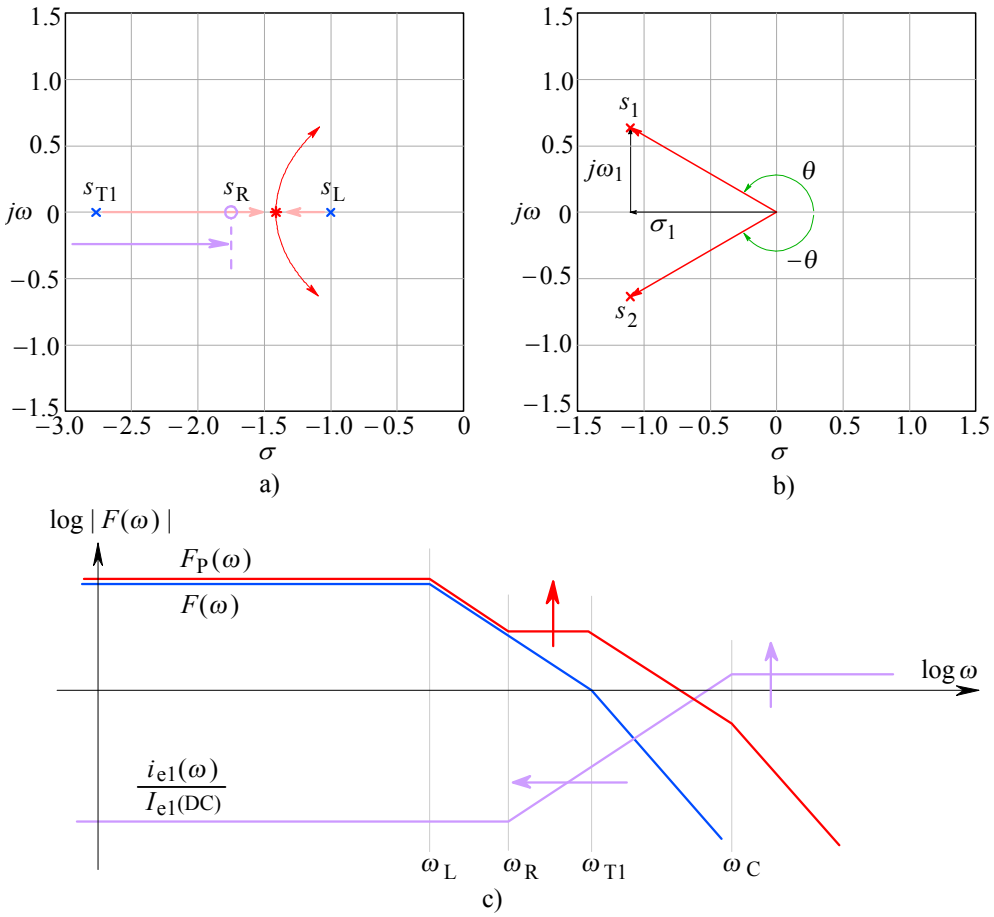

Fig. 3.5.2: Emitter peaking: a) two real poles travel towards each other when the emitter network zero goes from $-\infty$ towards s_L, forming eventually a complex conjugate pair; b) poles for Eq. 3.5.14 for the 2nd-order Bessel (MFED) response. c) frequency response asymptotes — the bandwidth is extended to ω_{T1} if $\omega_R = \omega_L$.

By using Eq. 3.5.18 we then calculate the third time constant:

$$\tau_R = 2\sqrt{\frac{R_s\,\tau_{T1}\,\tau_L}{R_{e1}(1+\tan^2\theta)}} - \frac{R_s\,\tau_{T1}}{R_{e1}} = \tag{3.5.27}$$

$$= 2\sqrt{\frac{60\cdot 79.58\cdot 10^{-12}\cdot 3.51\cdot 10^{-9}}{20\cdot(1+\tan^2 30°)}} - \frac{60\cdot 79.58\cdot 10^{-12}}{20} = 1.35\,\text{ns}$$

Now we can calculate C_{e1} using Eq. 3.5.23:

$$C_{e1} = \frac{\tau_{T1}\,\tau_L}{R_{e1}\,\tau_R} = \frac{79.58\cdot 10^{-12}\cdot 3.51\cdot 10^{-9}}{20\cdot 1.35\cdot 10^{-9}} = 10.35\,\text{pF} \tag{3.5.28}$$

According to Eq. 3.5.24 the value of the capacitor C is:

$$C = \frac{\tau_{T1} + \tau_L - \tau_R - \tau_{T1}\dfrac{\tau_L}{\tau_R}}{R_e} =$$

$$= \frac{79.58 \cdot 10^{-12} + 3.51 \cdot 10^{-9} - 1.35 \cdot 10^{-9} - 79.58 \cdot 10^{-12} \cdot \dfrac{3.51 \cdot 10^{-9}}{1.35 \cdot 10^{-9}}}{20}$$

$$= 101.6\,\text{pF} \tag{3.5.29}$$

Finally we calculate the value of the resistor R, from the time constant τ_R:

$$R = \frac{\tau_R}{C} = \frac{1.35 \cdot 10^{-9}}{101.6 \cdot 10^{-12}} = 13.29\ \Omega \tag{3.5.30}$$

3.5.2 Input Impedance Compensation

The introduction of the peaking elements R and C affects the HF input impedance in an unfavorable way. We have calculated the input impedance at the base emitter junction in Eq. 3.5.8, which we rewrite as:

$$Z_i = \frac{R_{e1}\,(1 + s\,\tau_R)}{s\,\tau_{T1}\,(1 + s\,\tau_L)} = \frac{s\,\tau_R\,R_{e1} + R_{e1}}{s^2\tau_{T1}\,\tau_L + s\,\tau_{T1}} \tag{3.5.31}$$

Here we have an additional pole at $s_L = -\omega_L = -1/\tau_L$ and a zero at $s_R = -\omega_R = -1/\tau_R$, both spoiling the purely capacitive character of the input impedance, which we would like to have (frankly, we would prefer the input capacitance to be zero as well, but this is not feasible). We have seen the Bode plot of the input impedance and its configuration already in Fig. 3.5.1b and 3.5.1c. At very high frequencies, where s becomes dominant, the input impedance obtains a simple capacitive character:

$$Z_i = \frac{R_{e1}\,\tau_R}{s\,\tau_{T1}\,\tau_L} \quad \Rightarrow \quad C_i = \frac{\tau_{T1}\,\tau_L}{R_{e1}\,\tau_R} \tag{3.5.32}$$

Our objective is to keep such an input impedance (at the base-emitter junction of Q_1) at lower frequencies also. In other words, at lower frequencies the plot of the input impedance should correspond to the $|1/sC_i|$ line in Fig. 3.5.1b. All other impedances that appear in the input circuit should be canceled by an appropriate compensating network. To find these impedances, we perform a 'continued fraction expansion' synthesis of the input admittance Y_i as derived from the right side of Eq. 3.5.8. Thus:

$$Y_i = \frac{1}{Z_i} = \frac{s^2\tau_{T1}\,\tau_L + s\,\tau_{T1}}{s\,\tau_R\,R_{e1} + R_{e1}} = s\,\frac{\tau_{T1}\,\tau_L}{R_{e1}\,\tau_R} + \frac{s\,\tau_{T1} - s\,\dfrac{\tau_{T1}\,\tau_L}{\tau_R}}{s\,\tau_R\,R_{e1} + R_{e1}} \tag{3.5.33}$$

The first fraction we recognize to be the input admittance $s\,C_i$. The second fraction can be inverted and, by canceling out s, we obtain the impedance:

$$Z_i' = \frac{s\,\tau_R\,R_{e1} + R_{e1}}{s\,\tau_{T1}\left(1 - \dfrac{\tau_L}{\tau_R}\right)} = \frac{R_{e1}\,\tau_R^2}{\tau_{T1}(\tau_R - \tau_L)} + \frac{R_{e1}\tau_R}{s\,\tau_{T1}(\tau_R - \tau_L)}$$

$$= -\,R_c - \frac{1}{s\,C_c} \tag{3.5.34}$$

This means a resistor $-R_c$ and a capacitor $-C_c$ connected in series, and this combination is in parallel with the input capacitance C_i. The values are negative because $\tau_R < \tau_L$ as was required in Eq. 3.5.6. On the basis of these results we can draw the equivalent input impedance circuit corresponding to Fig. 3.5.1c. The expression for the capacitance C_c is:

$$C_c = \frac{\tau_{T1}(\tau_L - \tau_R)}{R_{e1}\,\tau_R} \tag{3.5.35}$$

From Eq. 3.5.33, as well as from our previous analysis, we can derive that $R_c C_c = \tau_R$ and obtain a simpler expression for R_c:

$$R_c = \frac{\tau_R}{C_c} \tag{3.5.36}$$

Let us now continue our example of the emitter peaking cascode amplifier with the data $R_{e1} = 20\,\Omega$, $\tau_{T1} = 79.58\,\text{ps}$, $\tau_R = 1.51\,\text{ns}$, and $\tau_L = 3.51\,\text{ns}$, and calculate the values of C_i, C_c, and R_c. The input capacitance C_i, without C_M, is:

$$C_i = \frac{\tau_{T1}\,\tau_L}{R_{e1}\,\tau_R} = \frac{79.58 \cdot 10^{-12} \cdot 3.51 \cdot 10^{-9}}{20 \cdot 1.35 \cdot 10^{-9}} = 10.35\,\text{pF} \tag{3.5.37}$$

The value of the capacitance C_c is:

$$C_c = \frac{\tau_{T1}(\tau_L - \tau_R)}{R_{e1}\,\tau_R} = \frac{79.58 \cdot 10^{-12} \cdot (3.51 - 1.35) \cdot 10^{-9}}{20 \cdot 1.35 \cdot 10^{-9}} = 6.37\,\text{pF} \tag{3.5.38}$$

and the resistor R_c has a resistance of:

$$R_c = \frac{\tau_R}{C_c} = \frac{1.35 \cdot 10^{-9}}{3.51 \cdot 10^{-12}} = 385\,\Omega \tag{3.5.39}$$

The next step is to compensate the series connected $-C_c$ and $-R_c$. This can be done by connecting in parallel an equal combination with positive elements. The admittance of such a combination is zero and thus the impedance becomes infinity. The mathematical proof for this operation is:

$$Y_i' = \frac{1}{-R_c - \dfrac{1}{s\,C_c}} + \frac{1}{R_c + \dfrac{1}{s\,C_c}} = 0$$

and:

$$Z_i' = \frac{1}{Y_i'} \Rightarrow \infty \tag{3.5.40}$$

By doing so, only the input capacitances $C_i + C_M$ and the input resistance $(1+\beta)R_{e1}$ remain effective at the (junction) input.

The impedance Z_i as given by Eq. 3.5.8 is effective between the base–emitter junction and the ground. Unfortunately, no direct access is possible to the junction, because from there to the base terminal we have the base spread resistance r_{b1}. This means that r_{b1} must be subtracted from R_c to get the proper value of the compensating resistor. Supposing that $r_{b1} = 25\,\Omega$, the proper compensating resistor is simply:

$$R_c' = R_c - r_{b1} = 385 - 25 = 360\,\Omega \tag{3.5.41}$$

The complete input circuit is shown in Fig. 3.5.3; the input impedance components which are reflected from the emitter to base, are shown in the shaded area.

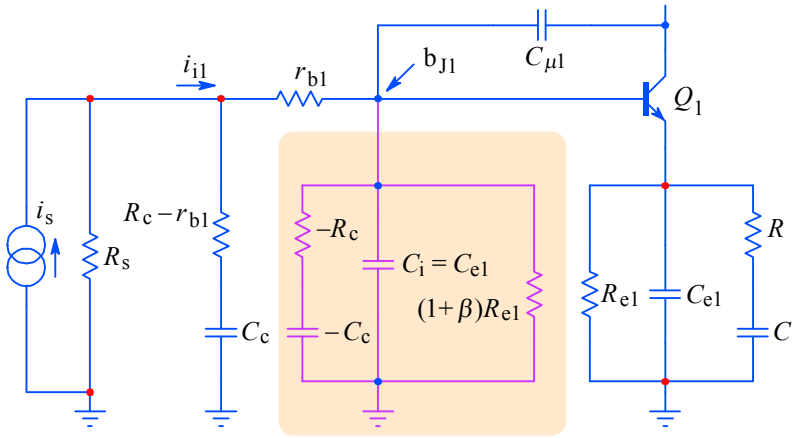

Fig. 3.5.3: The impedances in the emitter are reflected into the base junction of Q_1. The emitter peaking components R and C are reflected into **negative** elements $-R_c$ and $-C_c$, which must be compensated by adding externally an equal and positive R_c and C_c; for proper compensation r_{b1} must be subtracted from R_c.

The compensation of the input impedance is mandatory if we intend to apply an inductive peaking network at the input of that amplifying stage. The equivalent input capacitance, which will be seen as the load by the peaking circuit, is the capacitance from the transistor base–emitter junction to ground, $C_i + C_M$.

However, as mentioned before, these capacitances are seen with the base resistance r_{b1} in series. Also there is a parasitic base lead inductance, in addition to the length of PCB trace and pads having their own stray inductance and capacitance.

Therefore the inductive peaking circuit at the input of a transistor amplifying stage does not see a pure capacitance as its load. Special 'tricks of trade' must be applied, e.g., a modified T-coil peaking at the amplifier input, which we shall discuss in the next section.

3.6 Transistor Interstage T-coil Peaking

In Part 2 we have shown that the greatest bandwidth extension is achieved by using T-coil peaking. The analysis was based on the assumption that the T-coil tap was loaded by a pure capacitance. Unfortunately, for a transistor amplifier this is not the case. In case of a cascode amplifier the emitter network, formed by the parallel connection of $R_e C_e = \tau_T$, is reflected into the base circuit as a parallel connection of $(1+\beta)R_e$ and C_e, paralleled also by the Miller capacitance C_M; to this the series base spread resistance r_b must be added.

In Fig. 3.6.1a we draw such a stage [Ref. 3.5]. Since in the following analysis we do not need the transistor Q_2, we shall consider its emitter input as an ideal ground for the Q_1 collector current signal (of course, the value of the Miller capacitance C_M has to be calculated by considering the actual Q_2 emitter impedance). Thus we can drop the index '1', as all the parameters will belong to Q_1 only. To further simplify the analysis, we shall neglect the damping and thermal compensation impedances Z_d and Z_θ, as well as the emitter peaking. The resistor R_L is the T-coil loading resistor, which is also the load of the driving stage and we shall assume that its other end is also connected to an ideal AC ground. Fig. 3.6.1b shows the T-coil loaded by the equivalent small signal, high frequency input impedance of the transistor Q_1.

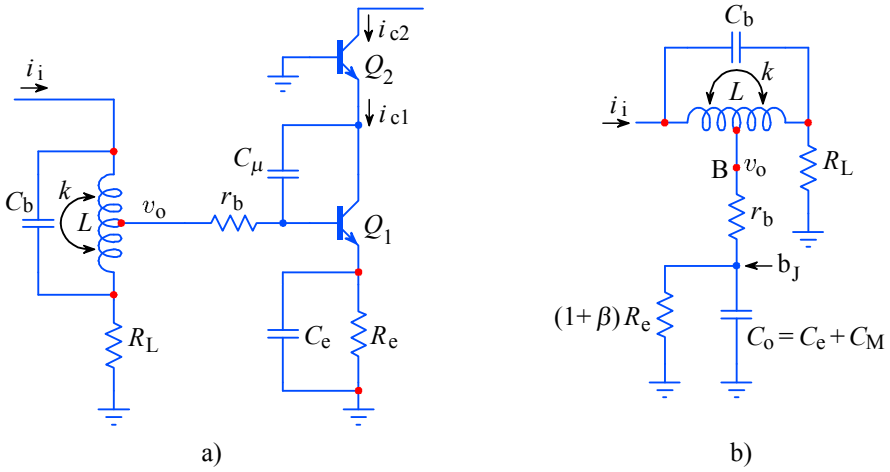

Fig. 3.6.1: a) The cascode amplifier with a T-coil interstage network. b) The T-coil loaded by the equivalent small signal, high frequency input impedance.

To prevent any confusion we must stress that C_b is the T-coil bridging capacitance, and not the base capacitance which is represented by $C_o = C_e + C_M$. As we know from the symmetrical T-coil analysis in Part 2, Sec. 2.4:

$$L = L_a + L_b = R_L^2\, C_o \tag{3.6.1}$$

Since the input shunt resistance $(1+\beta)R_e$ is usually much higher than r_b, we shall neglect it also, thus arriving at the circuit in Fig. 3.6.2a. Fig. 3.6.2b shows the equivalent T-coil circuit in which we have replaced the magnetic field coupling factor k with the negative mutual inductance $-L_M$ and the coil branches by their equivalent inductances L_a and L_b. Finally, in Fig. 3.6.2c we have replaced the branch impedances by symbols ***A*** to ***E*** to determine the three current loops I_1, I_2, I_3.

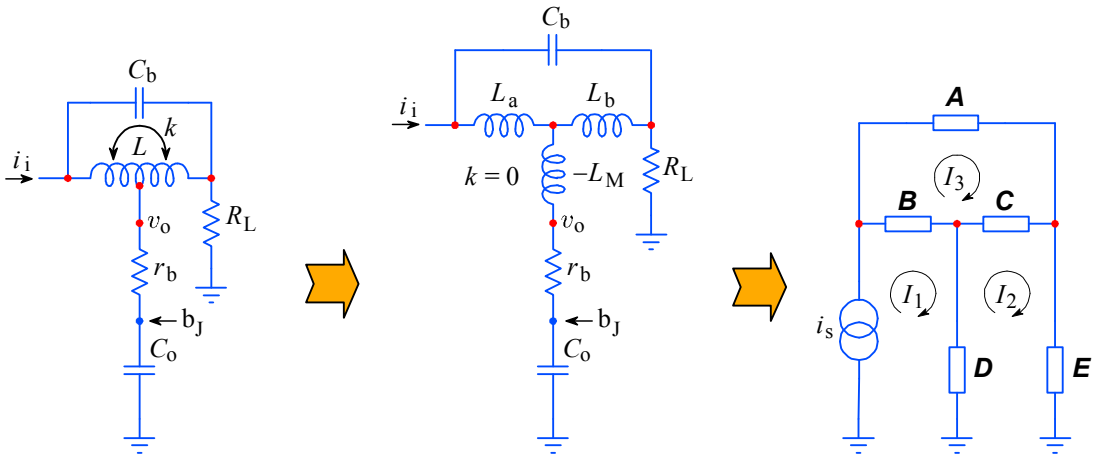

Fig. 3.6.2: a) The T-coil loaded by the simplified input impedance; b) the equivalent T-coil circuit in which k is substituted by $-L_M$; c) the equivalent branch impedances and the three current loops.

By comparing Fig. 2.4.1b,c, Sec. 2.4 with Fig. 3.6.2b,c we see that they are almost equal, except that in the branch ***D***, we have the additional series resistance r_b. Let us list all these impedances again, but now including r_b:

$$\begin{aligned} \boldsymbol{A} &= \frac{1}{s\,C_b} \\ \boldsymbol{B} &= sL_a \\ \boldsymbol{C} &= sL_b \\ \boldsymbol{D} &= -s\,L_M + r_b + \frac{1}{s\,C_o} \\ \boldsymbol{E} &= R_L \end{aligned} \tag{3.6.2}$$

The general analysis of the branches, Eq. 2.4.6–2.4.13, showed that the input impedance of the T-coil network is equal to its loading impedance $Z_i = \boldsymbol{E} = R_L$. As we shall soon see, r_b between the T-coil tap and C_o spoils this nice property; we shall have to compensate it. The analysis here is similar to that in Sec. 2.4, so we do not have to repeat it. Here we give the final result, Eq. 2.4.14, for convenience:

$$\boldsymbol{BCA} + \boldsymbol{BDA} + \boldsymbol{BEA} + \boldsymbol{DCA} - \boldsymbol{ECA} - \boldsymbol{E}^2\boldsymbol{A} - \boldsymbol{E}^2\boldsymbol{B} - \boldsymbol{E}^2\boldsymbol{C} = 0 \tag{3.6.3}$$

By entering all substitutions from Eq. 3.6.2, performing all the required multiplications and arranging the terms in the decreasing powers of s, we obtain:

$$s\left[\left(\frac{L_a L_b}{C_b} - \frac{L\,L_M}{C_b}\right) - R_L^2\,L\right] + \frac{L\,r_b}{C_b} + \frac{R_L}{C_b}(L_a - L_b) + \frac{1}{s}\left(\frac{L}{C_o\,C_b} - \frac{R_L^2}{C_b}\right) = 0 \tag{3.6.4}$$

or, more simply:

$$s\,K_1 + K_2 + s^{-1}K_3 = 0 \tag{3.6.5}$$

The difference between Eq. 3.6.4, 3.6.5 and Eq. 2.4.15, 2.4.16 is in the middle term. Again, if we want to have an input impedance independent of the frequency s, then each of the coefficients K_1, K_2, and K_3 must be zero [Ref. 3.5]:

$$K_1 = \frac{-\,L\,L_\mathrm{M}}{C_\mathrm{b}} + \frac{L_\mathrm{a}\,L_\mathrm{b}}{C_\mathrm{b}} - R_\mathrm{L}^2\,L = 0$$

$$K_2 = \frac{L\,r_\mathrm{b}}{C_\mathrm{b}} + \frac{R_\mathrm{L}}{C_\mathrm{b}}\,(L_\mathrm{a} - L_\mathrm{b}) = 0$$

$$K_3 = \frac{L}{C_\mathrm{o}\,C_\mathrm{b}} - \frac{R_\mathrm{L}^2}{C_\mathrm{b}} = 0 \qquad (3.6.6)$$

So we have the three equations from which we can calculate the parameters L_a, L_b, and L_M. By considering Eq. 3.6.1 we obtain:

$$L_\mathrm{a} = \frac{L}{2}\left(1 - \frac{r_\mathrm{b}}{R_\mathrm{L}}\right) = \frac{R_\mathrm{L}^2\,C_\mathrm{o}}{2}\left(1 - \frac{r_\mathrm{b}}{R_\mathrm{L}}\right) \qquad (3.6.7)$$

$$L_\mathrm{b} = \frac{L}{2}\left(1 + \frac{r_\mathrm{b}}{R_\mathrm{L}}\right) = \frac{R_\mathrm{L}^2\,C_\mathrm{o}}{2}\left(1 + \frac{r_\mathrm{b}}{R_\mathrm{L}}\right) \qquad (3.6.8)$$

$$L_\mathrm{M} = \frac{L}{4}\left(1 - \frac{r_\mathrm{b}^2}{R_\mathrm{L}^2}\right) - R_\mathrm{L}^2\,C_\mathrm{b} = \frac{R_\mathrm{L}^2\,C_\mathrm{o}}{4}\left(1 - \frac{r_\mathrm{b}^2}{R_\mathrm{L}^2}\right) - R_\mathrm{L}^2\,C_\mathrm{b} \qquad (3.6.9)$$

Two interesting facts become evident from Eq. 3.6.7 and 3.6.8. First, $L_\mathrm{a} < L_\mathrm{b}$, and this means that **the coil tap is not at the coil's center** any longer, but it is moved towards the coil's signal input node. Secondly, R_L must always be larger than r_b, otherwise L_a becomes negative. But we reach the limit of realizability long before that, since we know from Part 2 that $L_1 = L_\mathrm{a} - L_\mathrm{M}$ (and also $L_2 = L_\mathrm{b} - L_\mathrm{M}$).

In Eq. 3.6.9 we have two unknowns, L_M and C_b; therefore we need a fourth equation to calculate them. Similarly as we did in Part 2, Sec. 2.4, we shall use the transimpedance equation for this purpose. The procedure is well described from Eq. 2.4.20 to 2.4.24 and we write the last one again:

$$\frac{V_\mathrm{o}}{I_1} = \frac{1}{s\,C_0} \cdot \frac{\boldsymbol{CA + EA + EB + EC}}{\boldsymbol{CA + CB + DA + DB + DC + EA + EB + EC}} \qquad (3.6.10)$$

If we insert the substitutions from Eq. 3.6.2, we obtain the following result:

$$F(s) = \frac{V_\mathrm{o}}{I_1} = \frac{R_\mathrm{L}}{s^2\,R_\mathrm{L}^2\,C_\mathrm{o}\,C_\mathrm{b} + s\,C_\mathrm{o}\,\dfrac{R_\mathrm{L} + r_\mathrm{b}}{2} + 1} \qquad (3.6.11)$$

In a similar way, for the transimpedance from the input to R_L we would obtain:

$$\frac{V_\mathrm{R}}{I_\mathrm{i}} = R_\mathrm{L}\,\frac{s^2\,R_\mathrm{L}^2\,C_\mathrm{o}\,C_\mathrm{b} - s\,C_\mathrm{o}\,\dfrac{R_\mathrm{L} - r_\mathrm{b}}{2} + 1}{s^2\,R_\mathrm{L}^2\,C_\mathrm{o}\,C_\mathrm{b} + s\,C_\mathrm{o}\,\dfrac{R_\mathrm{L} + r_\mathrm{b}}{2} + 1} \qquad (3.6.12)$$

Since we have the factor $(R_L - r_b)$ in the numerator and a different factor $(R_L + r_b)$ in the denominator, this means that **the two zeros are not symmetrically placed** in relation to the two poles in the s-plane. Therefore Eq. 3.6.12 does not describe an all pass network and the input impedance is not simply R_L as before. This represents the basic obstacle to using T-coils in a transistor distributed amplifier, because the T-coil load can not be replaced by another T-coil network (for comparison see [Ref. 2.18 and 2.19]).

Eq. 3.6.11 has two poles, which we calculate from the canonical form of the denominator:

$$s^2 + s\,\frac{R_L + r_b}{2\,R_L^2\,C_b} + \frac{1}{R_L^2\,C_o C_b} = 0 \tag{3.6.13}$$

and both poles are:

$$s_{1,2} = -\frac{R_L + r_b}{4\,R_L^2\,C_b} \pm \sqrt{\left(\frac{R_L + r_b}{4\,R_L^2\,C_b}\right)^2 - \frac{1}{R_L^2\,C_o C_b}} \tag{3.6.14}$$

or, by extracting the common factor:

$$s_{1,2} = \frac{1 + r_b/R_L}{4\,C_b R_L}\left(-1 \pm \sqrt{1 - \frac{16\,C_b}{C_o\,(1 + r_b/R_L)^2}}\right) \tag{3.6.15}$$

An efficient inductive peaking must have complex poles. For Bessel poles, as was in Fig. 3.5.2b, the pole angles $\theta_{1,2} = \pm 150°$ and with this pole arrangement we obtain the MFED response. If the poles are complex the tangent of the pole angle is the ratio of the imaginary to the real component of Eq. 3.6.15:

$$\tan\theta = \frac{\Im\{s_1\}}{\Re\{s_1\}} = \sqrt{\frac{16\,C_b}{C_o\,(1 + r_b/R_L)^2} - 1} \tag{3.6.16}$$

By solving this equation for C_b we obtain:

$$C_b = C_o\,\frac{1 + \tan^2\theta}{16}\left(1 + \frac{r_b}{R_L}\right)^2 \tag{3.6.17}$$

Compared to the symmetrical T-coil, here we have the additional factor $(1 + r_b/R_L)^2$. For Bessel poles $\theta = 150° = 5\pi/6$ and $\tan^2\theta = 1/3$, thus for a single stage case:

$$C_b = \frac{C_o}{12}\left(1 + \frac{r_b}{R_L}\right)^2 \tag{3.6.18}$$

If we replace C_b in Eq. 3.6.9 with Eq. 3.6.18, the mutual inductance is:

$$L_M = R_L^2\,C_o\left[\frac{1}{4}\left(1 - \frac{r_b^2}{R_L^2}\right) - \frac{1}{12}\left(1 + \frac{r_b}{R_L}\right)^2\right] \tag{3.6.19}$$

With this we can calculate the coupling factor k between the coil L_1 and L_2 [Ref. 3.23]:

$$k = \frac{L_M}{\sqrt{L_1\,L_2}} = \frac{L_M}{\sqrt{(L_a - L_M)\,(L_b - L_M)}} \tag{3.6.20}$$

Now we have all the equations needed for the T-coil transistor interstage coupling.

3.6.1 Frequency response

To calculate the frequency response we apply Eq. 3.6.11, in which we shall replace the coil's bridging capacitance C_b by Eq. 3.6.18, since we shall discuss only the MFED response. Then we put it into the canonical form by factoring out the common factor:

$$F(s) = \frac{R_L^2\, C_o^2 \left(1 + \frac{r_b}{R_L}\right)^2}{12} \cdot \frac{R_L}{s^2 + s\,\frac{6}{R_L\, C_o}\left(1 + \frac{r_b}{R_L}\right) + \frac{12}{R_L^2\, C_o^2}\left(1 + \frac{r_b}{R_L}\right)} \tag{3.6.21}$$

The denominator of the second fraction has two roots:

$$s_{1,2} = \frac{1}{R_L\, C_o\, (1 + r_b/R_L)}\,(-3 \pm j\sqrt{3}\,) = \sigma_1 \pm j\,\omega_1 \tag{3.6.22}$$

Sometimes we prefer the normalized form of the roots and in this case $R_L C_o = 1/\omega_h = 1$. To emphasize the normalization, we add the subscript 'n', so $s_{1,2n} = \sigma_{1n} \pm j\,\omega_{1n}$. By applying the normalized poles of Eq. 3.6.22 to Eq. 2.2.27, which is a generalized second-order magnitude function, we obtain:

$$\left|F(\omega)\right| = \frac{\sigma_{1n}^2 + \omega_{1n}^2}{\sqrt{\left[\sigma_{1n}^2 + \left(\frac{\omega}{\omega_h} + \omega_{1n}\right)^2\right]\left[\sigma_{1n}^2 + \left(\frac{\omega}{\omega_h} - \omega_{1n}\right)^2\right]}} \tag{3.6.23}$$

By comparing the Bessel poles for a simple T-coil (Eq. 2.4.42) with Eq. 3.6.22, we notice that in the denominator we have an additional factor $(1 + r_b/R_L)$. Therefore it would be interesting to make several frequency responses with different ratios r_b/R_L, as listed in Table 3.6.1:

Table 3.6.1

r_b/R_L	σ_{1n}	ω_{1n}	Note
0.00	− 3.0	− 1.732	symmetrical T-coil
0.25	− 2.4	− 1.386	-
0.50	− 2.0	− 1.155	-

The corresponding frequency-response plots are drawn in Fig. 3.6.3, together with the three non-peaking responses ($L = 0$) as references. The bandwidth improvement factor for all three cases is $\eta_b = 2.72$. That is because the base resistance r_b decreases the bandwidth also for the non-peaking stage, where $L = 0$. We can prove this if we multiply the denominator of Eq. 3.6.22 by R_L:

$$s_{1,2} = \frac{1}{C_o\,(R_L + r_b)}\,(-3 \pm j\,\sqrt{3}\,) = \omega_h\,(-3 \pm j\,\sqrt{3}\,) \tag{3.6.24}$$

where $\omega_h = 1/C_o(R_L + r_b)$ is the non-peaking bandwidth considering r_b. So we shall obtain three different curves for three different ratios r_b/R_L, also for $L = 0$.

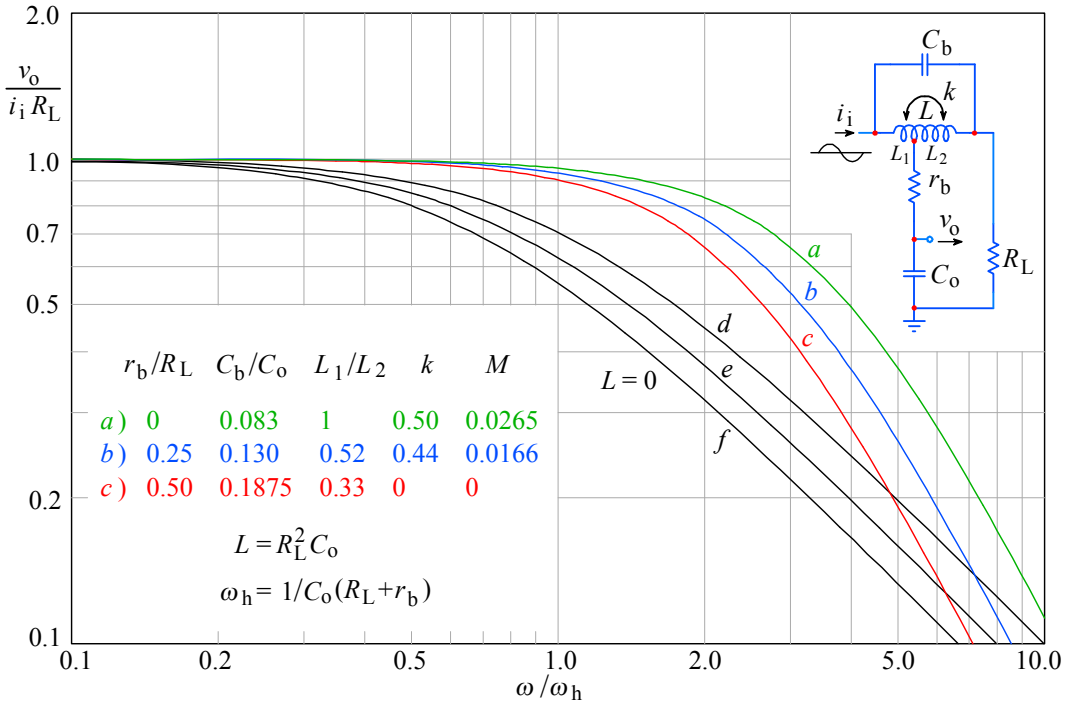

Fig. 3.6.3: MFED frequency response of the T-Coil transistor interstage coupling circuit for three different values of r_b: a) $r_b = 0$; b) $r_b = 0.25\,R_L$; c) $r_b = 0.5\,R_L$. For comparison the three reference cases ($L = 0$): d), e), and f), which correspond to the same three r_b/R_L ratios, are drawn. The bandwidth improvement factor of the peaking system remains 2.72 times over the non-peaking reference for each value of r_b.

From the analysis above, we can draw an important result:

The upper half-power frequency of a non-peaking transistor amplifier must be calculated by taking into account the sum $R_L + r_b$ (and not just R_L).

3.6.2 Phase Response

To calculate the phase response we insert our poles into Eq. 2.2.31:

$$\varphi = \arctan\frac{\omega/\omega_h + \omega_{1n}}{\sigma_{1n}} + \arctan\frac{\omega/\omega_h - \omega_{1n}}{\sigma_{1n}} \qquad (3.6.25)$$

In Fig. 3.6.4 the phase plots for the same three ratios of r_b/R_L as in the frequency response are shown, along with the three references ($L = 0$).

3.6.3 Envelope Delay

The envelope delay is calculated using Eq. 2.2.35:

$$\tau_e\,\omega_h = \frac{\sigma_{1n}}{\sigma_{1n}^2 + (\omega/\omega_h + \omega_{1n})^2} + \frac{\sigma_{1n}}{\sigma_{1n}^2 + (\omega/\omega_h - \omega_{1n})^2} \qquad (3.6.26)$$

and the responses are drawn in Fig. 3.6.5, for the three different ratios r_b/R_L, in addition to the three references ($L = 0$).

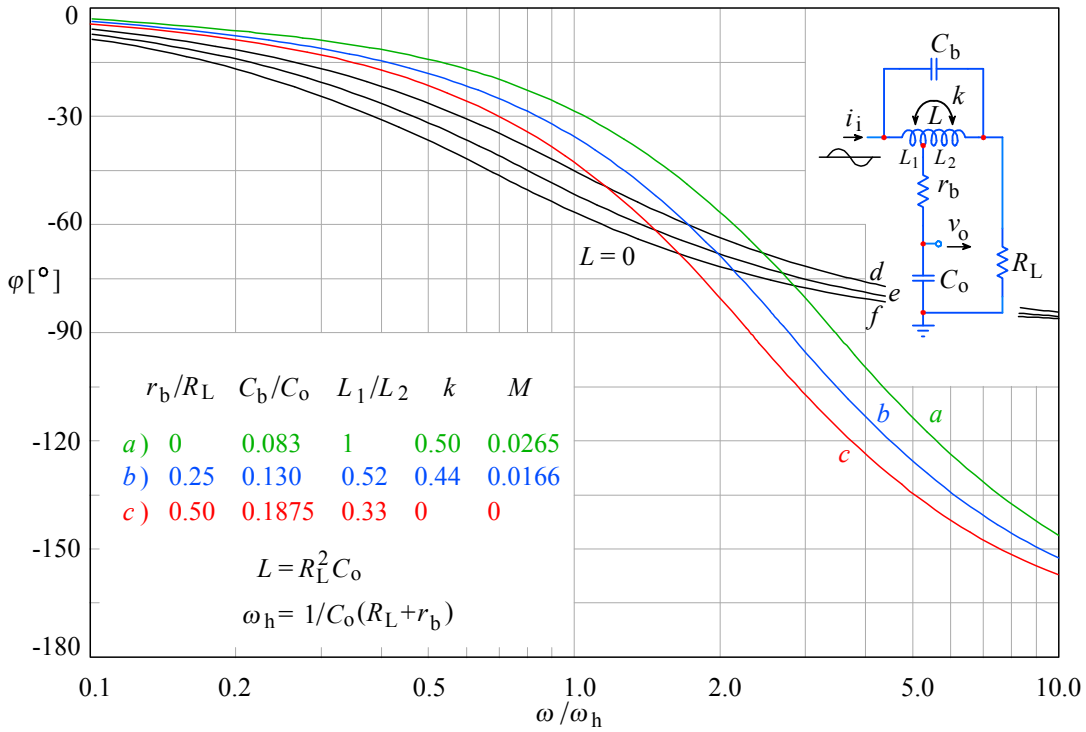

Fig. 3.6.4: MFED phase response of the T-Coil transistor interstage coupling circuit compared with the references ($L = 0$), for the same three values of r_b/R_L.

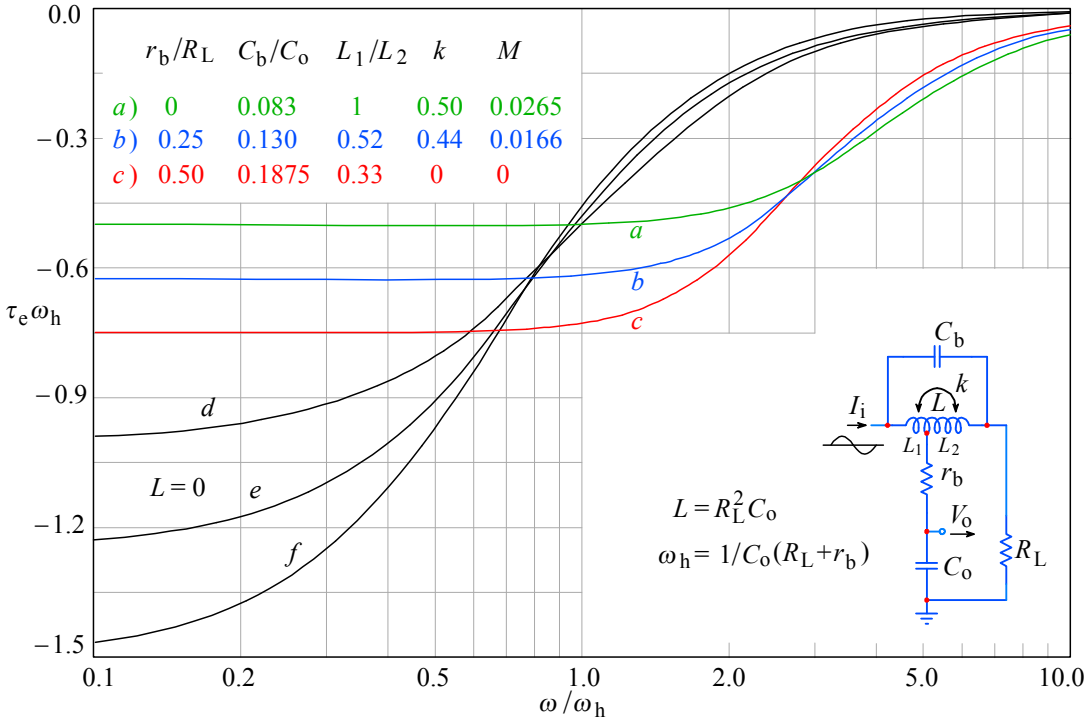

Fig. 3.6.5: MFED envelope delay response of the T-Coil transistor interstage coupling circuit compared with the references ($L = 0$) for the same three values of r_b/R_L.

3.6.4 Step Response

For plotting the step response we can use Eq. 2.4.47 (which was fully derived in Part 1, Eq. 1.14.18):

$$g(t) = 1 + \frac{1}{|\sin\theta|}\, e^{\sigma_1 t} \sin(\omega_1 t + \theta + \pi) \tag{3.6.27}$$

where θ is the pole angle according to Fig. 3.5.2b. By inserting the pole angle $\theta = 150°$ or $5\pi/6$, as required by the 2nd-order Bessel system, we obtain:

$$g(t) = 1 + 2\, e^{-3\,t/T} \sin\left[\sqrt{3}\ t/T + \left(1 + \frac{5}{6}\right)\pi\right] \tag{3.6.28}$$

However, here we must use $T = 1/\omega_h = C_o\,(R_L + r_b)$, as in Eq. 3.6.22 and 3.6.24. In Fig. 3.6.6 the step-response plots are drawn for three different ratios r_b/R_L as well as the three reference cases with $L = 0$.

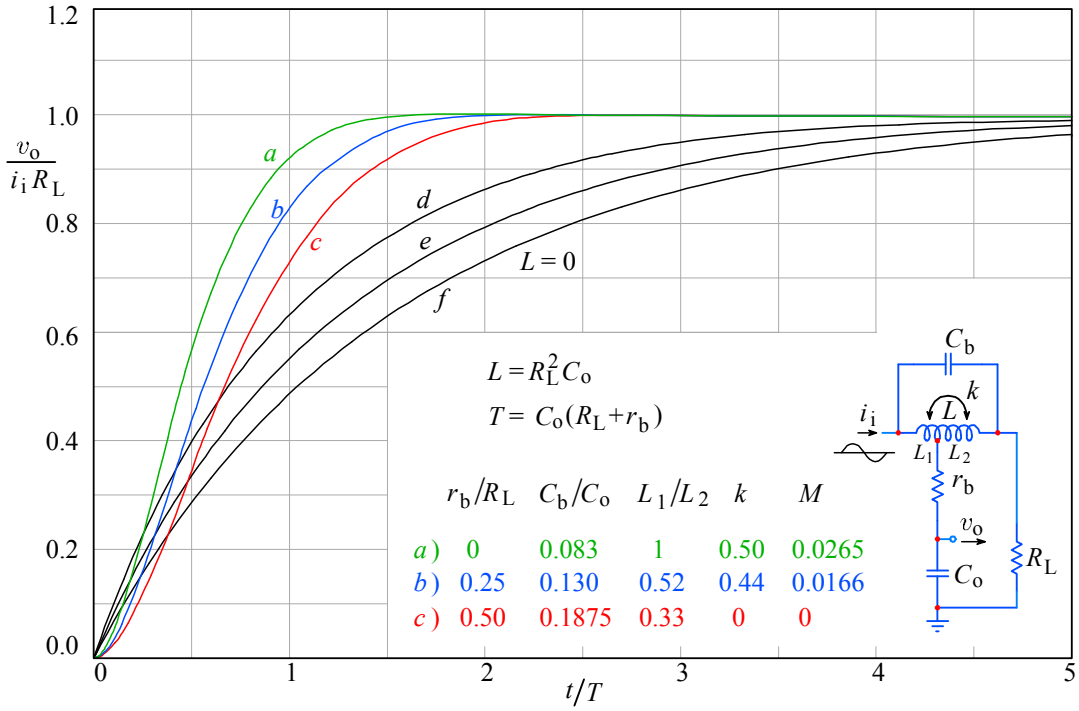

Fig. 3.6.6: MFED step-response of the T-coil transistor interstage coupling circuit, compared to the references ($L = 0$), for the same three values of r_b/R_L.

Thus we have completed the analysis of the basic case of a transistor T-coil interstage coupling. The reader who would like to have more information should study [Ref. 3.5]. In order to simplify the analysis, we have purposely neglected the transistor input resistance $\beta\,(r_\pi + 1)$ and also stray inductance L_s of the tap to transistor base terminal. In the next steps we shall discuss both of them.

3.6.5 Consideration of the transistor's input resistance

Fig. 3.6.7 shows the basic configuration of the transistor input circuit. We have also drawn the base-lead inductance L_s which will be discussed in the next section.

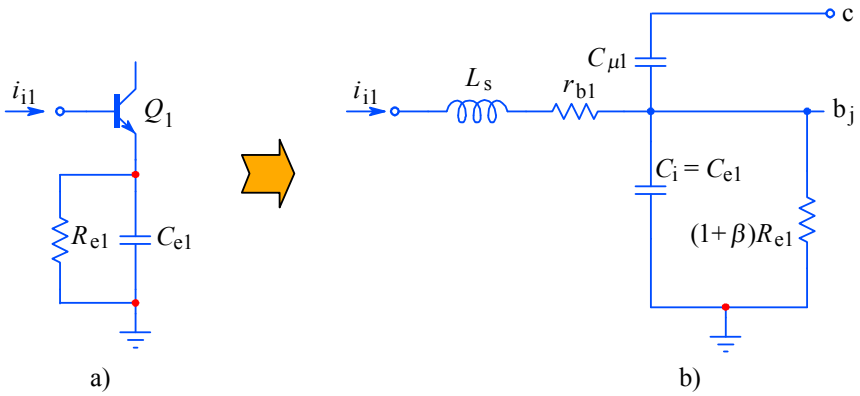

Fig. 3.6.7: The complete transistor input impedance: a) schematic; b) equivalent circuit, in which we include also the base lead inductance L_{b1}. The presence of the shunt resistance $(1 + \beta)\, R_{e1}$ requires a modified interstage T-coil circuit.

The resistance from the base–emitter junction to ground is:

$$R_i = (1 + \beta)\, R_e \tag{3.6.29}$$

as we have derived in Eq. 3.2.15. The effect of this resistance may be canceled if we insert an appropriate resistor R_s from the end of coil L_1 to the start of coil L_2, as shown in Fig. 3.6.8. It is essential that the resistor R_s is inserted on the 'left' side of L_2 (at the T-coil tap node), because in this case the bridging capacitance of C_b (self-capacitance of the coil) and the magnetic field coupling (k) are utilized. With the resistor placed on the 'right' side of L_2 (at the $R_L\, C_b$ node) , that would not be the case.

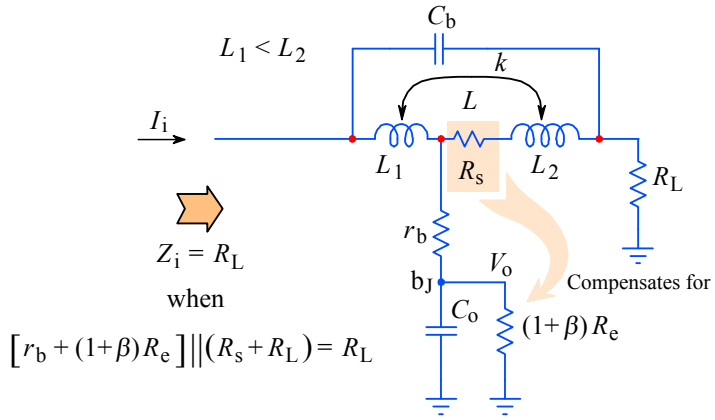

Fig. 3.6.8: The resistance R_s in series with L_2 is inserted near the T-coil tap to compensate the error in the impedance seen by the input current at low frequencies, owed to the parallel connection of $R_L\,||\,[r_b + (1 + \beta)R_e]$.

At very high frequencies we can replace all capacitors by short circuit and all inductors by open circuit. In this case the input resistance of the T-coil circuit is R_L. But

at very low frequencies the capacitors represent an open circuit and the inductors a short circuit. The transistor input resistance is then effectively in parallel with R_L. It is the task of the series resistor R_s to prevent this reduction of resistance. The idea is that:

$$(r_b + R_i) \,||\, (R_s + R_L) = R_L \tag{3.6.30}$$

If we solve this for R_s we obtain:

$$R_s = \frac{R_L^2}{R_i + r_b - R_L} \tag{3.6.31}$$

The introduction of this resistor spoils all the expressions from our previous analysis, and, to be exact, everything we derived to determine the basic T-coil parameters should be calculated anew, considering the additional parameter R_s. Since in practice the value of this resistor is very small, no substantial changes in other circuit parameters may be expected and the additional effort, which would be required by an exact analysis, would be worthless.

A sneaky method for implementing this compensation, while at the same time decreasing the stray capacitance (and also to create difficulties to the competition to copy the circuit) is to make the coil L_2 using an appropriate resistive wire.

3.6.6 Consideration of the base lead stray inductance

Fig. 3.6.9a shows the T-coil with the base lead stray inductance L_s at the tap. From Fig. 3.6.9b we realize that the **positive** inductance of the base lead L_s actually decreases the **negative** mutual inductance L_M of the T-coil. To retain the same conditions as in Fig. 3.6.2c at the beginning of the basic T-coil analysis, the coupling factor must be increased, thus increasing the mutual inductance to $L_M + L_s$.

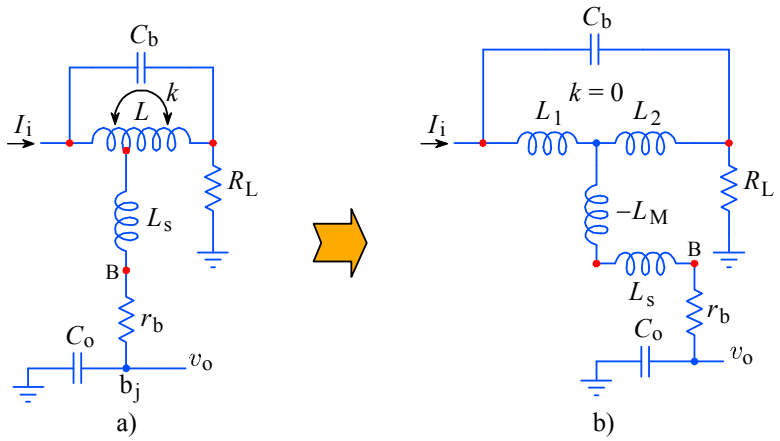

Fig. 3.6.9: a) The base lead inductance L_s decreases the value of mutual inductance, as indicated by the equivalent circuit in b). This can be compensated by recalculating the circuit with an increased coupling factor.

We shall mark the new T-coil circuit parameters with a prime (′) to distinguish them from the original parameters of the transistor interstage T-coil:

$$L'_M = L_M + L_s \tag{3.6.32}$$

Because the inductance from r_b to either end of the coil L is now increased by L_s, both inductances L_a and L_b must be decreased by the value of L_s:

$$L'_a = L_a - L_s \quad \text{and} \quad L'_b = L_b - L_s \tag{3.6.33}$$

By considering all these changes, the new (larger) value of the coupling factor is

$$k' = \frac{L'_M}{\sqrt{(L_a - L_M - 2\,L_s)\,(L_b - L_M - 2\,L_s)}} \tag{3.6.34}$$

Since it is sometimes difficult to achieve the required coupling factor we must take care that the base lead stray inductance L_s is as small as possible.

3.6.7 Consideration of the collector to base spread capacitance

So far we have considered only the lumped collector to base capacitance C_μ. However, in a real transistor the capacitance C_μ is spread along the base resistance r_b, as is drawn in Fig. 3.6.10a [Ref. 3.4]. For the analysis of such a circuit we should know the actual geometry involved; unless we are designing the transistor by ourselves, this would be difficult to find out. So we shall, rather, approximate this by splitting C_μ into three parts, $C_{\mu 1}$, $C_{\mu 2}$, and $C_{\mu 3}$, as suggested in Fig. 3.6.10b, adding also a constant value C_s to account for the external leads and PCB strays.

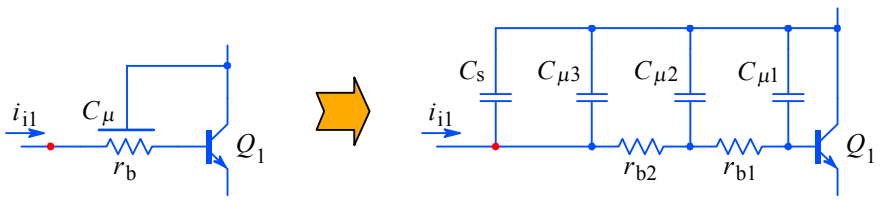

Fig. 3.6.10: a) The base–collector reverse capacitance C_μ is actually spread across the base resistance r_b. b) A good approximation is achieved by splitting r_b in half and C_μ in three parts, adding also the external stray capacitance C_s.

Those readers who are interested in the results and further suggestions, should study [Ref. 3.20].

3.6.8 The 'Folded' Cascode

While we are still speaking about cascode amplifiers, let us examine the 'folded' cascode circuit, Fig. 3.6.11. This circuit is a handy solution in cases of a limited supply voltage, a situation commonly encountered in modern integrated circuits and battery supplied equipment.

The first thing to note is that the collector DC currents can be different, since the bias conditions for Q_1 are set by the input base voltage and R_{e1} , whilst for Q_2 the bias is set by $V_{cc} - V_{b2}$ and R_{cc} .

Another interesting point is that R_{cc} (or a current source in its place) must supply the current for both transistors. Therefore when a signal is applied at the input the currents in Q_1 and Q_2 will be in anti-phase, i.e., when i_{o1} increases, i_{i2} decreases and vice-versa. Consequently, it is easier to achieve good thermal balance with such a circuit, than with the original cascode.

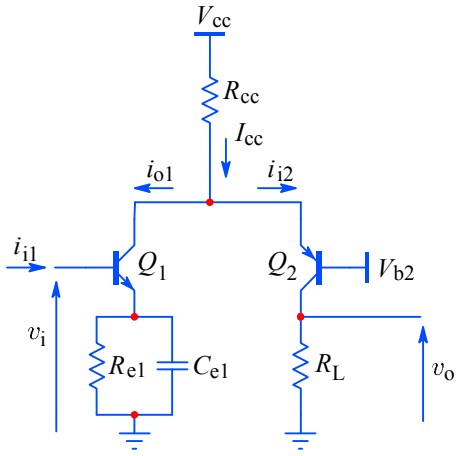

Fig. 3.6.11: The 'folded' cascode is formed by a complementary, NPN and PNP, transistor pair, connected in the otherwise usual cascode configuration. Since thermionic devices are not produced in complementary pairs, this circuit can not be realized with electronic tubes.

In an integrated circuit it is always more difficult to make fast PNP transistors, because of the lower mobility of the virtual positive charge (a vacant charge region, left behind an accelerated electron, can exist for a considerable time before another slow electron comes near enough to be trapped by it). It could then be advantageous to change the supply polarity and use a PNP type for Q_1 and an NPN type for Q_2.

In all other respects, the circuit presents problems identical to those of the original cascode, so all the solutions already discussed apply here as well.

3.7 Differential Amplifiers

In Sec. 3.4.2 we have explained that the instability of the transistor's DC bias depends on the ambient temperature and the heat generated internally, as a consequence of its power dissipation. The current amplification factor β_0 also depends on temperature. These effects multiply in a multi-stage DC amplifier. They can be greatly reduced using a symmetrical differential amplifier.

The basic differential amplifier is shown in Fig. 3.7.1. The input voltage of transistor Q_1 is v_{i1} and that of Q_2 is $v_{i2} = -v_{i1}$ (we are assuming these symmetrical driving voltages in order to eliminate any common mode voltages, thus simplifying the initial analysis). The emitters of both transistors are connected together and fed via the resistor R_{ee} from the voltage $V_{ee} < 0$. If we assume the circuit to be entirely symmetrical, e.g., $Q_1 = Q_2$ and $R_{L1} = R_{L2}$, and if both input voltages v_{i1} and v_{i2} are zero, the DC Output voltages are also equal, $V_{o1} = V_{o2}$, independently of the ambient temperature.

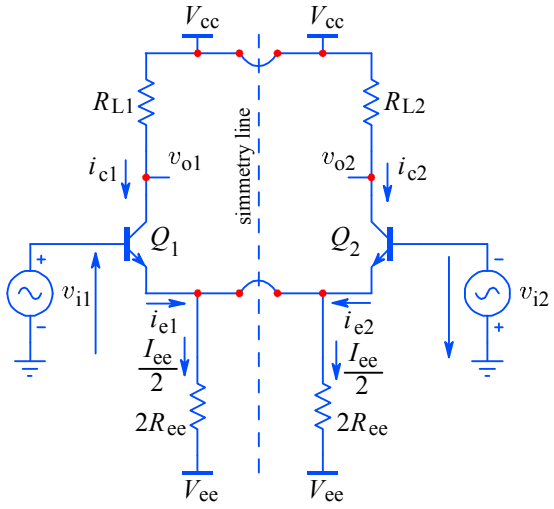

Fig. 3.7.1: The differential amplifier. We simplify the initial analysis by assuming $v_{i2} = -v_{i1}$, $R_{L1} = R_{L2}$ and $Q_1 = Q_2$ (all parameters).

The name *differential amplifier* suggests that we are interested in the amplification of voltage differences. In general, if one signal input voltage, say, v_{i1}, goes positive, the other input voltage v_{i2} goes negative by the same amount (we have accounted for this by drawing the polarity of the voltage generator v_{i2} in Fig. 3.7.1 opposite to v_{i1}). This means that any increase of the emitter current in transistor Q_1 is accompanied by an equal decrease in the emitter current in transistor Q_2. So the current through the resistor R_{ee} and the voltage at the emitter node are not changed. Therefore we can consider the emitter node as a virtual ground. The difference of the input voltages is:

$$v_{i1} - (-v_{i2}) = v_{i1} + v_{i2} \tag{3.7.1}$$

In a similar way as the input voltages, the signal output voltages v_{o1} and v_{o2} go up and down for an equal amount, however, we must account for the signal inversion in

the common emitter amplifier. If the voltage amplification of the input voltage difference is A_{vd} (which we can take directly from Eq. 3.1.14, where we discussed a simple common-base amplifier), the output signal voltage difference is:

$$v_{o2} - (-v_{o1}) = v_{o1} + v_{o2} = -A_{vd}\,(v_{i1} + v_{i2}) \tag{3.7.2}$$

An attentive reader will note that we have added the subscript 'd' to denote the differential mode gain.

In the case of both input voltages being equal and of the same polarity, both output voltages will also be equal and of same polarity; however, the output signal's polarity is the inverse of the input signal's polarity (owing to the 180° phase inversion of each common emitter amplifier stage). If the symmetry of the circuit were perfect, the output voltage difference would be zero, provided that the common mode excitation at the input remains well within the linear range of the amplifier. Such operation is named *common-mode amplification*, A_{vc} (here we have added the subscript 'c').

For the common mode signal the excursion of both output voltages with respect to their DC value is:

$$v_{o1} = v_{o2} = -A_{vc}\,\frac{v_{i1} + v_{i2}}{2} \approx -\frac{R_{L1}}{2\,R_{ee}}\,(v_{i1} + v_{i2}) \tag{3.7.3}$$

A good idea to visualize the common mode operation is to 'fold' the circuit across the symmetry line and consider it as a 'single ended' amplifier with both transistors and both loading resistors in parallel.

Since we are more interested in the differential mode amplification, we have pulled the expression for the common mode amplification, so to say, 'out of the hat'. The analysis so far is more intuitive than exact. The reason we did not bother to make a corresponding derivation of exact formulae is that the simple circuit shown in Fig. 3.7.1 is almost never used as a wideband amplifier owing to its large input capacitance. A basic differential amplifier in cascode configuration, with a constant current generator instead of the resistor R_{ee}, is drawn in Fig. 3.7.2. The reader who wants to study the full analysis of the basic low-frequency differential amplifier according to Fig. 3.7.1 should look in [Ref. 3.7]. We shall return briefly to the differential amplifier in Part 5.

3.7.1 Differential cascode amplifier

The analysis of the circuit in Fig. 3.7.2, a differential cascode amplifier, with the same rigor, considering all the complex impedances, would quickly run out of control owing to its complexity (remember Table 3.2.1, which should be applied to each transistor). However, if we take the emitter node to be a virtual ground, each half of the differential amplifier can be analyzed separately; actually, owing to the symmetry, the analysis of only one arm is needed, which has been done already in Sec. 3.4. So here we can focus on other problems which are peculiar to differential amplifiers only.

First of all, no differential amplifier is perfectly symmetrical, even if all of its transistors are on the same chip. The lack of a perfect symmetry causes the common mode input signal $(v_{i1} + v_{i2})/2$ to appear partly as a differential output signal. For the

same reason there is still some temperature drift, although greatly reduced in comparison with the single ended amplifier. The appearance of common mode signals at the output is especially annoying in electrobiological amplifiers (electrocardiographs and electroencephalographs). In these amplifiers, very small input signal differences (of the order of several μV) must be amplified in the presence of large (up to 1V) common mode signals from power lines, owing to capacitive pickup. The level of ability of the differential amplifier to reject the common mode signal is called *common mode rejection ratio*, $\mathrm{CMRR} = A_{\mathrm{vc}}/A_{\mathrm{vd}}$, generally expressed in decibels (dB). Since this is out of scope of this book, we shall not pursue these effects in detail.

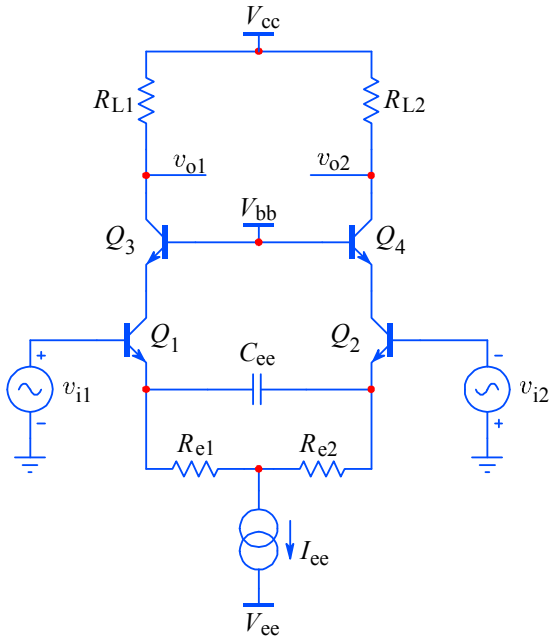

Fig. 3.7.2: The basic circuit of the differential cascode amplifier.

The optimum thermal stability of the differential cascode circuit could again be obtained by adjusting the quiescent currents in both halves of the differential amplifier to values such that the voltage drop on each loading resistor is equal to the voltage $(V_{\mathrm{cc}} - V_{\mathrm{bb}} - V_{\mathrm{be}})/2$, (see Eq. 3.4.19 and the corresponding explanation). However, as has been said for the simple cascode amplifier, the requirements for large bandwidth will prevent this from being realized. We would want to have low R_{L}, high V_{cc} and V_{bb}, and high I_{ee} to maximize the bandwidth. So the thermal stability will have to be established in a different way.

Differential amplifiers are particularly suitable for compensation of many otherwise insolvable errors. This is achieved by cross-coupling and adding anti-phase signals, so that the errors cancel. For example, the pre-shoot of the simple cascode amplifier, which is owed to capacitive feed through, can be effectively eliminated if two capacitors with the same value as $C_{\mu 1,2}$ are connected from the Q_1 emitter to the Q_2 collector, and vice-versa.

Similarly, by cross-coupling diodes or transistors we can achieve nonlinearity cancellation, leakage current compensation, better gain stability, DC stability, etc. In integrated circuits, even production process variations can be compensated in this way. Some such examples are given in Part 5.

3.7.2 Current source in the emitter circuit

To improve the common mode rejection, instead of having a large resistor R_{ee} and a correspondingly high voltage V_{ee} (resulting in an unnecessarily high power dissipation $P \approx V_{ee}^2/R_{ee}$) the common practice is to use high *incremental* resistance. This is usually done by a special connection of active devices in a configuration called *current source*. Such generators can have a high incremental resistance even when working with a relatively low V_{ee}.

The ideal current generator should be independent as much as possible from the applied voltage and from ambient temperature. A simple current sink, composed of two equal transistors Q_5 and Q_6 is shown in Fig. 3.7.3a. (We have given them the indices '5' and '6' in order to avoid any confusion with the former figures). The circuit is named the *current mirror* [Ref. 3.31], because the collector current I_{c6} is in some respect a 'mirror image' of I_R, as shown in Fig. 3.7.3b, where the current symmetry analysis is performed by normalizing the currents to those of the base. Current mirrors are in widespread use in integrated circuits in which complex multi-stage biassing is controlled from a single point.

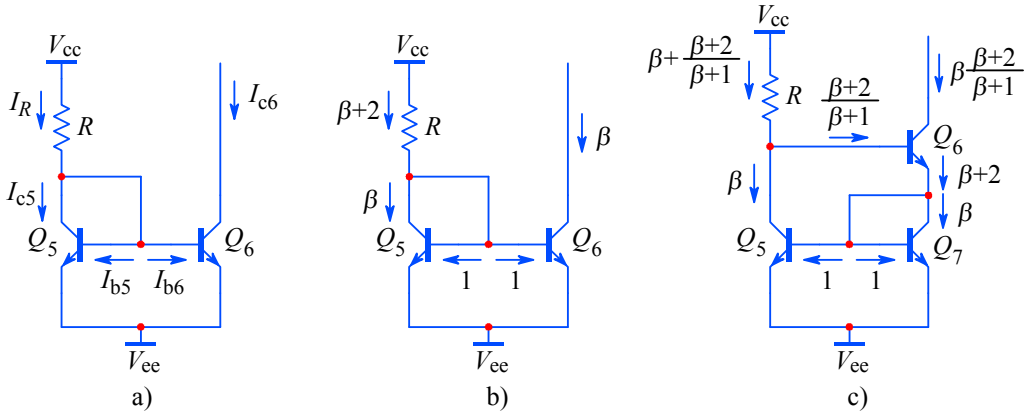

Fig. 3.7.3: a) The basic current mirror. b) Current symmetry analysis with the currents normalized to those of the base. c) The symmetry is improved in the Wilson mirror.

The current I_R is:

$$I_R = I_{c5} + I_{b5} + I_{b6} = I_{c5} + \frac{I_{c5}}{\beta_5} + \frac{I_{c6}}{\beta_6} \tag{3.7.4}$$

If both transistors are identical, then $\beta_5 = \beta_6 = \beta$ and $I_{c5} = I_{c6} = \beta I_b$. In this case:

$$I_R = I_{c5}\left(1 + \frac{2}{\beta}\right) \tag{3.7.5}$$

and the collector current is:

$$I_{c5} = \frac{I_R}{1 + \dfrac{2}{\beta}} \tag{3.7.6}$$

If β is very large then:

$$I_{c6} \approx I_R = \frac{V_{cc} - V_{be}}{R} \tag{3.7.7}$$

In general the collector current of a transistor is [Ref. 3.4]:

$$I_c = I_s \, e^{\frac{V_{be}}{V_T}} \left(1 + \frac{V_{ce}}{V_A + V_{ce}}\right) \tag{3.7.8}$$

where:

I_s = the collector saturation current (approx. 10^{-12} to 10^{-14} A);

V_A = Early voltage (usually between 100 and 150 V, see Fig. 3.4.11);

$V_T = k_B T/q$ (as defined at the beginning of Sec. 3.1).

Eq. 3.7.8 can be written simply from the geometric relations taken from Fig. 3.4.11. For a common silicon transistor the Early voltage is at least 100 V. Suppose both silicon transistors in Fig. 3.7.3a are identical and subject to the same temperature variations (on the same chip). The collector–emitter voltage of transistor Q_5 is the same as the base–emitter voltage, $V_{ce5} = V_{be5} \approx 0.65\,\text{V}$. In contrast, the collector–emitter voltage of transistor Q_6 is higher, say, $V_{ce6} = 15\,\text{V}$. The ratio of both collector currents is then:

$$\frac{I_{c6}}{I_{c5}} = \frac{1 + \dfrac{V_{ce6}}{V_A + V_{ce6}}}{1 + \dfrac{V_{ce5}}{V_A + V_{ce5}}} = \frac{1 + \dfrac{15}{100 + 15}}{1 + \dfrac{0.6}{100 + 0.6}} = 1.237 \tag{3.7.9}$$

By using more sophisticated circuits it is possible to make either $I_{c5} = I_{c6}$ or $I_R = I_{c6}$, or even to make any desired ratio between any of them [Ref. 3.31, 3.32, 3.33]. This is important in order to decrease the power dissipation in the resistor R. The power dissipated by Q_6 will then be the product of the desired current and the collector–emitter voltage set by the desired common mode range of the differential amplifier.

Since we are interested in wideband aspects of differential amplifiers, we shall not discuss further particularities here. However, current mirrors can also be used to convert the output signal of the differential amplifier into a single ended push pull drive, as is often done in modern operational amplifiers, and we shall return to this subject later in Part 5, with a discussion of the *Wilson* mirror [Ref. 3.32], Fig. 3.7.3c.

Before closing the analysis of current sinks, let us calculate the incremental collector resistance r_o of transistor Q_6, which can be derived simply from Fig. 3.4.11:

$$r_o = \frac{\Delta V_{ce6}}{\Delta I_{c6}} = \frac{V_A + V_{ce6}}{I_{c6}} \tag{3.7.10}$$

Returning to our differential amplifier example of Fig. 3.7.2 with $V_{ee} = -15\,\text{V}$, suppose we require a differential amplifier current $I_{ee} = I_{e1} + I_{e2} = I_{c6} = 0.03\,\text{A}$. By assuming the Early voltage $V_A = 135\,\text{V}$ and $V_{ce6} \approx V_{ee}$, the incremental collector resistance is:

$$r_o = \frac{135 + 15}{0.03} = 5\,\text{k}\Omega \tag{3.7.11}$$

If we were to replace the current generator by a simple resistor $R_{ee} = r_o$, the voltage V_{ee} in Fig. 3.7.2 would have to be:

$$(I_{e1} + I_{e3})\, R_{ee} = 0.03\,\text{A} \cdot 5000\,\Omega = 150\,\text{V} \tag{3.7.12}$$

which is 10 times more. Correspondingly, the power dissipation in the resistor R_{ee} would also be 10 times greater, or 4.5 W, compared to 0.45 W for Q_6.

A high incremental resistance r_o is also important for achieving high CMRR, because it gives the differential amplifier a higher immunity to power supply voltage variations (which is also a common mode signal).

A simple way of improving the current generator, thus achieving even greater CMRR factors, is shown in Fig. 3.7.4, where negative feedback, provided by the Q_5 gain, is used to stabilize the collector current of Q_6 and increase the incremental resistance, whilst a low voltage Zener diode (named after its inventor, the American physicist *Clarence M. Zener*, 1905-1993) reduces the V_{be} thermal drift of Q_5, owing to an almost equal, but opposite thermal coefficient.

In this circuit any increase in Q_6 collector current I_{c6} is sensed by its voltage drop on R_2, increasing V_{b5}, which in turn increases I_{e5}, thus reducing I_{b6} and therefore also I_{c6}. The reduction feedback factor is nearly equal to the Q_5 current gain β. Effectively, the output resistance is increased from r_o of Eq. 3.7.10 to about βr_o. Note that this circuit does not rely on identical transistor parameters, so it can be used in discrete circuits.

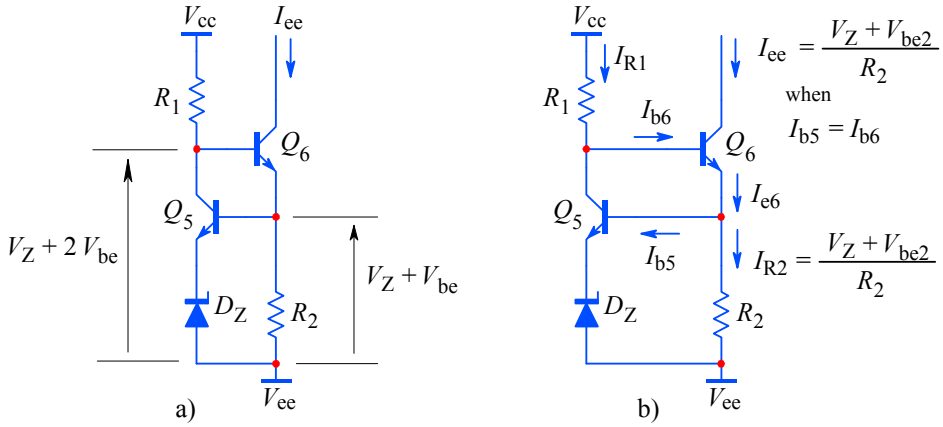

Fig. 3.7.4: Improved current generator: a) voltage drops; b) current analysis.

The circuits shown and only briefly discussed here should give the reader a starting point in current control design. Many more circuits, either simple or more elaborate, can be found in the references quoted.

3.8 The f_T Doubler

Let us return to the differential cascode amplifier of Fig. 3.7.2, where the basic analysis was done with the assumption that the inputs were driven by a differential voltage source. Here we shall analyze a current driven stage, which could suitably be used as an intermediate amplifier stage with the T-coil peaking at the input, such as the cascode of Fig. 3.6.1. The T-coil peaking has already been analyzed in detail, so we shall concentrate on the active part of the circuit and see how it can be improved.

In Fig. 3.8.1 we have the differential cascode circuit, driven differentially by the current source i_s. This current source is loaded by the resistance R_s which we have split in half and grounded its middle point. The output currents from the collectors of Q_3 and Q_4 drive the differential inputs of the next amplifying stage and we are not interested in it now. What we are interested in, is the current gain of this differential stage. The reader who has followed the previous analysis with some attention should by now be able to understand the following relation intuitively:

$$\frac{i_o}{i_s} \approx \frac{R_s}{R_e} \cdot \frac{1}{1 + s\left(R_s \frac{\tau_{T1}}{R_e} + \frac{R_s}{2} C_\mu\right)} \cdot \frac{1}{1 + s\,\tau_{T2}} \tag{3.8.1}$$

The last fraction is the frequency dependent part owed to $Q_{3,4}$.

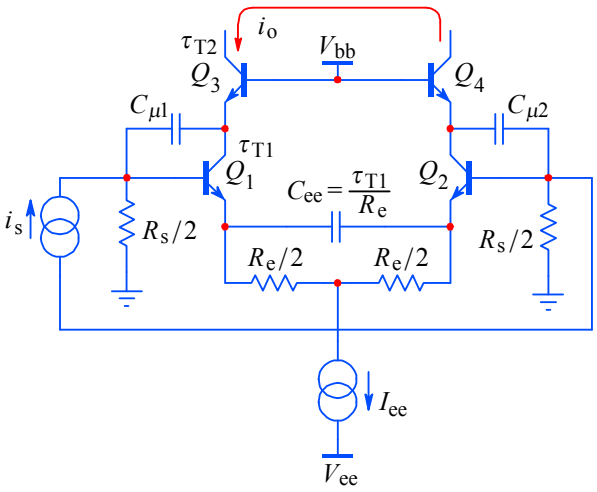

Fig. 3.8.1: The current driven differential cascode amplifier. We assume that the transistor pair $Q_{1,2}$, and the pair $Q_{3,4}$, respectively, have identical main parameters. The emitters of $Q_{1,2}$ see the R_eC_{ee} network, set to equal the time constant τ_{T1} of transistors $Q_{1,2}$.

The low frequency current gain is simply:

$$A_i = \frac{R_s}{R_e} \tag{3.8.2}$$

We can substitute this in Eq. 3.8.1 to highlight the bandwidth dependence on gain:

$$\frac{i_o}{i_s} \approx A_i \frac{1}{1 + s\left(A_i\,\tau_{T1} + A_i \frac{R_e\,C_\mu}{2}\right)} \cdot \frac{1}{1 + s\,\tau_{T2}} \tag{3.8.3}$$

This means that by reducing the gain A_i we can extend the bandwidth. On the basis of this there arises the idea that we can add another differential stage to double the current (and therefore also the current gain) and then optimize the stage, choosing between the doubling of gain with the same bandwidth and the doubling of bandwidth with the same gain, or any factor in between.

The basic f_T doubler circuit, developed by *C.R. Battjes*, [Ref. 3.1], is presented in Fig. 3.8.2. Each differential pair amplifies the voltage drop on its own $R_s/2$ and each pair sees its own R_e between the emitters, thus the current gain is simply:

$$\frac{i_o}{i_s} \approx \frac{R_s}{R_e} \cdot \frac{1}{1 + s\left(R_s \frac{\tau_{T1}}{2\,R_e} + \frac{R_s C_\mu}{2}\right)} \cdot \frac{1}{1 + s\,\tau_{T2}}$$

$$\approx A_i \frac{1}{1 + s\,A_i\left(\frac{\tau_{T1}}{2} + \frac{R_e\,C_\mu}{2}\right)} \cdot \frac{1}{1 + s\,\tau_{T2}} \qquad (3.8.4)$$

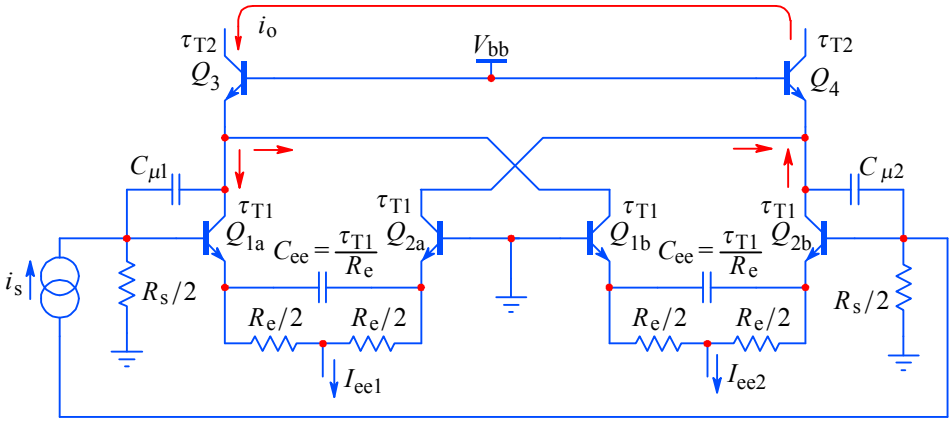

Fig. 3.8.2: The basic f_T doubler circuit. We assume equal transistors for $Q_{1a,2a}$ and $Q_{1b,2b}$. The low input impedance of $Q_{3,4}$ emitters allows summing the collector current of each pair, but cross-coupled for in phase signal summing.

Another advantage of this circuit is the reduced input capacitance:

$$C_i = \frac{2\,\tau_{T1}}{R_e} + C_\mu \qquad \text{for the circuit in Fig. 3.8.1} \qquad (3.8.5)$$

$$C_i = \frac{\tau_{T1}}{R_e} + C_\mu \qquad \text{for the circuit in Fig. 3.8.2} \qquad (3.8.6)$$

This will ease the application of T-coil peaking at the input.

But there are also limitations. As can be deduced from Eq. 3.8.4, the 'doubler' term in the circuit name is misleading, because the term with τ_{T2} is not influenced by the reduced gain. Therefore, the amount of bandwidth improvement depends on which time constant is larger. The part with $R_e C_\mu$ can be reduced by selecting transistors with low C_μ, but this we would do anyway. And we do not want to reduce R_e, because it would increase the gain (for same R_s).

Another problem is that, although the transfer function is of second order, there are two real poles, so we can not 'tune' the system for an efficient peaking. By forcing the system to have complex conjugate poles with emitter peaking, we would increase the emitter capacitance C_{ee}, which would be reflected into the base as an increased input capacitance; this would increase exactly that term which we have just halved.

A quick estimate will give us a little more feeling of the improvement achievable. Let us have a number of transistors, with $f_T = 3.5\,\text{GHz}$, $C_\mu = 1\,\text{pF}$, $R_s = 2 \times 50\,\Omega$, $Q_{3,4}$ collector load $R_L = 2 \times 50\,\Omega$, $C_L = 1\,\text{pF}$ and the total current gain $A_i = 3$. Assuming that the system's response is governed by a dominant pole, we can calculate the rise time of the conventional system as:

$$t_r = 2.2\sqrt{A_i^2\left(\frac{1}{2\pi f_T} + \frac{R_e C_\mu}{2}\right)^2 + \left(\frac{1}{2\pi f_T}\right)^2 + [R_L(C_L + C_\mu)]^2} \tag{3.8.7}$$

Then, for the ordinary differential cascode in Fig. 3.8.1:

$$t_{r1} = 476\,\text{ps} \tag{3.8.8}$$

whilst for the f_T doubler we have:

$$t_{r2} = 355\,\text{ps} \tag{3.8.9}$$

and the improvement factor is 1.34, much less than 2. Transistors with lower f_T might give an apparently greater improvement (about 1.7 could be expected) owing to the lower contribution of the source's impedance. However, it seems that a better idea would be to remain with the original bandwidth and use the gain doubling instead, which could lead to a system with a lower number of stages, which in turn could be optimized more easily.

On the other hand, the reduced input capacitance is really beneficial to the loading of the input T-coils. With the data from the example above, we can calculate the T-coils for the conventional and the doubler system and the resulting bandwidths. From Eq. 3.6.21 we can find that:

$$\omega_H = \sqrt{\frac{12}{(R_L C_i)^2}\left(1 + \frac{r_b}{R_L}\right)} \tag{3.8.10}$$

By assuming an $r_b = 15\,\Omega$ and C_i of 6.5 and 3.7 pF, respectively (Eq. 3.8.5 and 3.8.6), we can calculate an f_H of 1.9 and 3.4 GHz, a ratio of nearly 1.8, which is worth considering.

In principle one could use the same doubler implementation with 4, 6, or more transistor pairs; however, the input capacitance poses a practical limit. A system with 4 pairs is already slower than the system with two pairs.

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3.9 JFET Source Follower

Wideband signals come usually from two source types: low impedance sources are usually those from the output of other wideband amplifiers, while medium and high impedance sources are usually those from sensors or other very low power sources.

In the first case, we employ standardized impedances, 50 Ω or 75 Ω, so that both the source and the load have the same impedance as the characteristic impedance of the cable that connects them. In this way we preserve the bandwidth and prevent reflections which would distort the signal, but we pay for this by the 50 % (−6 dB) attenuation of the signal's amplitude.

In the second case we also want a standardized value of the impedance, but this time the value is 1 MΩ, in parallel with some (inevitable) capacitance, usually 20 pF (but values from 10 to 25 pF can also be found). The standardized capacitance is helpful not only in determining the loading of the source at high frequencies, but also to allow the use of 'probes', which are actually special HF attenuators (÷10 or ÷100), so that the source can be loaded by a 10 MΩ or even a 100 MΩ resistance, while keeping the loading capacitance below some 12 pF.

With the improvement of semiconductor production processes, the so called 'active' probes have been developed, used mostly for extremely wideband signals, such as those found in modern communications and digital computers. Active probes usually have a 10 kΩ || 2 pF input impedances, with no reduction in amplitude.

The key component of both high input impedance amplifiers and active probes is the JFET (*junction field effect transistor*) source follower [Ref. 3.16].

The basic JFET source follower circuit configuration is shown in Fig. 3.9.1. In contrast to the BJT emitter follower (with an input resistance of about βR_e), the JFET source follower has a very high input resistance (between 10^9 and 10^{12} Ω), owed to the specific construction of the JFET. Its gate (a p–n junction with the drain–source channel) is reverse biased in normal operation, modulating the channel width by the electrical field only, so the input current is mainly owed to the reverse biased p–n junction leakage and the input capacitances, C_{gd} and C_{gs}.

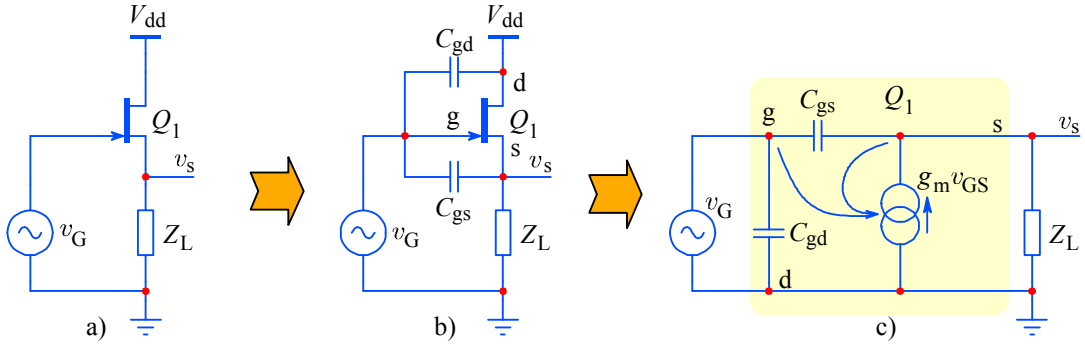

Fig. 3.9.1: The JFET source follower: a) circuit schematic; b) the same circuit, but with an ideal JFET and the inter-electrode capacitances drawn as external components; c) equivalent circuit.

A MOSFET (*metal oxide silicon field effect transistor*) has even greater input resistance (up to ~10^{15} Ω); however it also has a greater input capacitance (between 20

and 200 pF; it is also more noisy and more sensitive to damage by being overdriven), so it is not suitable for a wideband amplifier input stage.

In Fig. 3.9.1b we have drawn an ideal JFET device and its inter-electrode capacitances are modeled as external components. These capacitances determine the response at high frequencies [Ref. 3.8, 3.16, 3.20, 3.35]. Fig. 3.9.1c shows the equivalent circuit.

The source follower is actually the common drain circuit with a voltage gain of nearly unity, as the name 'follower' implies. The meaning of the circuit components is:

C_{gd} gate–drain capacitance; in most manufacturer data sheet it is labeled as C_{rss} (*common source circuit reverse capacitance*); values usually range between 1 and 5 pF;

C_{gs} gate–source capacitance; in their data sheet, manufacturers usually report the value of C_{iss}, the *common source total input capacitance*, therefore we obtain $C_{gs} \approx C_{iss} - C_{rss}$; values of C_{gs} usually range from 3 to 15 pF;

g_m JFET transconductance; usual values range between 1 000 and 15 000 µS (in some data-sheets, the symbol 'mho' is used to express that the unit *siemens* $[S] = [1/\Omega]$);

Z_L the loading impedance of the JFET source.

The JFET drain is connected to the power supply which must be a short circuit for the drain signal current, therefore we can connect C_{gd} to ground, in parallel with the signal source. We assume the signal source impedance to be zero; so we can forget about C_{gd} for a while.

From the equivalent circuit in Fig. 3.91c we find the currents for the node g:

$$i_g = v_G\, s\, C_{gd} + (v_G - v_s)\, s\, C_{gs} \tag{3.9.1}$$

and the currents for the node s:

$$(v_G - v_s)\, s\, C_{gs} + (v_G - v_s)\, g_m = \frac{v_s}{Z_L} \tag{3.9.2}$$

which can be rewritten as:

$$v_G \left(1 + \frac{g_m}{s\, C_{gs}}\right) = v_s \left(1 + \frac{g_m}{s\, C_{gs}} + \frac{1}{s\, C_{gs} Z_L}\right) \tag{3.9.3}$$

From this we obtain the system's voltage gain:

$$A_v = \frac{v_s}{v_G} = \frac{Z_L \left(1 + \dfrac{s\, C_{gs}}{g_m}\right)}{Z_L \left(1 + \dfrac{s\, C_{gs}}{g_m}\right) + \dfrac{1}{g_m}} \tag{3.9.4}$$

In practical follower circuits we want to make the output signal's dynamic range as high and the voltage gain as close to 1 as possible. The simplest way to achieve this is by replacing Z_L with a constant current generator, Fig. 3.9.2, much as we have done in

the differential amplifier. By doing this, we increase the real (resistive) part of the loading impedance, but we can do little to reduce the always present loading capacitance C_L.

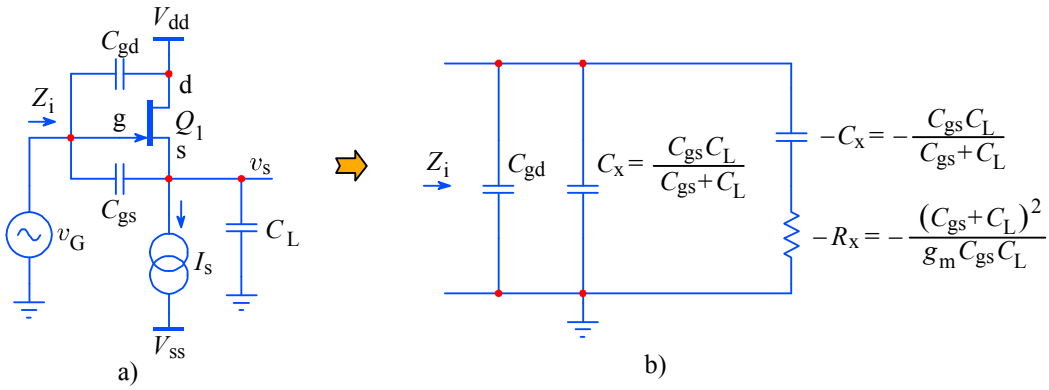

Fig. 3.9.2: The JFET source follower biased by a current generator and loaded only by the inevitable stray capacitance C_L: a) circuit schematic; b) the input impedance has two **negative** components, owed to C_{gs} and g_m (see Sec. 3.9.5).

In Eq. 3.9.4 the term C_{gs}/g_m is obviously the characteristic JFET time constant, τ_{FET}:

$$\frac{C_{gs}}{g_m} = \tau_{FET} = \frac{1}{\omega_{FET}} \tag{3.9.5}$$

Since we now have $Z_L = 1/j\omega C_L$ we can rewrite Eq. 3.9.4 as:

$$A_v = \frac{v_s}{v_G} = \frac{1 + \dfrac{j\omega}{\omega_{FET}}}{1 + j\omega\left(\dfrac{1}{\omega_{FET}} + \dfrac{C_L}{g_m}\right)} \tag{3.9.6.}$$

and by replacing g_m with $\omega_{FET}\, C_{gs}$ (Eq. 3.9.5) we obtain:

$$\frac{v_s}{v_G} = \frac{1 + \dfrac{j\omega}{\omega_{FET}}}{1 + \dfrac{j\omega}{\omega_{FET}} \cdot \dfrac{1}{D_c}} \tag{3.9.7.}$$

Here D_c is the input to output capacitive divider, which would set the output voltage if only the capacitances were in place:

$$D_c = \frac{C_{gs}}{C_{gs} + C_L} \tag{3.9.8.}$$

We would like to express Eq. 3.9.7 by its pole s_1 and zero s_2, so we need the normalized canonical form:

$$F(s) = A_0 \frac{-s_1}{s - s_1} \cdot \frac{s - s_2}{-s_2} \tag{3.9.9}$$

Therefore we replace $j\omega$ with s, multiply both the numerator and the denominator by $\omega_{\text{FET}}\, D_{\text{c}}$ and obtain:

$$F(s) = D_{\text{c}} \frac{s - (-\omega_{\text{FET}})}{s - (-\omega_{\text{FET}}\, D_{\text{c}})} \tag{3.9.10}$$

At zero frequency, the transfer function gain is:

$$A_0 = F(0) = D_{\text{c}} \frac{\omega_{\text{FET}}}{\omega_{\text{FET}}\, D_{\text{c}}} = 1 \tag{3.9.11}$$

so the zero is:

$$s_2 = -\omega_{\text{FET}} \tag{3.9.12}$$

and the pole is:

$$s_1 = -\omega_{\text{FET}}\, D_{\text{c}} \tag{3.9.13}$$

These simple relations are the basis from which we shall calculate the frequency response magnitude, the phase, the group delay and the step response of the JFET source follower (simplified at first and including the neglected components later).

3.9.1 Frequency response magnitude

The frequency response magnitude is the normalized absolute value of $F(s)$ and we want to have the normalization in both gain and frequency. Eq. 3.9.7 is already normalized in frequency (to ω_{FET}) and the gain $A_0 = 1$. To get the magnitude, we must multiply $F(j\omega)$ by its complex conjugate, $F(-j\omega)$ and take the square root:

$$|F(\omega)| = \sqrt{F(j\omega)\, F(-j\omega)} = \sqrt{\frac{1 + \dfrac{j\omega}{\omega_{\text{FET}}}}{1 + \dfrac{j\omega}{\omega_{\text{FET}}} \cdot \dfrac{1}{D_{\text{c}}}} \cdot \frac{1 - \dfrac{j\omega}{\omega_{\text{FET}}}}{1 - \dfrac{j\omega}{\omega_{\text{FET}}} \cdot \dfrac{1}{D_{\text{c}}}}}$$

$$|F(\omega)| = \sqrt{\frac{1 + \left(\dfrac{\omega}{\omega_{\text{FET}}}\right)^2}{1 + \left(\dfrac{\omega}{\omega_{\text{FET}}\, D_{\text{c}}}\right)^2}} \tag{3.9.14}$$

Since we want to examine the influence of loading we shall plot the transfer function for three different values of the ratio $C_{\text{L}}/C_{\text{gs}}$: 0.5, 1.0, and 2.0 (the corresponding values of D_{c} being 0.67, 0.5, and 0.33, respectively). The plots, shown in Fig. 3.9.3, have three distinct frequency regions: in the lower one, the circuit behaves as a voltage follower, with the JFET playing an active role, so that $v_{\text{s}} = v_{\text{G}}$, whilst in the highest frequency region, only the capacitances are important; in between we have a transition between both operating modes.

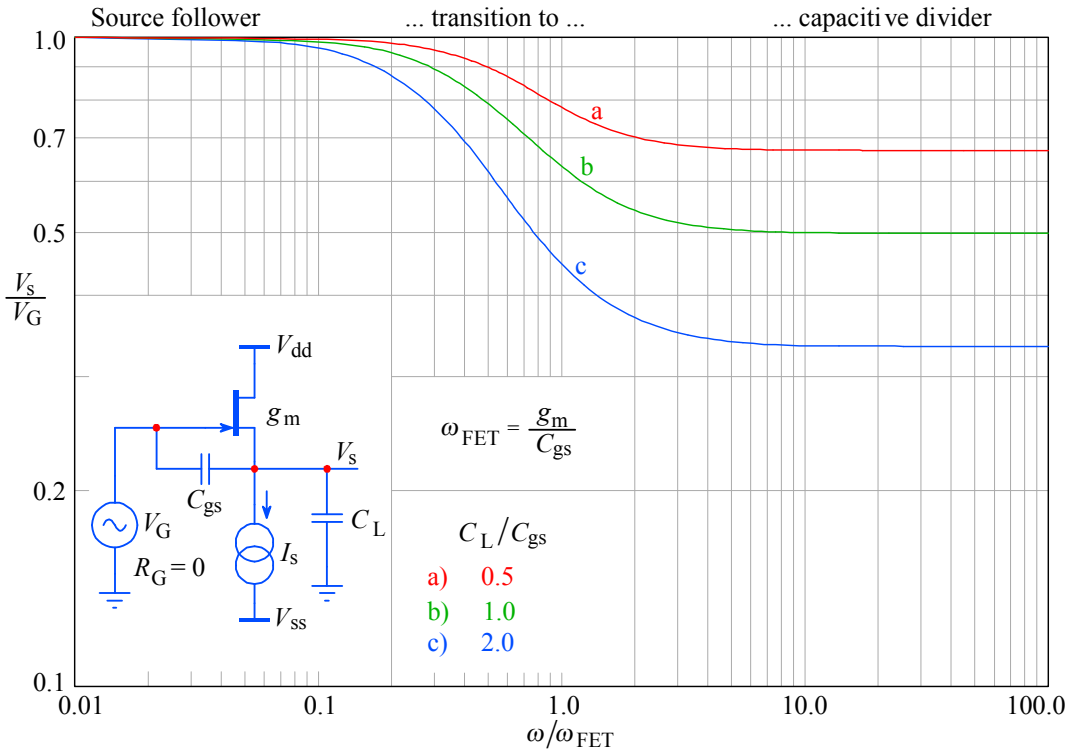

Fig. 3.9.3: Magnitude of the frequency response of the JFET source follower for three different capacitance ratios C_L/C_{gs}. The pole $s_3 = -1/R_G C_i$ has not been taken into account here (see Fig. 3.9.7 and Fig. 3.9.8).

The relation for the upper cutoff frequency is very interesting. If we set $|F(\omega)|$ to be equal to:

$$\sqrt{\frac{1+(\omega_h/\omega_{FET})^2}{1+(\omega_h/\omega_{FET}\,D_c)^2}} = \frac{1}{\sqrt{2}} \tag{3.9.15}$$

it follows that:

$$\omega_h = \omega_{FET}\,\frac{D_c}{\sqrt{1-2\,D_c^2}} \tag{3.9.16}$$

From Eq. 3.9.15 we can conclude that by putting $D_c = 1/\sqrt{2}$ the denominator is reduced to zero, thus $\omega_h = \infty$. This means that for such a capacitive ratio the magnitude never falls below $1/\sqrt{2}$. However attractive the possibility of achieving infinite bandwidth may seem, this can never be realized in practice, because any signal source will have some, although small, internal resistance R_G, resulting in an additional input pole $s_3 = -1/R_G C_i$, where C_i is the total input capacitance of the JFET. The complete transfer function will now be (see Fig. 3.9.7 and 3.9.8):

$$F(s) = \frac{s_1 s_3}{-s_2} \cdot \frac{s-s_2}{(s-s_1)(s-s_3)} \tag{3.9.17}$$

3.9.2 Phase

We obtain the phase response from Eq. 3.9.7 by taking the arctangent of the ratio of the imaginary to the real part of $F(j\omega)$:

$$\varphi(\omega) = \arctan \frac{\Im\{F(j\omega)\}}{\Re\{F(j\omega)\}} \tag{3.9.18}$$

Since in Eq. 3.9.7 we have a single real pole an a single real zero, the resulting phase angle is calculated as:

$$\varphi(\omega) = \arctan \frac{\omega}{\omega_{\mathrm{FET}}} - \arctan \frac{\omega}{\omega_{\mathrm{FET}}\, \mathrm{D_c}} \tag{3.9.19}$$

In Fig. 3.9.4 the three phase plots with same C_L/C_{gs} ratios are shown. Because of the zero, the phase returns to the initial value at high frequencies.

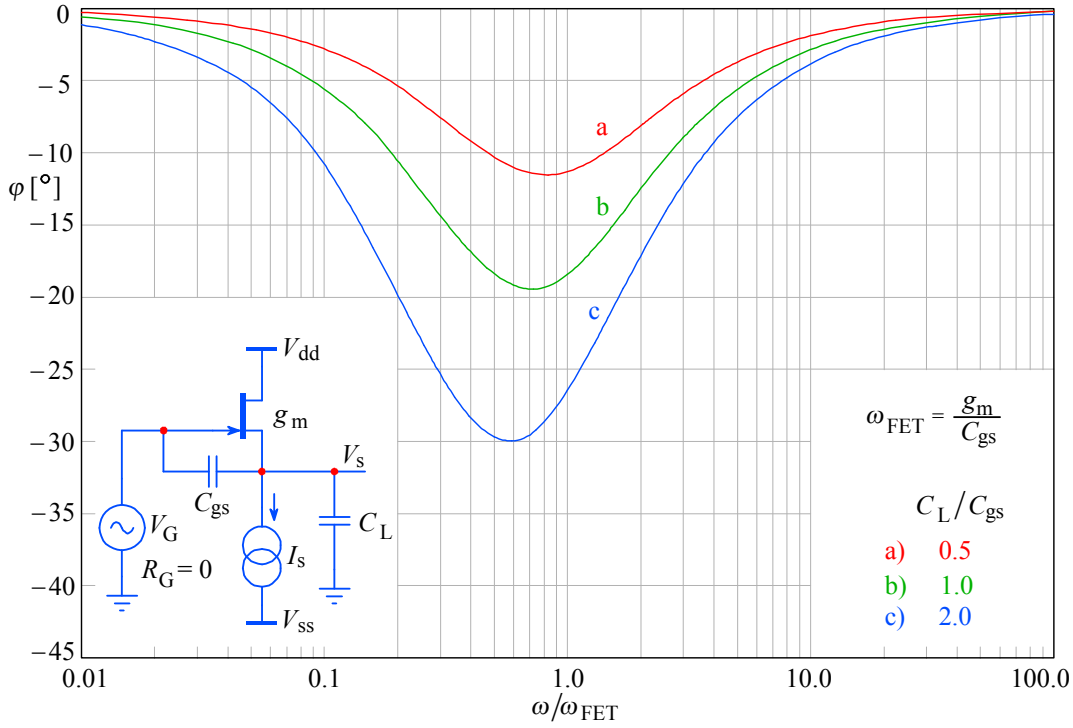

Fig. 3.9.4: Phase plots of the JFET source follower for the same three capacitance ratios.

3.9.3 Envelope delay

We obtain the envelope delay by taking the ω derivative of the phase:

$$\tau_e = \frac{d\varphi}{d\omega} \tag{3.9.20}$$

but we usually prefer the normalized expression $\tau_e\, \omega_h$. In our case, however, the upper cut off frequency, ω_h, is changing with the capacitance divider D_c. So instead of ω_h we

shall, rather, normalize the envelope delay to the characteristic frequency of the JFET itself, ω_{FET}:

$$\tau_e\,\omega_{FET} = \frac{1}{1+(\omega/\omega_{FET})^2} - \frac{D_c}{D_c^2+(\omega/\omega_{FET})^2} \tag{3.5.21}$$

The envelope delay plots for the three capacitance ratios are shown in Fig. 3.9.5. Note that for all three ratios there is a frequency region in which the envelope delay becomes **positive**, implying that the output signal advance, in correlation with the phase plots, goes up with frequency. We have explained the physical background of this behavior in Part 2, Fig. 2.2.5, 2.2.6. The positive envelope delay influences the input impedance in a very unfavorable way, as we shall soon see.

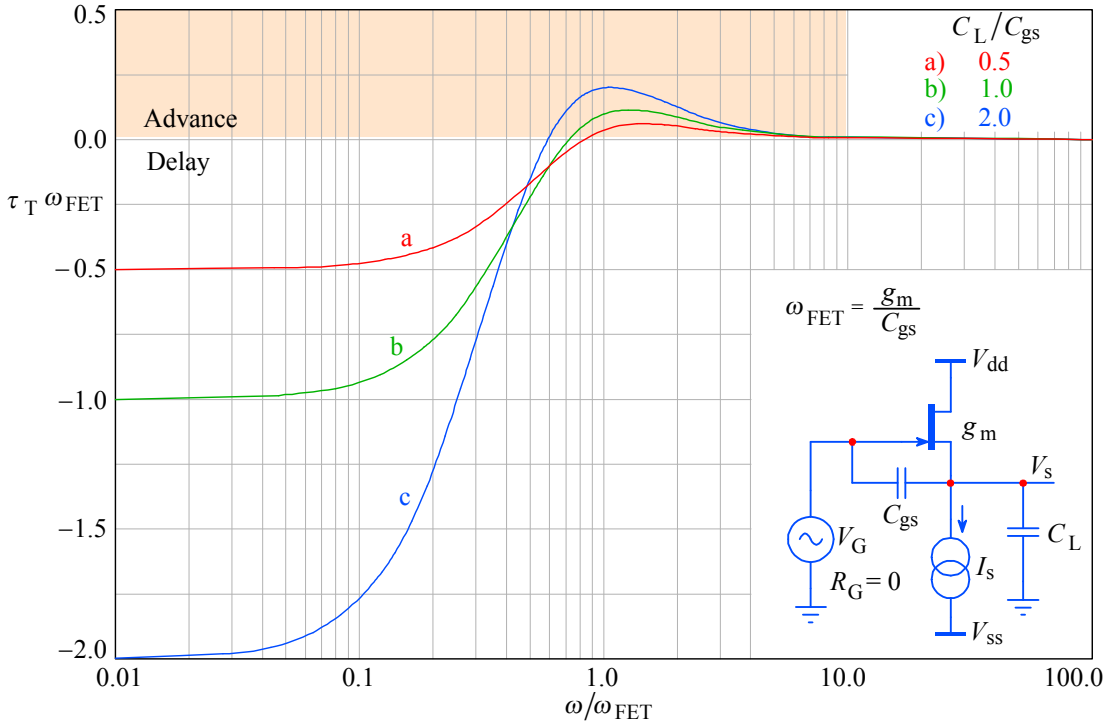

Fig. 3.9.5: The JFET envelope delay for the three capacitance ratios. Note the positive peak (phase advance region): trouble in sight!

3.9.4 Step response

We are going to use Eq. 3.9.9, which we multiply by the unit step operator $1/s$ to obtain the step response in the complex frequency domain; we then obtain the time domain response by applying the inverse Laplace transform:

$$G(s) = \frac{1}{s}\,F(s) = \frac{1}{s}\,D_c\,\frac{s-s_2}{s-s_1} \tag{3.9.22}$$

$$g(t) = \mathcal{L}^{-1}\{G(s)\} = D_c \sum_{s=0}^{s_1} \operatorname{res} \frac{(s-s_2)\,e^{st}}{s\,(s-s_1)} \tag{3.9.23}$$

The residue at $s \to 0$ is:

$$\text{res}_0 = \lim_{s \to 0} s \frac{(s - s_2)\, e^{st}}{s\,(s - s_1)} = \frac{s_2}{s_1} \tag{3.9.24}$$

and the residue at $s \to s_1$ is:

$$\text{res}_1 = \lim_{s \to s_1} (s - s_1) \frac{(s - s_2)\, e^{st}}{s\,(s - s_1)} = \frac{s_1 - s_2}{s_1}\, e^{s_1 t} \tag{3.9.25}$$

By entering both residues back into Eq. 3.9.23 we get:

$$g(t) = D_c \left(\frac{s_2}{s_1} + \frac{s_1 - s_2}{s_1}\, e^{s_1 t} \right) \tag{3.9.26}$$

and, by considering Eq. 3.9.12 and 3.9.13, as well as that $\omega_{FET} = 1/\tau_{FET}$ and using the normalized time t/τ_{FET}, we end up with:

$$g(t) = 1 - (1 - D_c)\, e^{-D_c t/\tau_{FET}} \tag{3.9.27}$$

The plot of this relation is shown in Fig. 3.9.6, again for the same three capacitance ratios. The initial output signal jump at $t = 0$ is the input signal cross-talk (through C_{gs}) multiplied by the D_c factor:

$$g(0) = D_c \tag{3.9.28}$$

Following the jump is the exponential relaxation towards the normal follower action at lower frequencies. If the input pole $s_3 = -1/R_G C_i$ is taken into account, the jump would be slowed down to an exponential rise with a time constant of $R_G C_i$.

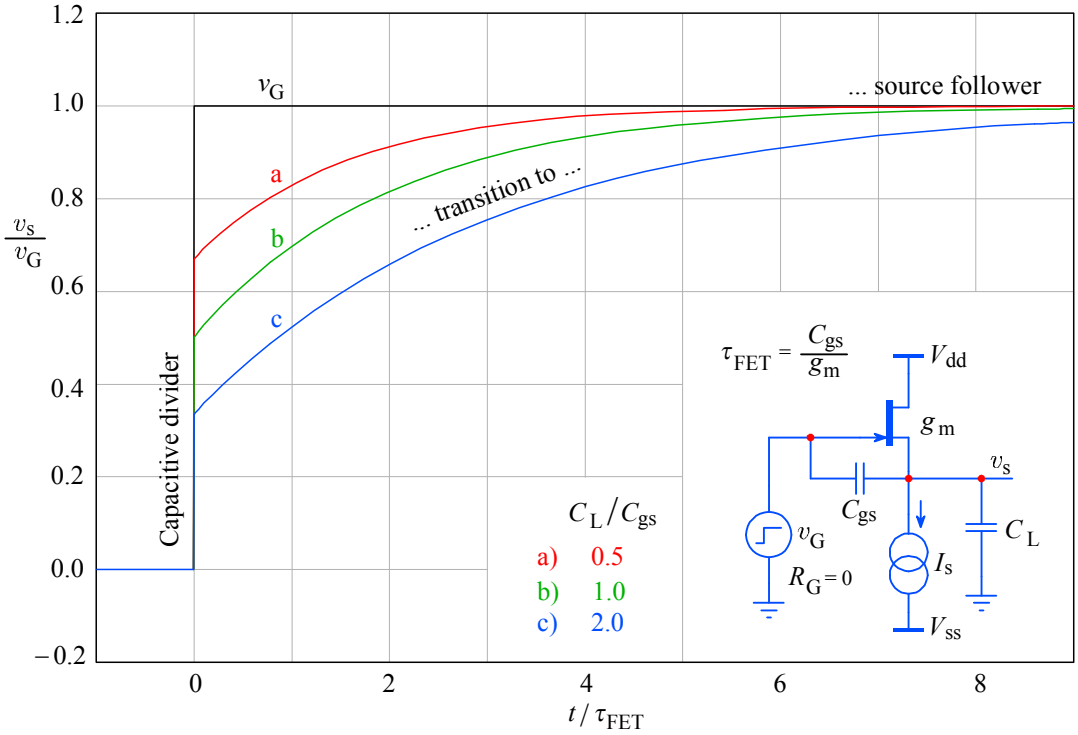

Fig. 3.9.6: The JFET source follower step response for the three capacitance ratios.

As mentioned earlier in connection with Eq. 3.9.17, when the value of R_G is comparable to $1/g_m$, an additional pole has to be to considered. We must derive the system transfer function again, from the following two equations:

For the currents into the node g:

$$\frac{v_G - v_g}{R_G} = \frac{v_g}{\frac{1}{s\,C_{gd}}} + \frac{v_g - v_s}{\frac{1}{s\,C_{gs}}} \tag{3.9.29}$$

and for the currents into the node s:

$$\frac{v_g - v_s}{\frac{1}{s\,C_{gs}}} + (v_g - v_s)\,g_m = \frac{v_s}{\frac{1}{s\,C_L}} \tag{3.9.30}$$

We first express v_g as a function of v_s from Eq. 3.9.30:

$$v_g = v_s\left(1 + \frac{s\,C_L}{s\,C_{gs} + g_m}\right) \tag{3.9.31}$$

Then we replace v_g in Eq. 3.9.29 by 3.9.31:

$$v_G = v_s\left(1 + \frac{s\,C_L}{s\,C_{gs} + g_m}\right)(1 + R_G\,s\,C_{gd} + R_G\,s\,C_{gs}) - v_s R_G\,s\,C_{gs} \tag{3.9.32}$$

After some further manipulation we arrive at:

$$\frac{v_s}{v_G} = \frac{1}{1 + R_G\,s\,C_{gd} + \frac{s\,C_L}{s\,C_{gs} + g_m}(1 + R_G\,s\,(C_{gd} + C_{gs}))} \tag{3.9.33}$$

Now we put this into the normalized canonical form and use Eq. 3.9.5 again to replace the term g_m/C_{gs} with ω_{FET}. Also, we express all the time constants as functions of ω_{FET} and the appropriate capacitance ratios. Finally, we want to see how the response depends on the product $g_m R_G$, so we multiply all the terms containing R_G with g_m and compensate each of them accordingly. The final expression is:

$$\frac{v_s}{v_G} = \frac{(s + \omega_{FET})\frac{1}{g_m R_G} \cdot \frac{\omega_{FET}\,\frac{C_{gs}}{C_{gd}}}{\left(1 + \frac{C_L}{C_{gs}} + \frac{C_L}{C_{gd}}\right)}}{s^2 + s\,\frac{\omega_{FET}\left[1 + \frac{1}{g_m R_G}\left(\frac{C_{gs}}{C_{gd}} + \frac{C_L}{C_{gd}}\right)\right]}{\left(1 + \frac{C_L}{C_{gs}} + \frac{C_L}{C_{gd}}\right)} + \frac{1}{g_m R_G} \cdot \frac{\omega_{FET}^2\,\frac{C_{gs}}{C_{gd}}}{\left(1 + \frac{C_L}{C_{gs}} + \frac{C_L}{C_{gd}}\right)}} \tag{3.9.34}$$

To plot the responses we shall set:

$$\frac{C_L}{C_{gs}} = 1, \qquad \frac{C_{gs}}{C_{gd}} = 5, \qquad \omega_{FET} = 1, \qquad s = j\omega, \qquad \text{and} \qquad g_m R_G = [0.3,\ 1,\ 3]$$

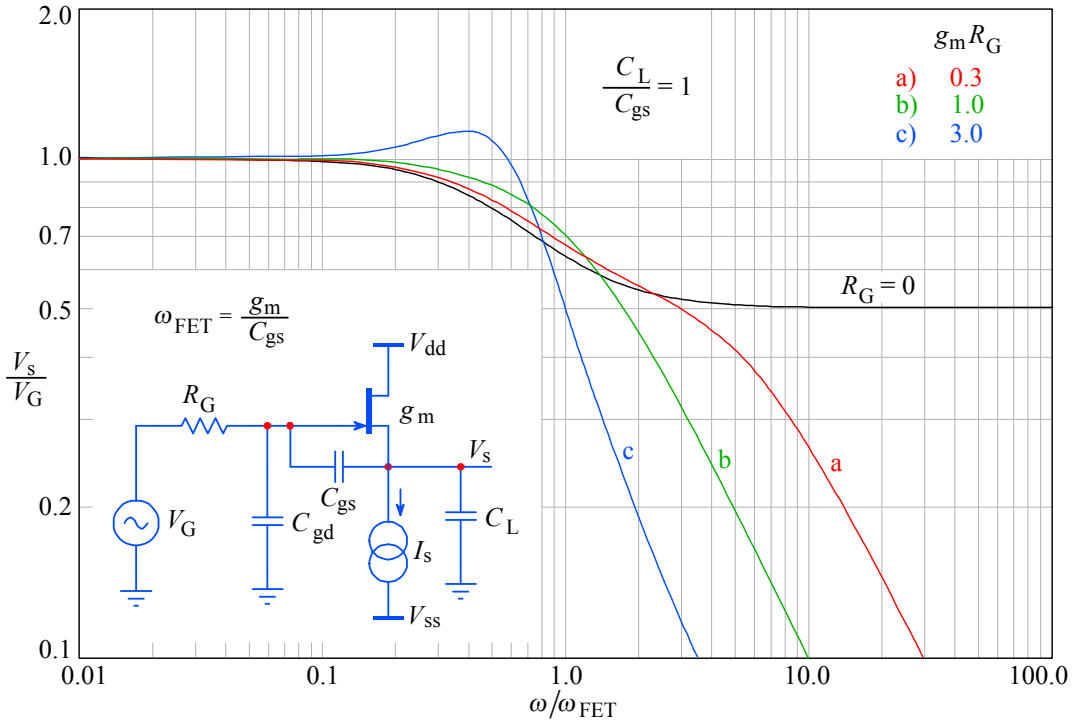

Fig. 3.9.7: The JFET source follower frequency response for a ratio $C_L/C_{gs} = 1$ and a variable signal source impedance, so that $R_G g_m$ is 0.3, 1, and 3, respectively. Note the response peaking for $g_m R_G = 3$.

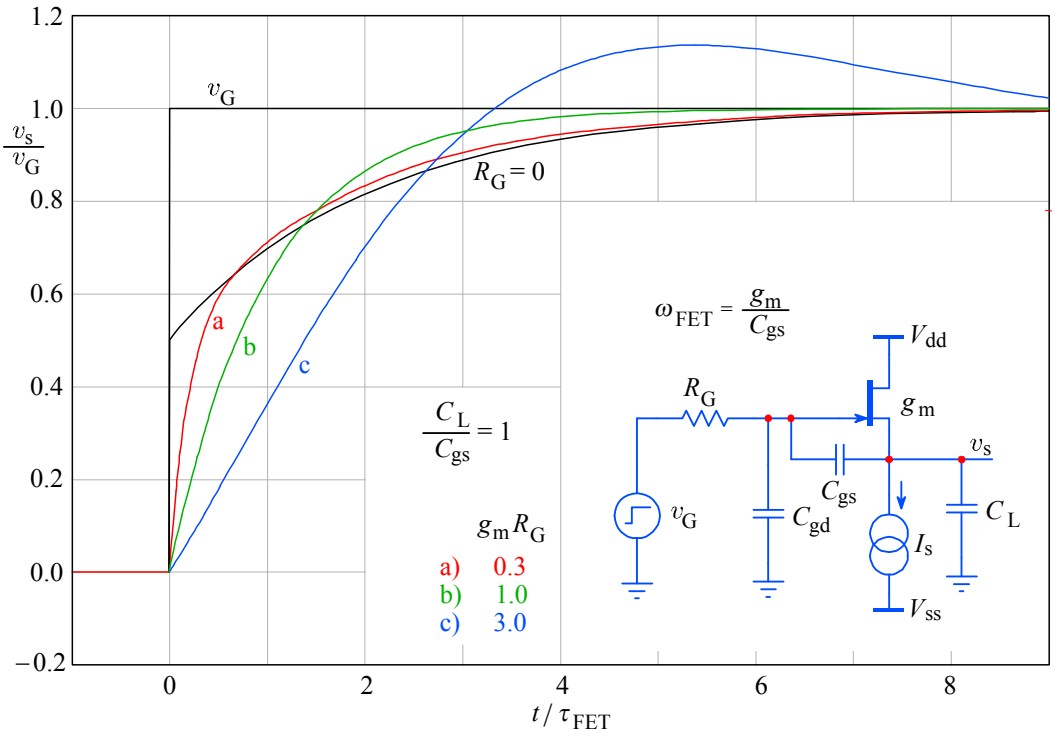

Fig. 3.9.8: The JFET source follower step response for the same conditions as in Fig. 3.9.7.

3.9.5 Input impedance

In Fig. 3.9.7 and 3.9.8 we have seen how the JFET source follower response is affected by its input impedance; this behavior becomes evident when the signal source has a non-zero resistance. Here, we are going to explore the circuit in more depth to examine the influence of a complex and, in particular, inductive signal source.

As we have done in the previous analysis, the gate–drain capacitance C_{gd} will appear in parallel with the input, so we can treat its admittance separately and concentrate on the remaining input components.

We start from Eq. 3.9.1 by solving it for v_s:

$$v_s = v_G - \frac{i_i}{s\,C_{gs}} \tag{3.9.35}$$

This we insert into Eq. 3.9.2:

$$-v_G\,(s\,C_{gs} + g_m) + \left(v_g - \frac{i_i}{s\,C_{gs}}\right)\left(s\,C_{gs} + g_m + \frac{1}{Z_L}\right) = 0 \tag{3.9.36}$$

Because the JFET source is biased from a constant current generator (whose impedance we assume to be infinite) the loading admittance is $1/Z_L = s\,C_L$. Let us put this back into Eq. 3.3.36 and rearrange it a little:

$$v_G\,s\,C_L = i_i\left(1 + \frac{g_m}{s\,C_{gs}} + \frac{C_L}{C_{gs}}\right) \tag{3.9.37}$$

Furthermore:

$$v_G = i_i\left(\frac{1}{s\,C_L} + \frac{g_m}{s^2\,C_{gs}\,C_L} + \frac{1}{s\,C_{gs}}\right)$$

$$= i_i\,\frac{s\,(C_{gs} + C_L) + g_m}{s^2\,C_{gs}\,C_L} \tag{3.9.38}$$

The input impedance (without C_{gd}, hence the prime [$'$]) is then:

$$Z_i' = \frac{v_g}{i_i} = \frac{s\,(C_{gs} + C_L) + g_m}{s^2\,C_{gs}\,C_L} \tag{3.9.39}$$

To see more clearly how this impedance is comprised, we invert it to find the admittance and apply the continuous fraction synthesis in order to identify the individual components.

$$Y_i' = \frac{s^2\,C_{gs}\,C_L}{s\,(C_{gs} + C_L) + g_m} = s\,\frac{C_{gs}\,C_L}{C_{gs} + C_L} - \frac{g_m\,s\,\dfrac{C_{gs}\,C_L}{C_{gs} + C_L}}{s\,(C_{gs} + C_L) + g_m} \tag{3.9.40}$$

The first fraction is the admittance of the capacitances C_{gs} and C_L connected in series. Let us name this combination C_x:

$$C_x = \frac{C_{gs}\,C_L}{C_{gs} + C_L} \tag{3.9.41}$$

The second fraction, which has a negative sign, must be further simplified. We invert it again, and after some simple rearrangement we obtain the impedance:

$$Z_x = -\frac{(C_{gs}+C_L)^2}{g_m C_{gs} C_L} - \frac{C_{gs}+C_L}{s C_{gs} C_L} \tag{3.9.42}$$

The first part is interpreted as a negative resistance, which we shall label $-R_x$ in order to follow the negative sign in the following analysis more clearly:

$$-R_x = -\frac{(C_{gs}+C_L)^2}{g_m C_{gs} C_L} \tag{3.9.43}$$

The second part as a negative capacitance, which we label $-C_x$ because it has the same absolute value as C_x from the Eq. 3.9.41:

$$-C_x = -\frac{C_{gs} C_L}{C_{gs}+C_L} \tag{3.9.44}$$

Now that we have all the components we can reintroduce the gate–drain capacitance C_{gd}, so that the final equivalent input impedance looks like Fig. 3.9.9. We can write the complete input admittance:

$$Y_i = j\omega (C_{gd}+C_x) - \frac{1}{R_x + \dfrac{1}{j\omega C_x}} \tag{3.9.45}$$

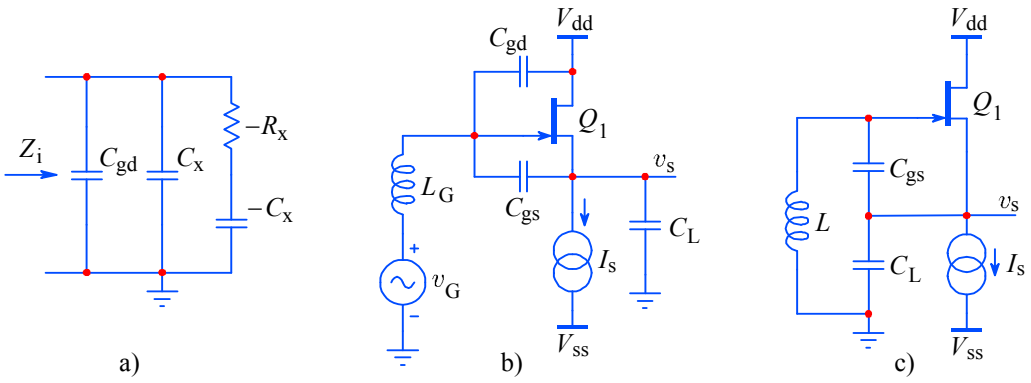

Fig. 3.9.9: a) The equivalent input impedance of the capacitively loaded JFET source follower has negative components which can be a nuisance if, as in b), the signal source has an inductive impedance, forming c) a familiar Colpitts oscillator. If C_{gd} is small, the circuit will oscillate for a broad range of inductance values.

We can separate the real and imaginary part of Y_i by putting Eq. 3.9.45 on a common denominator:

$$Y_i = \Re\{Y_i\} + \Im\{Y_i\}$$

$$= -\frac{\omega^2 C_x^2 R_x}{1+\omega^2 C_x^2 R_x^2} + j\omega \frac{C_{gd}+\omega^2 C_x^2 R_x^2 (C_{gd}+C_x)}{1+\omega^2 C_x^2 R_x^2} \tag{3.9.46}$$

The negative real part can cause some serious trouble [Ref. 3.24]. Suppose we are troubleshooting a circuit with a switching power supply and we suspect it to be a cause of a strong electromagnetic interference (EMI); we want to use a coil with an appropriate inductance L (which, of course, has its own real and imaginary admittance) to inspect the various parts of the circuit for EMI intensity and field direction. If we connect this coil to the source follower and if the coil resistance is low, we would have:

$$\Re\{Y_L\} + \Re\{Y_\mathrm{i}\} \leq 0 \tag{3.9.47}$$

and the source follower becomes a familiar Colpitts oscillator, Fig. 3.9.9c [Ref. 3.25]. Indeed, some older oscilloscopes would burst into oscillation if connected to such a coil and with its input attenuator switched to maximum sensitivity (a few highly priced instruments built by respectable firms, back in early 1970's, were no exception).

By taking into account Eq. 3.9.42, 3.9.43 and 3.9.9 and substituting $\omega_\mathrm{FET} = g_\mathrm{m}/C_\mathrm{gs}$, the real part of the input impedance can be rewritten as:

$$\Re(Y_\mathrm{i}) = G_\mathrm{i} = -g_\mathrm{m}\,\frac{C_\mathrm{L}}{C_\mathrm{gs}} \cdot \frac{(\omega/\omega_\mathrm{FET})^2}{1 + (\omega/\omega_\mathrm{FET}\,D_\mathrm{c})^2} \tag{3.9.48}$$

The last fraction represents the normalized frequency dependence of this admittance:

$$G_\mathrm{iN} = \frac{(\omega/\omega_\mathrm{FET})^2}{1 + (\omega/\omega_\mathrm{FET}\,D_\mathrm{c})^2} \tag{3.9.49}$$

Fig. 3.9.10 shows the plots of G_iN for the same ratios of $C_\mathrm{L}/C_\mathrm{gs}$ as before. Note the quadratic dependence (of D_c) at high frequencies.

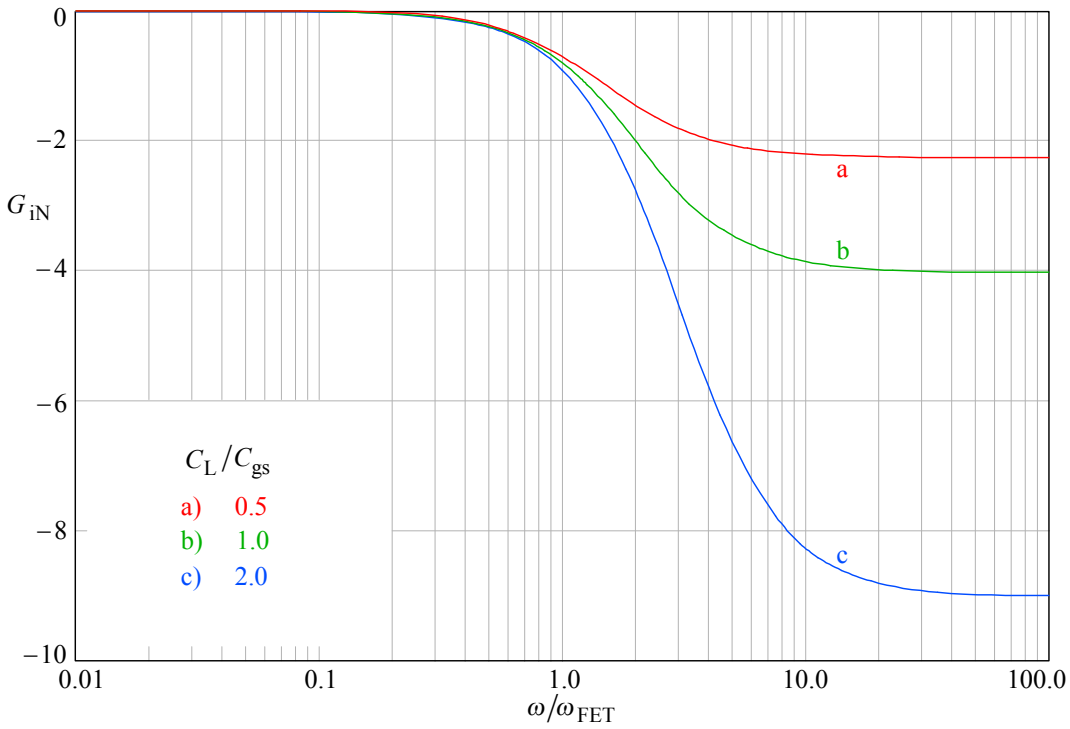

Fig. 3.9.10: Normalized negative input conductance G_iN vs. frequency.

A negative input impedance is always highly undesirable and we shall show a few possible solutions. The obvious way would be to introduce a resistor in series with

the JFET gate; since we should have some series resistance anyway in order to protect the sensitive input from static discharge or accidental overdrive, this will seem to be the preferred choice. However, after a closer look, this protection resistance is too small to prevent oscillations in case of an inductive signal source impedance. The required resistance value which will guarantee stability in all conditions will be so high that the bandwidth will be reduced by nearly an order of magnitude. Thus this method of compensation is used only if we do not care how much bandwidth we obtain.

A more elegant method of compensation is the one which we have used already in Fig. 3.5.3. If we introduce a serially connected $R_x C_x$ network in parallel with the JFET input, as shown in Fig. 3.9.11, we obtain $Y_x = 0$ and $Z_x = \infty$. Note the corresponding phasor diagram: we first draw the negative components, $-R_x$ and $-C_x$, find the impedance vector $-Z_x$ and invert it to find the negative admittance, $-Y_x$. We then compensate it by a positive admittance Y_x such that their sum $Y_{ic} = 0$. We finally invert Y_x to find Z_x and decompose it into its real and imaginary part, R_x and C_x:

$$Y_{ic} = \frac{1}{-R_x - \dfrac{1}{j\omega C_x}} + \frac{1}{R_x + \dfrac{1}{j\omega C_x}} = 0 \qquad (3.9.50)$$

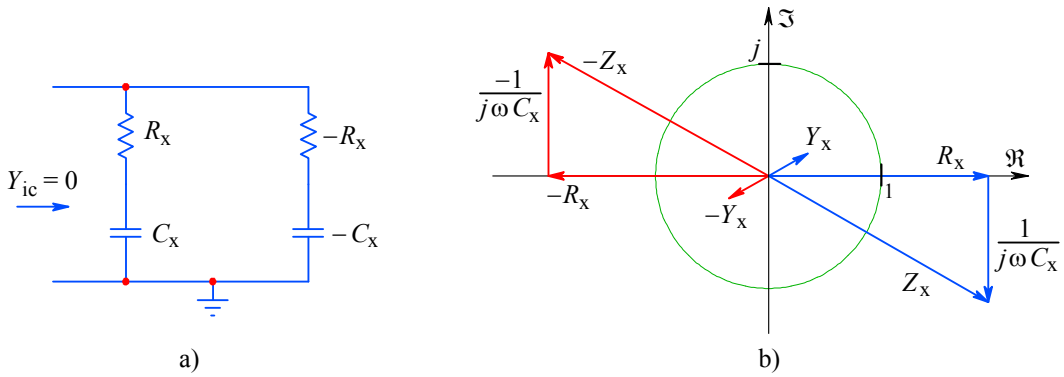

Fig. 3.9.11: a) The negative components of the input impedance can be compensated by an equal but positive network, connected in parallel, so that their admittances sum to zero (infinite impedance). In b) we see the corresponding phasor diagram.

With this compensation, the total input impedance is the one belonging to the parallel connection of C_{gd} with C_x and assuming a 1 MΩ gate bias resistor R_{in}:

$$Z_i = \frac{1}{\dfrac{1}{R_{in}} + j\omega(C_{gd} + C_x)} = \frac{R_{in}}{1 + j\omega\left(C_{gd} + \dfrac{C_{gs}\,C_L}{C_{gs} + C_L}\right)R_{in}} \qquad (3.9.51)$$

The analysis of the input impedance would be incomplete without Fig. 3.9.12, where the Nyquist diagrams of the impedance are shown revealing its frequency dependence, as well as the influence of different signal source impedances.

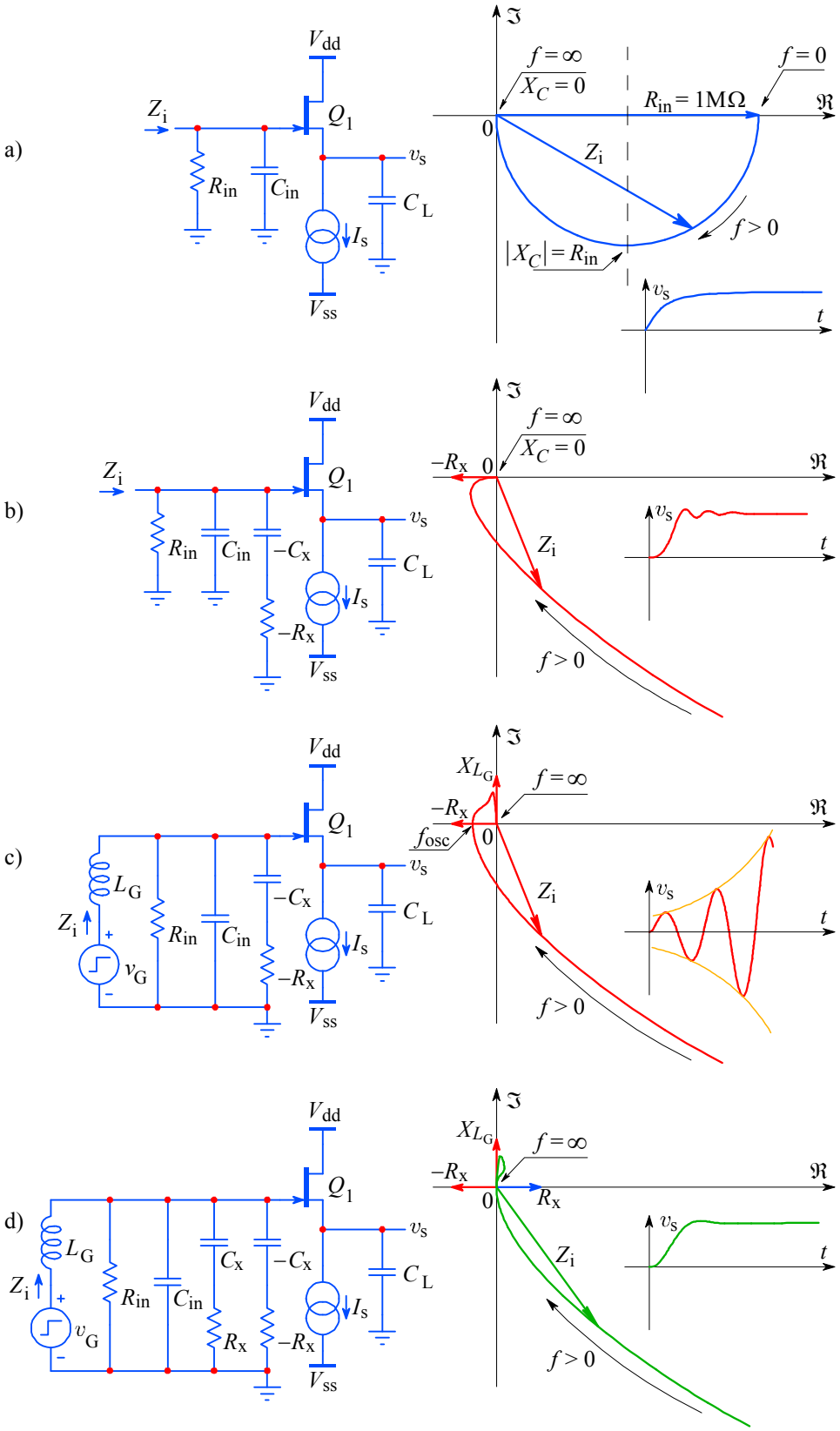

Fig. 3.9.12: **a)** The input impedance of the JFET source follower, assumed to be purely capacitive and in parallel with a 1 MΩ gate biasing resistor; thus at $f = 0$ we see only the resistor and at $f = \infty$ the reactance of the input capacitance is zero; **b)** the negative input impedance components affect the input impedance near the origin; **c)** with an inductive signal source, the point in which the impedance crosses the negative real axis corresponds to the system resonant frequency, provoking oscillations. **d)** The compensation removes the negative components.

In Fig. 3.9.12a the JFET gate is tied to ground by a 1 MΩ resistor, which, with a purely capacitive input impedance, would give a phasor diagram in the form of a half circle with frequency varying from DC to infinity.

In Fig. 3.9.12b we concentrate on the small area near the complex plane origin (high frequencies, close to f_{FET}), where we draw the influence of the negative input impedance components, assuming a resistive signal source.

In Fig. 3.9.12c an inductive signal source (with a small resistive component) will cause the impedance crossing the real axis in the negative region, therefore the circuit would oscillate at the frequency at which this crossing occurs.

Finally, in Fig. 3.9.12d we see the same situation but with the negative components compensated as in Fig. 3.9.11. Note the small loop in the first quadrant of the impedance plot — it is caused by the small resistance R_G of the coil L_G, the coil inductance, and the total input capacitance C_{in}.

In Fig. 3.9.13 we see yet another way of compensating the negative input impedance. Here the compensation is achieved by inserting a small resistance R_d in the drain, thus allowing the anti-phase signal at the drain to influence the gate via C_{gd} and cancel the in-phase signal from the JFET source via C_{gs}. This method is sometimes preferred over the former method, because the PCB pads, which are needed to accommodate the additional compensation components, also create some additional parasitic capacitance from the gate to ground.

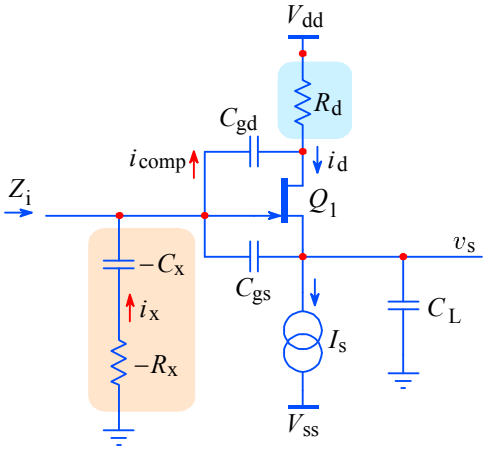

Fig. 3.9.13: Alternative compensation of the input impedance negative components, using negative feedback from the JFET drain.

It should be noted, however, that the negative input impedance compensation can be achieved for small signals only. Large signals vary the JFET gate's reverse bias voltage and the drain–source voltage considerably, therefore both C_{gs} and C_{gd}, as well as g_m, change with voltage. We therefore expect some nonlinear effects to appear with a large signal drive. We shall examine this and some other aspects of the source follower's performance in Part 5.

Résumé of Part 3

In this part we have analyzed some basic circuits for wideband amplification, examined their most important limitations, and explained several ways of improving their high frequency performance. The property which can cause most trouble, even for experienced designers, is the negative input impedance of some of the most useful wideband circuits, and we have shown a few possible solutions.

The reader must realize, however, that the analytical tools and solutions presented are by no means the ultimate design examples. For a final design, many other aspects of circuit performance must also be carefully considered, and, more often than not, these other factors will compromise the wideband performance severely.

As we have indicated at some points, there are ways of compensating certain unwanted circuit behavior by implementing the system in a differential configuration, but, on the negative side, this doubles the number of active components, increasing cost, power dissipation, circuit size, strays and parasitics and also the production and testing complexity. From the wideband design point of view, having many active components usually means many more poles and zeros that must be carefully analyzed and appropriately 'tuned'.

In Part 4 and Part 5 we shall explain some theoretical and practical techniques for an efficient design approach at the system level.

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