# *VCS Simulator Summary*

Your startup environment (in your `.bashrc file`) includes this alias:

```
alias vcs='vcs -gui -R +charge_decay +pathpulse +v2k'
```

To avoid this alias (you usually would not want to), invoke `\vcs` instead of `vcs`.

You must provide a valid verilog file name when you invoke VCS; if the file has a syntax error, VCS will exit immediately with an informative error message.

For one verilog file, invoke `vcs` *filename*

To invoke VCS on a design of several files, the names (with path if necessary) must be listed top-down in a file. Then, invoke VCS on the file (using `-f`):

```
vcs -f file_with_design_files_listed
```

***Graphical UI hints (for Introductory Lab 1):***

After invoking `vcs -f Intro_Top.vcs`

a GUI control window will appear. Notice that the `[Hierarchy]` window (left side of GUI) displays the design structure. Pick each `[+]` to expand the views until all are `[-]`. You can see that `Testbench` contains an instance of `Intro_Top` named `Topper01`, and that `Topper01` contains three other instances, one of `SR`, one of `XorNor`, and one of `AndOr`.

To run the ***Intro*** simulation: [*NOTE: Old and new VCS commands differ here.*]

1. Pick `[File]/[Load Session...]`; on the form, select "`session_Intro_Top.tcl`" and `[Load]` it. A wave window will appear, preloaded with a set of signals to be simulated.

   ***For other labs*** with no `session_*.tcl` file, do this instead: (*a*) highlight any variable(s) in the *VCS* verilog text window and: Either (*b*) pick `[Signal]/[Add to Waves]` or (*b*) pick `[New Wave View]` in the drop-down menu with the  icon.

   Then, in the new wave window, pick `[Simulator]/[Rebuild and Start]`. This compiles the design files listed in `Intro_Top.vcs` and creates an executable named **`simv`**. Whenever you change the verilog, this is what you must do to recompile it Also, the explicit `Start` sets the current simulation time to 0 ns, visible at the upper left of the wave window. You may create a console message window using the  icon at the bottom of any wave window; hover the cursor over this icon to view messages in a help balloon.

2. To run the simulation to completion, press {`F5`} or pick `[Simulator]/[Start|Continue]`. The simulation will stop, and the wave window will display the trailing signal states.

3. To view the complete simulation waveforms, pick the zoom-full  icon.

4. Measure a time difference: Use the left mouse button to pick the first rising edge of **`Cstim`**; use the middle mouse button on the first rising edge of **`Dstim`**. You should get 50 ns.

5. Try `[Simulator]/[Rebuild and Start]` to rerun the simulation and redisplay the results in a second wave window. Use [`File`]/[`Exit`] to close all VCS windows.

***Special hints (for labs after Lab 1)*:**

When simulating a netlist, it is useful to add "`-v `" before the library line in the `.vcs` file: VCS then compiles only those models actually in the design. Use `vcs -help` to see all available VCS options.

You can save your VCS gui window setup and signal choices with [File]/[Save Session...]. The saved session file is a Tcl script.