John Michael Williams

Digital VLSI Design with Verilog

A Textbook from Silicon Valley Polytechnic Institute, *Second Edition*

This book is structured as a step-by-step course of study along the lines of a VLSI integrated circuit design project. The entire Verilog language is presented, from the basics to everything necessary for synthesis of an entire 70,000 transistor, full-duplex serializer-deserializer, including synthesizable PLLs. The author includes everything an engineer needs for in-depth understanding of the Verilog language: Syntax, synthesis semantics, simulation, and test. Complete solutions for the 27 labs are provided in the downloadable files that accompany the book. For readers with access to appropriate electronic design tools, all solutions can be developed, simulated, and synthesized as described in the book. A partial list of design topics includes design partitioning, hierarchy decomposition, safe coding styles, back annotation, wrapper modules, concurrency, race conditions, assertion-based verification, clock synchronization, and design for test. A concluding presentation of special topics includes SystemVerilog and Verilog-AMS.

- Covers the entire Verilog language – using most of it in practice;
- Provides 27 lab exercises, with complete and tested answers;
- Explains and emphasizes synthesizability, wherever it pertains to language features;
- Develops as a major project a synthesizable 70,000-gate SerDes;
- Presents synthesis-relevant usage of *SystemVerilog*, and the basic functionality of *Verilog-AMS*.

Electrical Engineering

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